High Efficiency 2.7A Synchronous Boost Convertor

General Description

The LP6252 is a current mode, constant frequency step-up converter. It has typical 2.7A switch current limit. The LP6252 operates with a switching frequency at 1MHz with internal compensation, which reduces the number of external components and minimizes the size of inductor and capacitor.

The devices allows the extern resistor to program the output voltage, it can support output up to 5.5V.

In shutdown mode ,the output is disconnected form the input and current consumption is reduced to less than 1 μA.

The devices are available in SOT23-6 and TDFN-6 package.

Features

- Up to 95% efficiency
- Output to Input Disconnect at Shutdown Mode
- Shutdown current:<1uA
- Output voltage Up to 5.5V
- Over Output Voltage Protection
- Over Current Protection
- Over Temperature Protection
- Internal Compensation of Soft-start
- 1MHz fixed frequency switching
- High switch current limit :2.7A
- Available in SOT23-6 and TDFN-6 Package

Order Information

LP6252 □ □ □

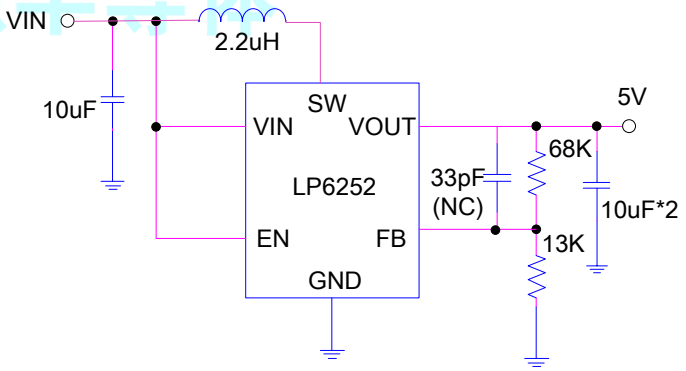
F: Halogen Free and Pb Free

Package Type

B6: SOT23-6

QV:TDFN-6

Typical Application Circuit



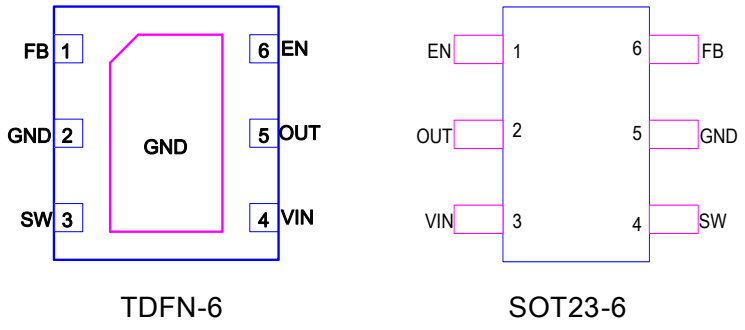
Applications

- ✧ Battery products
- ✧ Host Products
- ✧ Panel

Marking Information

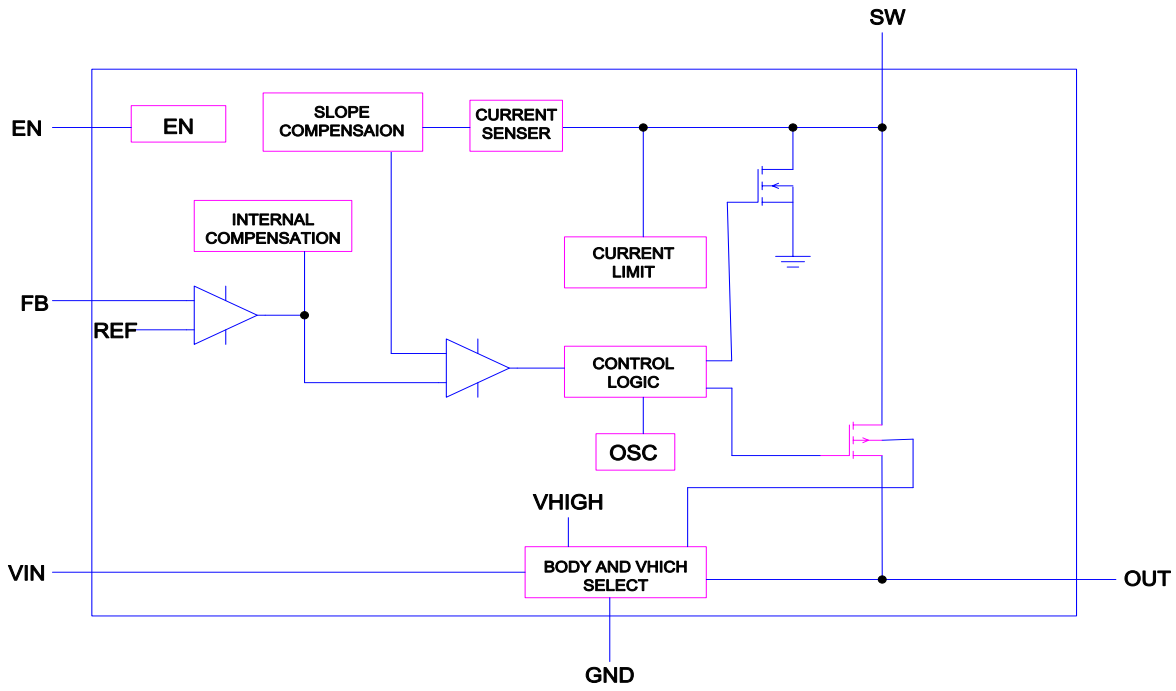
Device	Marking	Package	Shipping
LP6252B6F	LPS 5VYWX	SOT23-6	3K/REEL
LP6252QVF	LPS 5TYW	TDFN-6	4K/REEL
Marking indication: Y:Production year W:Production period X:Production batch			

Functional Pin Description

Package Type	Pin Configurations
TDFN-6 / SOT23-6	 TDFN-6 SOT23-6

Pin		Name	Description
TDFN-6	SOT23-6		
1	6	FB	Voltage Feedback Input pin. Connect to an external resistive voltage divider from the output to FB to set the output voltage. The feedback voltage is 0.8V.
2	5	GND	Power ground and Analog ground.
3	4	SW	Power Switching node.
4	3	VIN	Power supply input.
5	2	OUT	Boost Converter output.
6	1	EN	Enable logic input. Logic high enables the device. Logic low disables the device.

Function Diagram



Absolute Maximum Ratings Note 1

- ✧ Input and VOUT to GND ---------- -0.3 to 6.3V
- ✧ Other Pin to GND (FB,EN,SW) ---------- -0.3 to 6.3V
- ✧ Maximum Junction Temperature ---------- 150°C
- ✧ Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C
- ✧ Storage Temperature Range ---------- -60℃ to 125°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (SOT23-6, PD,T_A=25℃) ---------- 0.45W
- ✧ Thermal Resistance (SOT23-6, J_A) ---------- 250℃/W
- ✧ Maximum Power Dissipation (TDFN-6, PD,T_A=25℃) ---------- 1.2W
- ✧ Thermal Resistance (TDFN-6, J_A) ---------- 95℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

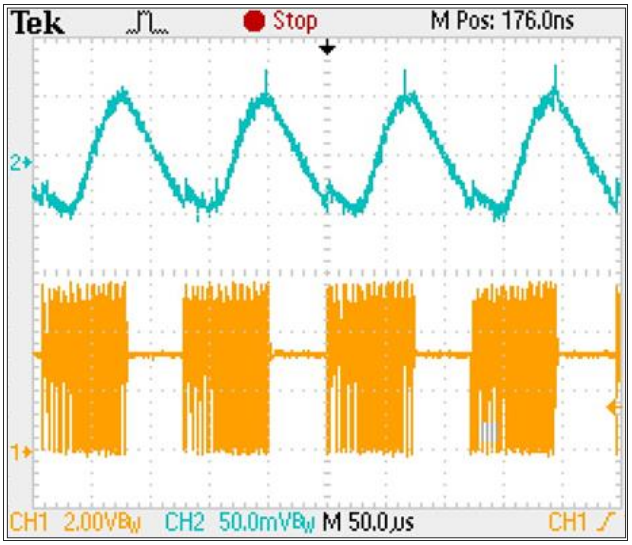
Electrical Characteristics

(V_{IN}=3.5V, V_{OUT}=5V, C_{IN}=10uF, C_{OUT}=22uF, L=2.2uH, R_1=68K, R_2=13K)

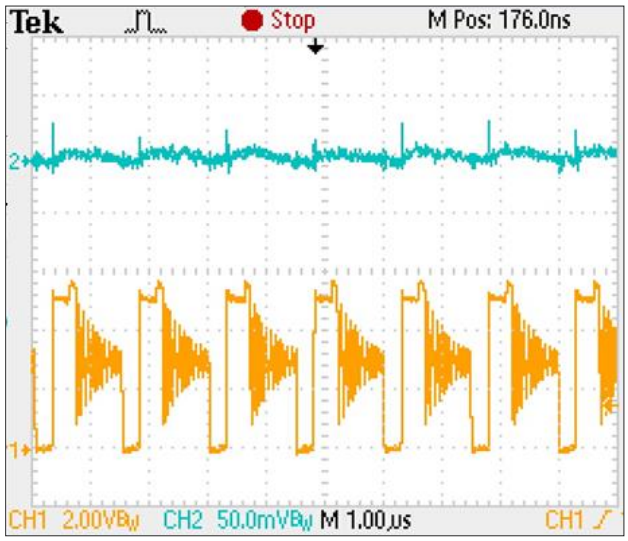
Parameter	Condition	Min	Typ	Max	Units
Supply Voltage		2.5		5.5	V
Output Voltage Range		2.5		5.5	V
UVLO		1.8		2.4	V
Supply Current(Shutdown)	V_{EN}=0V,V_{IN}=5V		0.05	1	uA
Feedback Voltage		784	800	816	mV
Feedback Input Current	V_{FB}=0.82V		50		nA
Switching Frequency			1		MHz
Maximum Duty Cycle		80	90	95	%
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.4			V
Low-side Current Limit		2.7	3		A
High-side On Resistance	V_{OUT}=3.3V		200		mΩ
Low-side On Resistance			150		mΩ

Over temperature protection			150		℃

Typical Operating Characteristics

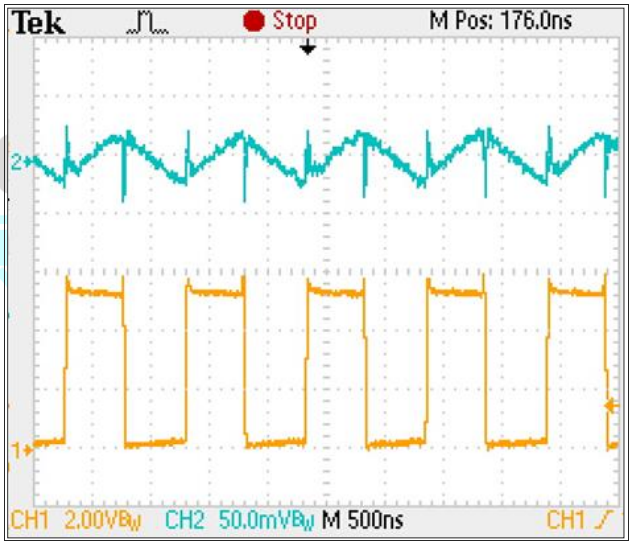


V_{OUT}=5V, V_{IN}=3V, I_{OUT}=2mA, $CH_1=V_{SW}$,$CH_2=\triangle V_{OUT}$

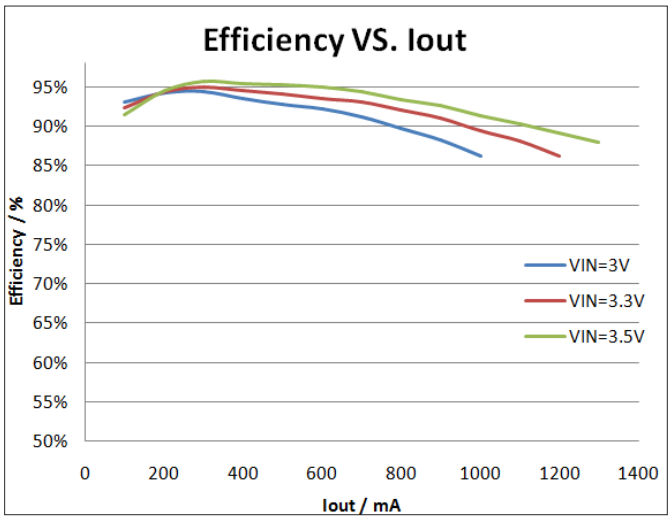


V_{OUT}=5V, V_{IN}=3V, I_{OUT}=100mA, $CH_1=V_{SW}$,$CH_2=\triangle V_{OUT}$

V_{OUT}=5V, V_{IN}=3V, I_{OUT}=500mA, $CH_1=V_{SW}$,$CH_2=\triangle V_{OUT}$



V_{OUT}=5V, V_{IN}=3V, I_{OUT}=1A, $CH_1=V_{SW}$,$CH_2=\triangle V_{OUT}$



Operation Information

The LP6252 is a high efficiency synchronous boost converter. The device supports a wide input voltage range from 2.5V to 5.5V and output voltage rage from 2.5V to 5.5V.

When the LP6252 is disabled, there is no current path from SW to OUT. When the LP6252 is enabled, a limited start-current charges the output voltage rising to SW, then the part operates in force PWM mode for regulating the output voltage to the target value. At the beginning of each cycle, the N-channel MOSFET switch is turned on, forcing the inductor current to rise, The current at the source of the switch is internally measured and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage. When the inductor current rises sufficiently, the PWM comparator turns off the switch, forcing the inductor current to the output capacitor through the internal P-Channel MOSFET rectifier, which forces the inductor current to decrease. The peak inductor current is controlled by the error voltage. Thus the output voltage controls the inductor current to satisfy the lode.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. Use a 100K resistor for R_2 of the voltage divider. Determine the high-side resistor R_1 by the equation:

$$V_{OUT} = (R_1 / R_2 + 1) \times V_{FB}$$

Pre-Boost Current and Short Circuit Protect

Initially output voltage is lower than battery voltage, and the LP6252 enters pre-boost phase. During pre-boost phase, the internal NMOSFET/PMOSFET is turned off/on and a constant current is provided from battery to output until the output voltage close to the battery voltage. The constant current is limited by internal controller. If the output short to ground, the LP6252 also limits the output current to avoid damage condition

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitors are recommended. The tantalum capacitors can be used as well, but the ESR is bigger than ceramic capacitor. The output voltage ripple consists of two components: one is the pulsating output ripple current flows through the ESR, and the other is the capacitive ripple caused by charging and discharging.

$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C}$$

$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \times f_{OSC}} \right)$$

Inductor Selection

For a better efficiency in high switching frequency converter, the inductor selection has to use a proper core material such as ferrite core to reduce the core loss and choose low ESR wire to reduce copper loss. The most important point is to prevent the core saturated when handling the maximum peak current. Using a shielded inductor can minimize radiated noise in sensitive applications. The maximum peak inductor current is the maximum input current plus the half of inductor ripple current. The calculated peak current has to be smaller than the current limitation in the electrical characteristics. A typical setting of the inductor ripple current is 20% to 40% of the maximum input current. If the selection is 40%, the maximum peak inductor current is

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} I_{RIPPLE} = 1.2 \times I_{IN(MAX)}$$
$$= 1.2 \times \left[\frac{I_{OUT(MAX)} \times V_{OUT}}{\eta \times V_{IN(MIN)}} \right]$$

The minimum inductance value is derived from the following equation :

$$L = \frac{\eta \times V_{IN(MIN)}^2 \times [V_{OUT} - V_{IN(MIN)}]}{0.4 \times I_{OUT(MAX)} \times V_{OUT}^2 \times f_{OSC}}$$

Depending on the application, the recommended inductor value is between 1μH to 4.7μH.

Input Capacitor Selection

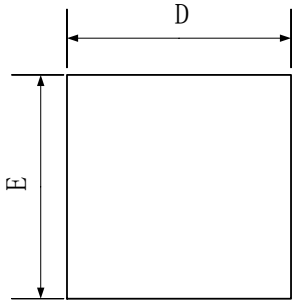
For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 10μF input capacitor is sufficient for most applications. For a lower output power requirement application, this value can be decreased.

Layout Guide

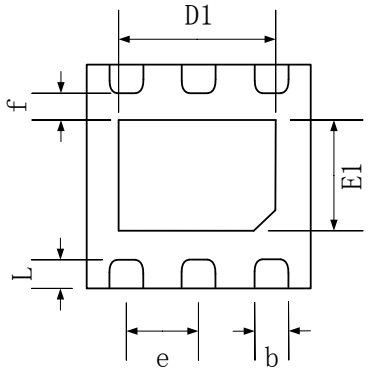
For high frequency switching power supplies, the PCB layout is important step in system application design. In order to let IC achieve good regulation, high efficiency and stability, it is strongly recommended the power components(Inductor, input and output capacitor) should be placed as close as possible to chip. The set races should be wide and short. The feedback pin and then works of feedback and compensation should keep away from the power loops, and be shielded with a ground trace or plane to prevent noise coupling.

Packaging Information

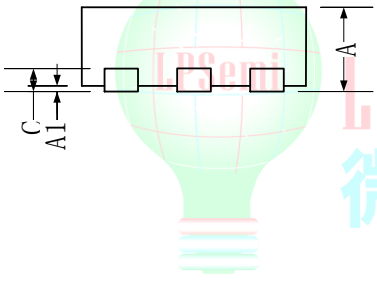
TDFN-6



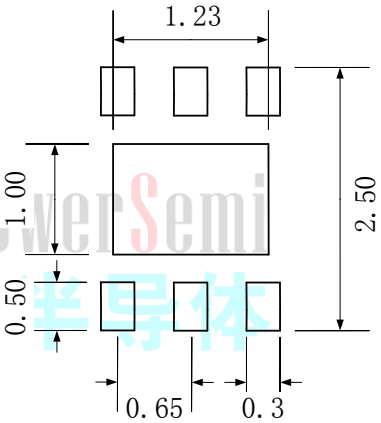
TOP VIEW



BOTTOM VIEW



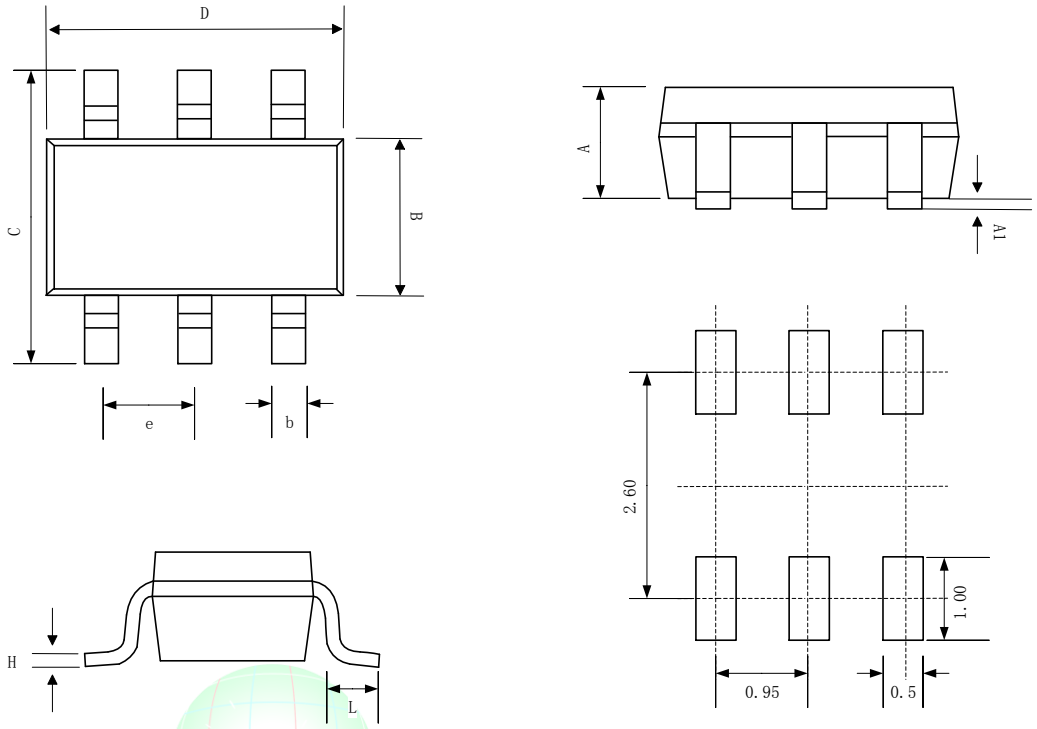
SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.22	0.30	0.35
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D1	1.00	1.23	1.70
E	1.90	2.00	2.10
E1	0.50	0.70	1.10
e	0.65 BSC		
L1	0.20	0.30	0.40
f	0.20	-	-

SOT23-6



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610