800mA Single Chip Li-Ion and Li-Polymer Charger with NTC and High input withstand voltage

General Description

LP4040 is a complete constant-current/ constant voltage linear charger for single cell lithium-ion battery. No external sense resistor is needed, and no blocking diode is required due to the internal MOSFET architecture. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature. The charge voltage is fixed at 4.2V, and the charge current can be programmed externally with a single resistor.

The LP4040 automatically terminates the charge cycle when the charge current drops below the programmed termination threshold after the final float voltage is reached.

When the input supply is removed, the device automatically enters a low current state, dropping the battery drain current to less than 1μA.

Other features include charge current monitor, under voltage lockout, automatic recharge, status pins to indicate charging state and the presence of an input voltage and an NTC thermistor input used to monitor battery temperature.

Order Information

LP4040 □□ □

- F: Pb-Free
- Package Type
  QV: TDFN-10

Features

- Input Voltage up to 30V
- Battery Maximum Voltage up to 17V
- Input Over Voltage Protection：6V
- NTC Thermistor Input for Temperature Qualified Charging
- Short-circuit Protection
- Programmable Charge Current up to 800mA
- Less Than 1μA Battery Reverse Current
- Protection of Reverse Connection of Battery
- No MOSFET, Sense Resistor or Blocking Diode Required
- Constant-Current / Constant-Voltage Operation with Thermal Regulation to Maximize Charge Rate Without Risk of Overheating
- TDFN-10L Package
- RoHS Compliant and 100% Lead (Pb)-Free

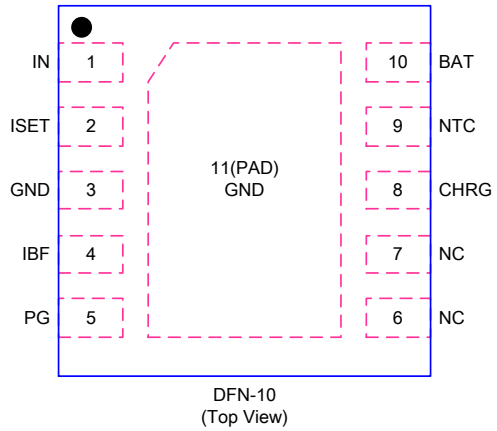
Applications

- Portable Media Players/Game
- Power Bank
- Bluetooth Applications
- PDA/MID

Marking Information

Device	Marking	Package	Shipping
LP4040QVF	LPS LP4040 YWX	TDFN-10	4K/REEL
Marking indication: Y:Production year W:Production week X:Series Number			

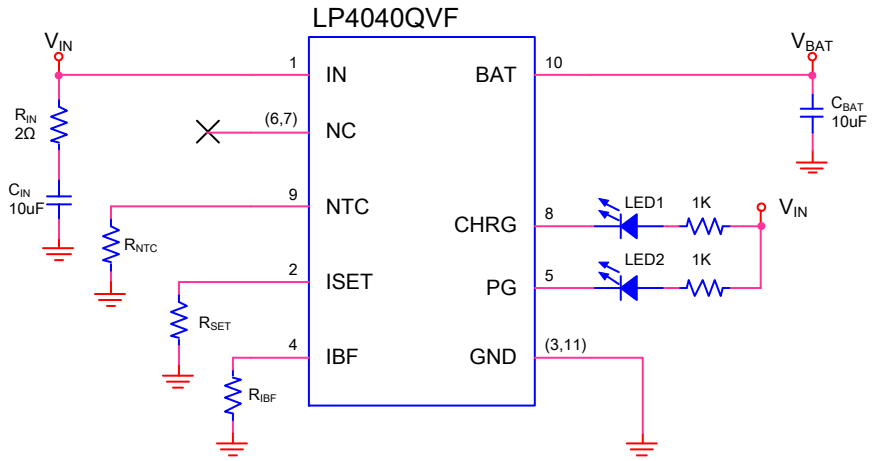
Functional Pin Description

Package Type	Pin Configurations
TDFN-10	

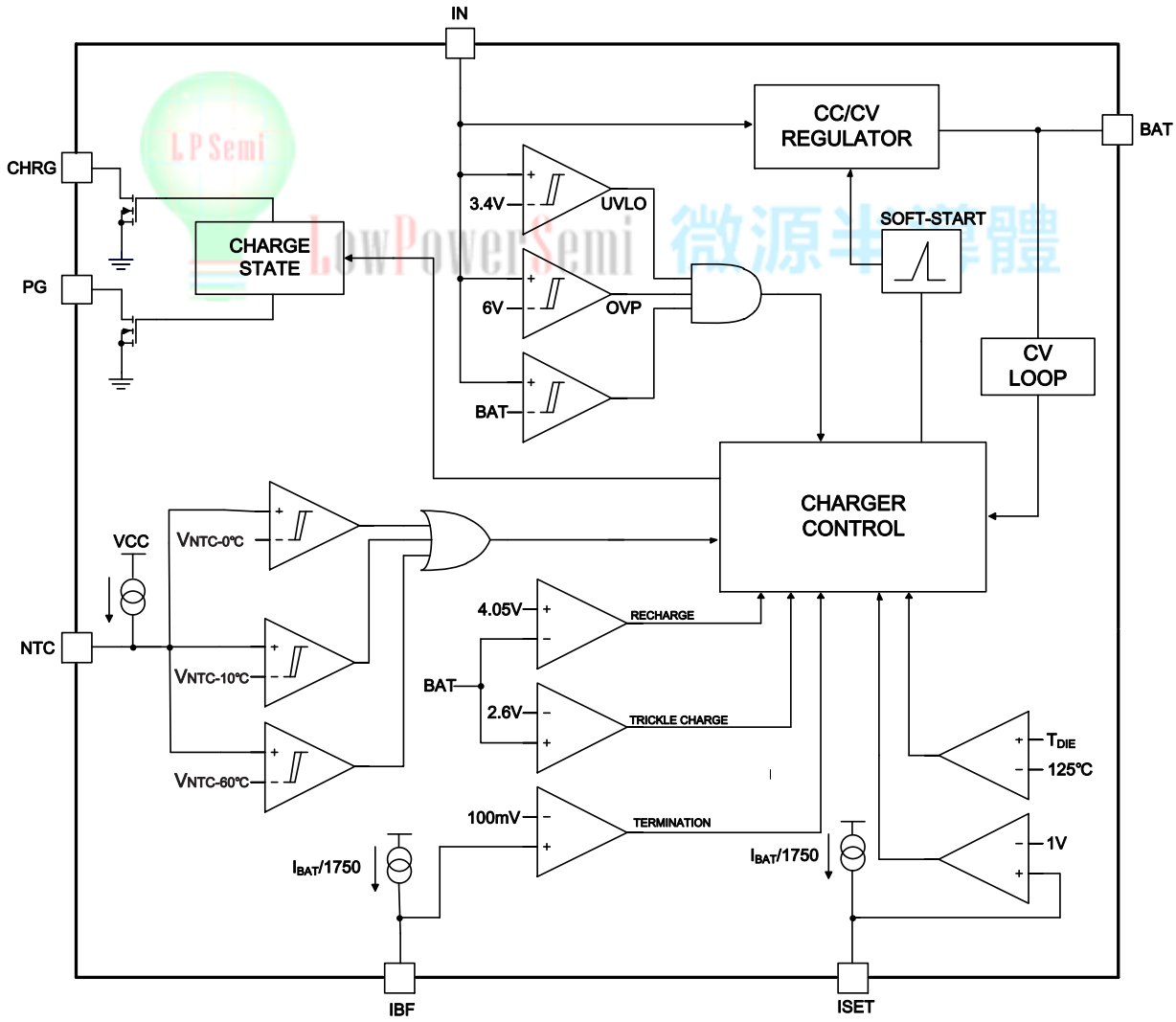
Pin Description

Pin No.	Name	Description
1	IN	IN is the input power source. Connect to a wall adapter.
2	ISET	Charge Current Program. The charge current is programmed by connecting a 1% resistor (R_{SET}) to ground. $I_{BAT} = \frac{1750 \times V_{ISET}}{R_{SET}}$
3	GND	GND is the connection to system ground.
4	IBF	Charge Termination Program. The charge termination current threshold current is programmed by connecting a 1% resistor (R_{IBF}) to ground.
5	PG	Open-Drain Status Output. Low indicates the input voltage is above UVLO and the BAT voltage.
6,7	NC	No Connection.
8	CHRG	Open-Drain Status Output. When the battery is charging, the CHRG pin is pulled low by an internal N-MOS. When the charge cycle is completed, the pin could be pulled High by an external pull high resistor.
9	NTC	Negative Thermal Coefficient (NTC) Thermistor Pin.
10	BAT	BAT is the connection to the battery. Typically a 10μF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 1uF ceramic capacitor is required.
11(PAD)	GND	GND is the connection to system ground.

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings Note 1

- ✧ IN to GND ---------- -0.3V to 30V
- ✧ BAT to GND ---------- -5V to 17V
- ✧ Other Pin to GND ---------- -0.3V to 6.5V
- ✧ Maximum Junction Temperature (T_J)---------- 125℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
- ✧ Storage Temperature ---------- -55℃ to 150℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance (θ_{JA}) ---------- 76℃/W

ESD Susceptibility

- ✧ HBM(Human Body Model) ---------- 2KV
- ✧ MM(Machine Model) ---------- 200V

Electrical Characteristics

(T_A=25℃, V_{IN} = 5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ.	Max	Units
V_{IN}	Input Voltage		4.5	5	5.8	V
I_{IN}	Input Supply Current	charge mode		220		uA
		Standby Mode		215		uA
		Shutdown Mode		240		uA
V_{UV}	Input Under Voltage Lockout Threshold	V_{IN} Rising		4.4		V
V_{UV_HYS}	Input Under Voltage Lockout Hysteresis			100		mV
V_{OVP}	Input Over Voltage Protection Threshold	V_{IN} Rising		6		V
V_{OVP_HYS}	Input Over Voltage Protection Hysteresis			30		mV
I_{BAT}	BAT Pin Current	R_{SET}=3.5KΩ, Current Mode	450	500	550	mA
		R_{SET}=17.5KΩ, Current Mode	90	100	110	mA
		V_{BAT}=4.2V V_{IN}=float or 0V		0.1		uA
V_{FLOAT}	Regulated Output (Float) Voltage	I_{BAT}=40mA	4.158	4.2	4.242	V
V_{ASD}	V_{IN} - V_{BAT} Lockout Threshold Voltage			120		mV
I_{TRIKL}	Trickle Charge Current	V_{BAT}<V_{TRIKL}, R_{SET}=10KΩ		20		%I_{BAT}
V_{TRIKL}	Trickle Charge Threshold Voltage	V_{BAT} Rising		2.6		V
V_{TRIL_HYS}	Trickle Charge Hysteresis Voltage			100		mV
V_{ISET}	ISET Pin Voltage	R_{SET}=10KΩ, Current Mode		1		V
I_{NTC}	NTC bias current			41.5		uA
V_{NTC_0}	Low temperature pending voltage threshold			1.12		V
V_{NTC_10}	Half charging current mode voltage threshold			0.75		V
V_{NTC_60}	High temperature disable voltage threshold			0.17		V
$V_{NTC-DIS}$	NTC function disable voltage threshold			4.45		V
I_{STAT}	Status Pins (CHRG/PG) Weak Pull-Down Current	V_{STAT}=5V			5	uA
V_{STAT}	Status Pins (CHRG/PG) Output Low Voltage	I_{STAT}=5mA			0.5	V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT}-V_{RECHRG}		150		mV
T_{LIM}	Junction Temperature in Constant Temperature Mode			125		℃

Application Information

The LP4040 has built-in input voltage surge protection as high as 30V. The charger IC will be automatically disabled when the input voltage is lower than 4.4V or higher than 6V. The open-drain PG Pin is used to indicate an input power good condition (4.4V<V_{IN}<6V). If the input voltage is lower than the battery voltage, the IC is also disabled to prevent the battery from draining.

A charge cycle begins when the voltage at the VIN pin rises above the UVLO threshold level, when a battery is connected to the charger output. If the BAT pin is less than 2.6V, the charger enters trickle charge mode. In this mode, the LP4040 supplies approximately 1/10 the ISET programmed charge current to bring the battery voltage up to a safe level for full current charging. When the BAT pin voltage rises above 2.6V, the charger enters constant-current mode(CC), where the ISET programmed charge current is supplied to the battery. When the BAT pin approaches the final float voltage, the LP4040 enters constant-voltage mode(CV) and the charge current begins to decrease, and the battery full indication is set when the charge current in the CV mode is reduced to the programmed full battery current.

Charge Current Program

The charge current (I_{BAT}) is set by a resistor (R_{SET}) connecting from the ISET pin to GND. The relationship of the charge current and the programming resistance is established by the following equations.

$$I_{BAT} = \frac{1750 \times V_{ISET}}{R_{SET}}$$

Where V_{ISET} is 1V

Termination Charge Current Program

The battery charge Termination current threshold (I_{BF}) is programmed by connecting a resistor R_{IBF} from the IBF pin to GND:

$$I_{BF} = \frac{R_{SET} \times I_{BAT}}{R_{IBF}}$$

Charge Status Indicator (CHRG/PG)

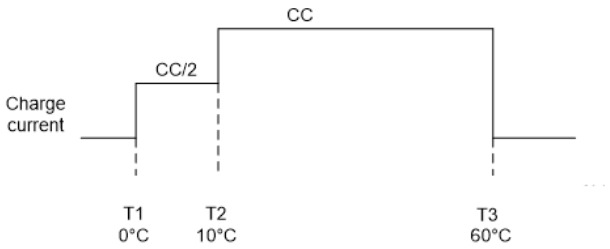
After application of a 5V source, the input voltage rises above the V_{UV} and sleep thresholds (V_{IN}>V_{BAT}+V_{ASD}), but is less than OVP (V_{IN}<V_{OVP}), then the PG turns on and provides a low impedance path to ground. CHRG/FULL has two different states: strong pull-down (~5mA) and high impedance. The strong pull-down state indicates that the LP4040 is in a charge cycle. When the charger is entered CV mode and once the charge current has reduced to the battery full charge current threshold (I_{BF}), the CHRG pin will become high impedance and the FULL pin will become strong pull-down.

Function	CHRG
Charging	Low
Charge finished	Hi-z

Function	PG
V_{IN}<V_{UV}	Hi-z
V_{UV}<V_{IN}<V_{OVP}	Low
V_{OVP}<V_{IN}	Hi-z

Battery Temperature Detection

The NTC function for the LP4040 is designed to follow the new JEITA temperature standard for Li-Ion. There are now three thresholds, 60℃, 10℃, and 0℃. Normal operation occurs between 10℃ and 60℃. If between 0℃ and 10℃ the charge current level is cut in half. Above 60℃ or below 0℃ the charge is disabled.



Thermal protection

The NTC feature is implemented using an internal 47μA current source to bias the thermistor connected from the NTC terminal to GND(designed for use with a 10K Ω NTC β=3370 [SEMITEC 103AT-2 or Mitsubishi TH05-3H103F]). If NTC feature is not needed, a fixed 10kΩ can be placed between NTC and GND to allow normal operation. Since the NTC current is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10KΩ NTC (at 25 ℃).

Automatic Recharge

Once the charge cycle is terminated, the LP4040 continuously monitors the voltage on the BAT pin. A charge cycle restarts when the battery voltage falls below 4.05V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at or near a fully charged condition and eliminates the need for periodic charge cycle initiations.

Thermal Limit

An internal thermal feedback loop reduces the charge current if the die temperature attempts to rise above a preset value of approximately 125℃. This feature protects the LP4040 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LP4040. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.

Power Dissipation

The conditions that cause the LP4040 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Nearly all of this power dissipation is generated by the internal MOSFET calculated to be approximately:

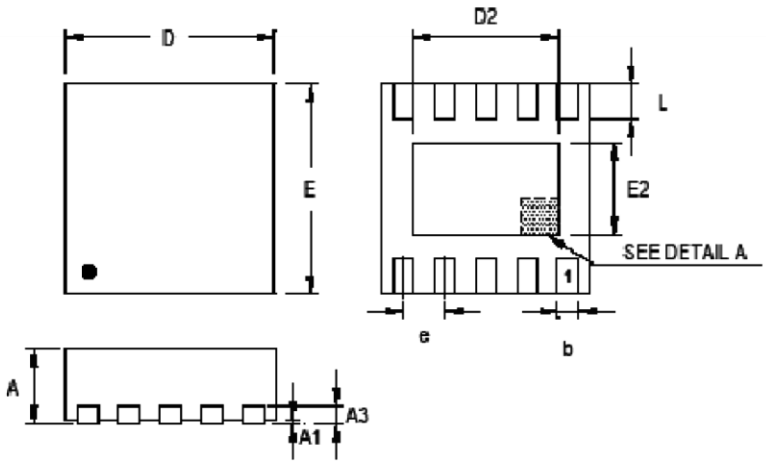
$$P_D = (V_{IN} - V_{BAT}) \times I_{BAT}$$

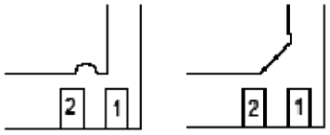
Where P_D is the power dissipated, V_{IN} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 125℃ - P_D \times \theta_{JA}$$

Package Information

TDFN-10L(2*2)





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions in millimeters		Dimensions in inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.150	0.250	0.006	0.010
b	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D2	1.300	1.500	0.051	0.059
E	1.900	2.100	0.075	0.083
E2	0.800	1.000	0.031	0.039
e	0.400		0.016	
L	0.250	0.350	0.010	0.014