LP6451

18V/3A Synchronous BUCK Switching Converter

Features

- Wide input voltage range: 4.2V – 18V
- Output voltage range: 0.6V – 7V
- High efficiency operation
  - Integrated an 50-mΩ LS-MOSFET and an 80-mΩ HS-MOSFET
  - 90% efficiency at 3A load from 12V to 5V conversion
- Automatic PFM mode at light load
- ±1% Vref accuracy
- Typical 1.2-MHz switching frequency
- COT control scheme with fast load transient response
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- 1.0ms typical soft-start time
- 1.6mm X 2.9mm SOT23-6 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV and TV box
- 12V Industrial bus applications

General Description

The LP6451 is a synchronous buck converter supporting up to 3A output current. The LP6451 employs an adaptive constant-on-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP6451 supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP6451 integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP6451 also integrates multiple protection functions, i.e., over-current protection (OCP), overtemperature protection (OTP), under-voltage lockout (UVLO), and short circuit protection (SCP).

The LP6451 is available in a small 6-pin 1.6mmX2.9mm SOT23-6 package.

Order Information

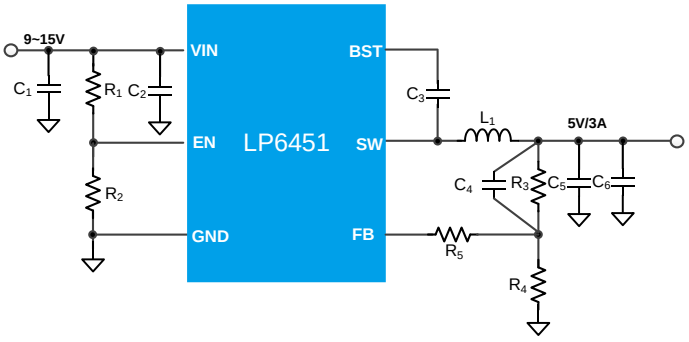
LP6451 □□ □

F:Green/Pb Free

Package Type

B6 : SOT23-6

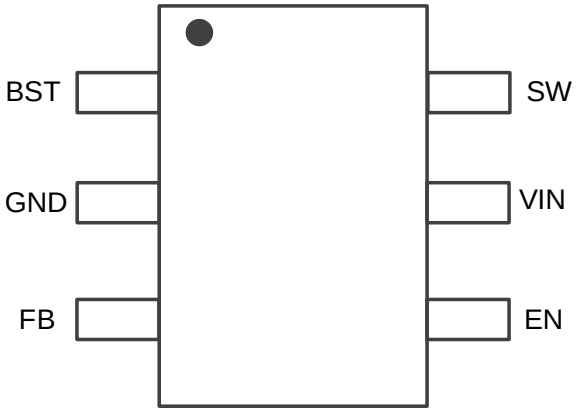
Typical Application Circuit



Device Information

Part Number	Top Marking	Operation Mode	Package	Shipping
LP6451B6F	LPS AQYWX	PFM	SOT23-6	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



SOT23-6
(Top View)

LP6451 Pinout

Pin Description

Pin #	Name	Description
1	BST	Bootstrap pin. Power supply for high-side MOSFET gate driver. A 0.1-µF capacitor must be connected between this pin and the SW pin.
2	GND	Power ground of the IC.
3	FB	Feedback pin. Use a resistor divider to set the desired output voltage.
4	EN	Enable input. This pin can be used to control the system power sequence.
5	VIN	IC power supply input.
6	SW	The switching node of the converter.

Absolute Maximum Ratings (Note)

VIN, SW, and EN to GND ---------- -0.3V to 18V
FB to GND ---------- -0.3V to 6.5V
BST to SW ---------- -0.3V to 6.5V
SW to GND （5ns transient） ---------- -3.5V to 20V
Operating Ambient Temperature Range (TA) ----------40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec) ----------260℃

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
CDM (Charged-device Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ----------160℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.2		18	V
V_{OUT}	Output voltage	0.6		7	V
L	Inductor	1		4.7	μH
T_A	Ambient temperature range	-40		85	°C
C_{IN}	Input decoupling capacitor	4.7		100	μF
C_{OUT}	Output capacitor	10		100	μF

Electrical Characteristics

(The specifications are measured under conditions V_{IN} = 12V, T_J = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_R}	Input under voltage lockout threshold	V_{IN} rising threshold		4.0	4.2	V
V_{ULVO_H}	UVLO hysteresis	V_{IN} falling threshold		0.3		V
I_{q_VIN}	Input quiescent current	No switching, EN=3V, FB=1.0V		440	550	μA
I_{sd_VIN}	Input shutdown current	EN=0, V_{IN}=12V		3		μA
BUCK CONVERTER						
I_{LIM}	Low-side valley current limit	T_J=25ºC	3.3	4.2	5.0	A

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	T_J=25°C	0.594	0.6	0.606	V
R_{dson_HS}	High-side FET on resistance	V_{IN}=12V		80		mΩ
R_{dson_LS}	Low-side FET on resistance	V_{IN}=12V		50		mΩ
F_{sw}	Switching frequency			1200		kHz
t_{on-min}	Minimum on-time[1]			50		ns
$t_{off-min}$	Minimum off-time[1]	V_{FB}=V_{ref} - 0.2V		100		ns
t_d	EN delay time[1]	From EN high to first switching		500		μs
t_{ss}	Soft-start time[1]	From first switching to 95%Vref		0.75		ms
T_{jsd}	Thermal shutdown threshold	Rising threshold		160		°C
	Thermal shutdown threshold	Falling threshold		135		°C
I_{leak_FB}	FB pin leakage current			0.01		μA
EN Logic						
V_{EN}	EN pin logic high threshold	EN Rising threshold	1.14	1.2	1.26	V
V_{hys}	EN pin threshold hysteresis			0.2		V
	EN pin internal pull-down resistance			900		kΩ

[1]: Not production tested. Guaranteed by design.

Typical Characteristics

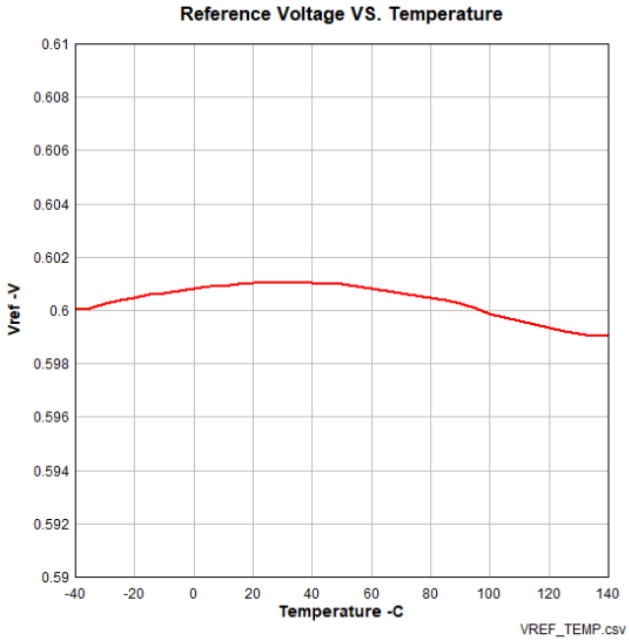


Figure 1. Reference voltage VS. Junction Temperature

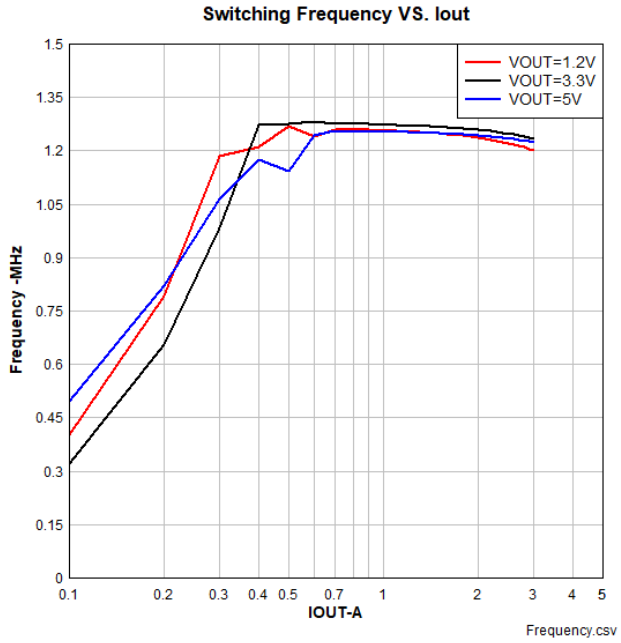


Figure 2. Switching Frequency VS. Output Current

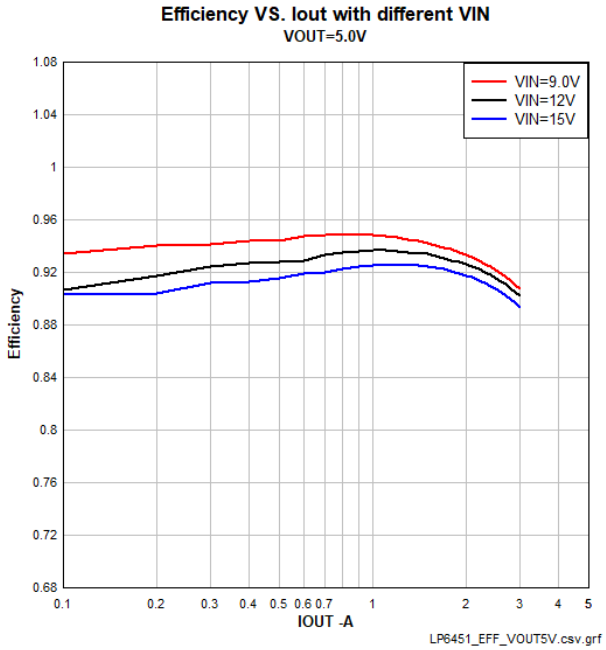


Figure 3. VOUT=5.0V, Efficiency, L=2.2 μ H

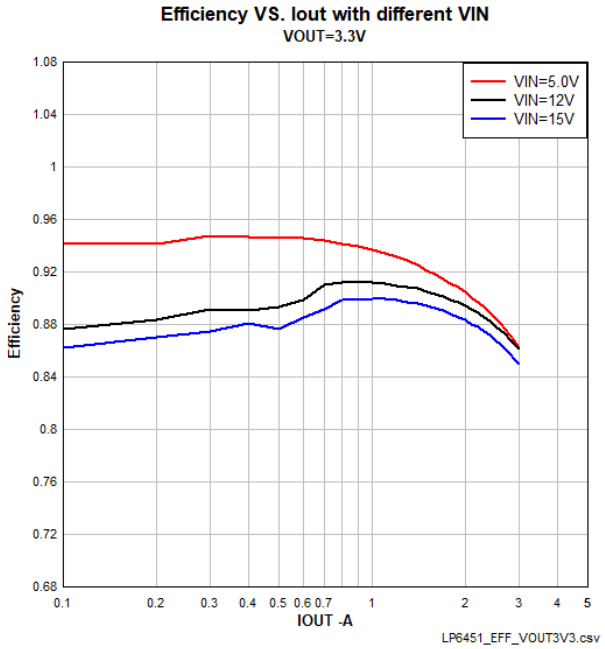


Figure 4. VOUT=3.3V, Efficiency, L=2.2 μ H

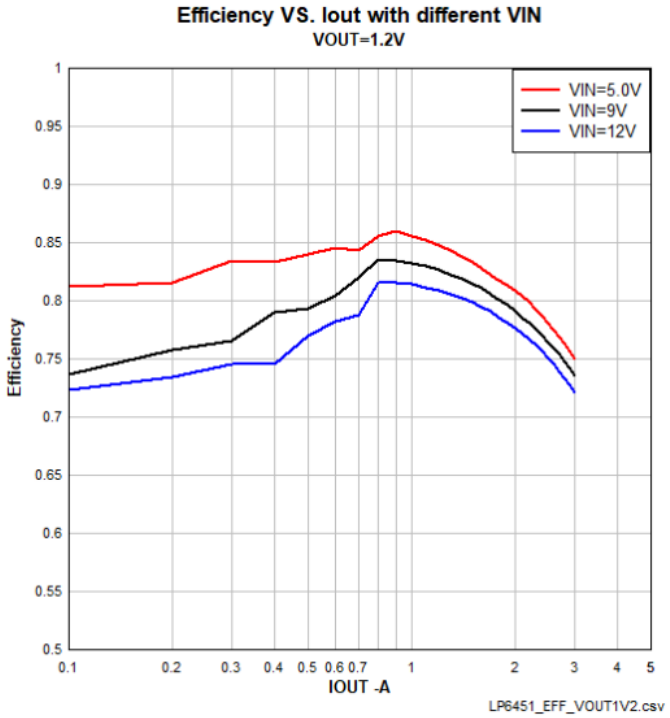


Figure 5. VOUT=1.2V, Efficiency, L=1 μ H

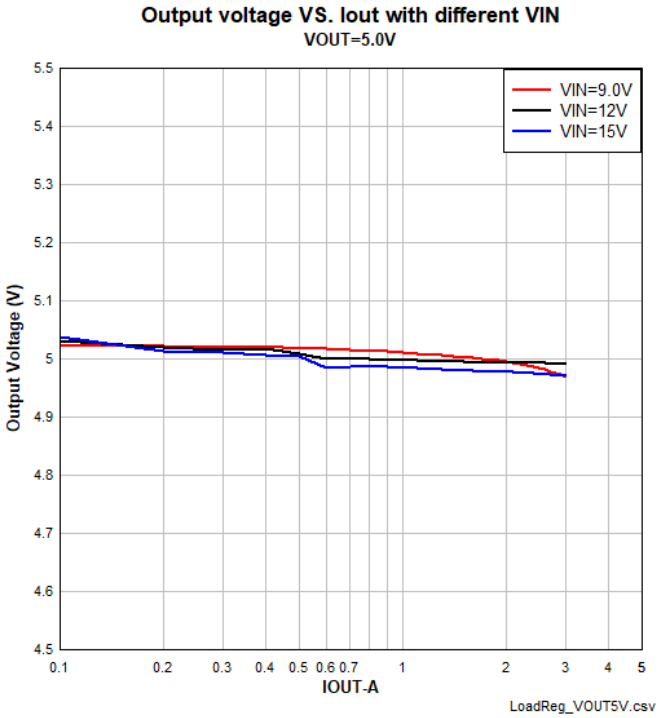


Figure 6. VOUT=5V, Regulation, L=2.2μH

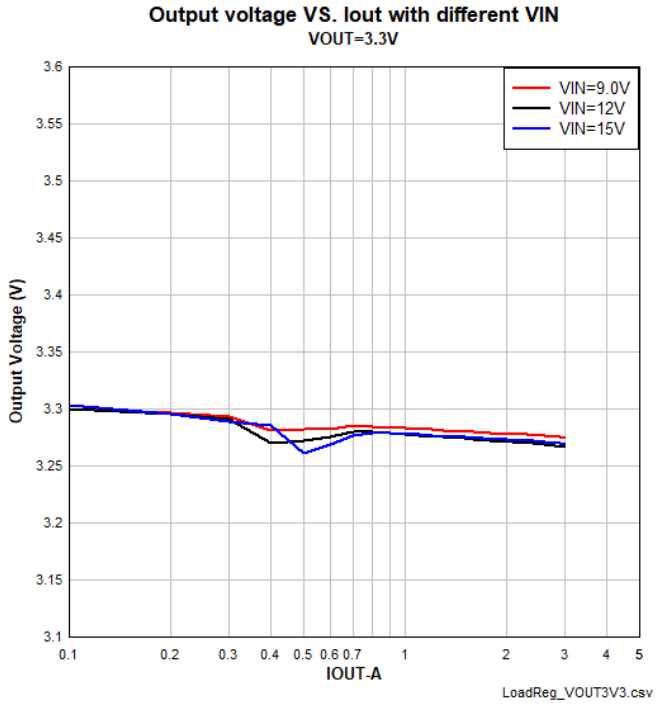


Figure 7. VOUT=3.3V, Regulation, L=2.2μH

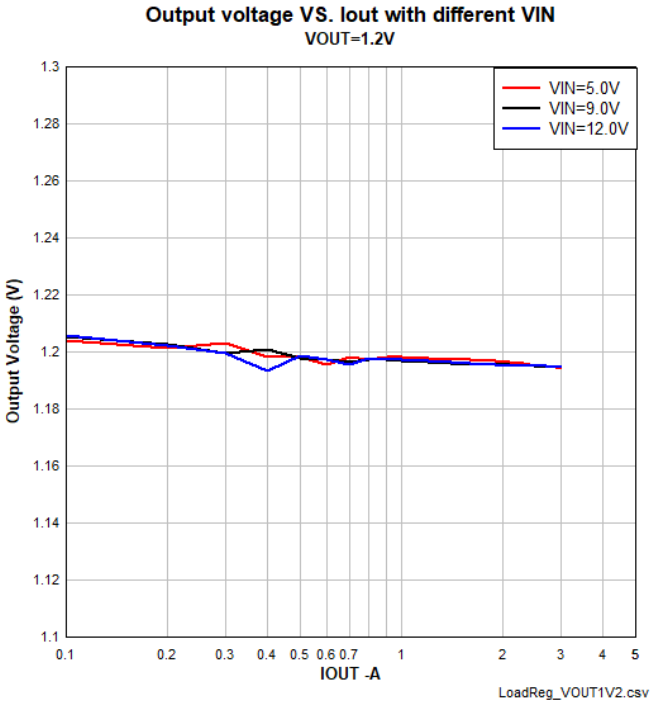
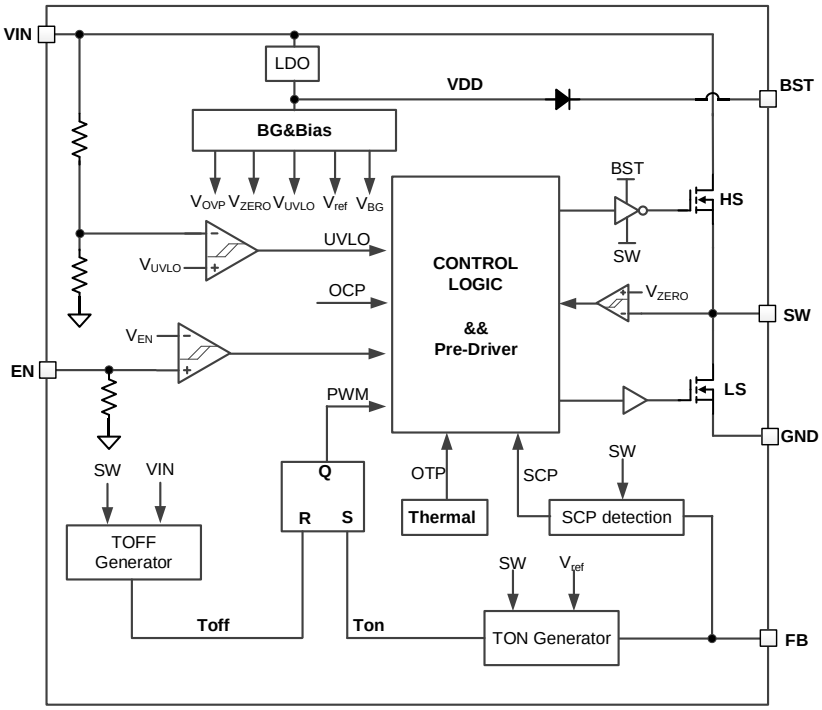


Figure 8. VOUT=1.2V, Regulation, L=1μH

Functional Block Diagram



Detailed Description

Overview

The LP6451 is a 3A synchronous buck converter, supporting 4.2-18V input voltage range. The adaptive COT control scheme enables fast transient respond and minimizes the output capacitance. The LP6451 supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP6451 automatically transfers between PFM and PWM according to the output current.

Under Voltage Lockout (UVLO)

When the input voltage VIN is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP6451 can be enabled by the EN pin.

EN Control

The EN pin can be used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP6451 enables all the internal circuits, delays for 260us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1000kΩ pull-down resistor to ground.

Soft-start

The LP6451 integrates soft-start function with a typical time of 0.75ms(t_{ss}). After passing the UVLO threshold and enabled by the EN pin with the 500us delay(t_d), the internal reference voltage ramps from zero to the Vref in 0.75-ms and the output voltage ramps up accordingly.

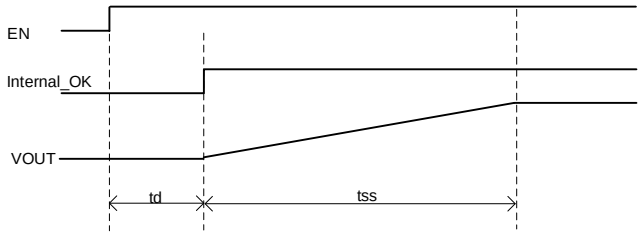


Figure 9. Soft Start Sequence

Constant-ON Time (COT) Control Scheme

The LP6451 integrates the COT control scheme for pseudo-fixed- frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal on-time (TON) generator block monitors the FB-pin voltage and turns on the high-side MOSFET to start a switching cycle, when the FB-pin voltage drops to an internal reference voltage Vref. Then the internal circuits start to calculate the on-time of the high-side MOSFET, which is proportional to the input voltage and inversely proportional to the output voltage. Once the on-time is finished, the TOFF generator turns off the high-side MOSFET and turns on the low-side MOSFET.

PFM Operation

The LP6451 is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

Bootstrap Capacitor

The LP6451 integrates two N-MOSFET to achieve high efficiency. The high-side MOSFET is powered by the bootstrap capacitor CBST, which is between the BST pin and SW pin.

Over Current Protection and Short Circuit Protection

The LP6451 protects an over current situation by limiting the inductor valley current. The current of low-side MOSFET is monitored all the time to sense the inductor valley current when the LP6451 is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit pluses a half of the inductor ripple current.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to 50% of the Vref for 1.5-ms, the LP6451 shuts down. The LP6451 will restart after at least 500-us waiting time. If the SCP condition still holds after soft-start, the LP6451 shutdown again, repeating the operation described above.

When the over current condition is removed, the output voltage returns to normal operation.

Thermal Protection

The LP6451 has a thermal protection function. The device will shut down when the internal temperature is higher than 160°C and will restart after the temperature drops below 135°C.

Application Information

Design Requirements

The table 1 shoes the design parameters for a typical 5V output voltage in the IPC application.

Table 1 Design Parameters

Parameter	Target
Input voltage range	9~15V
Output voltage	5V
Transient ripple	±200mV
Operating frequency	1200kHz

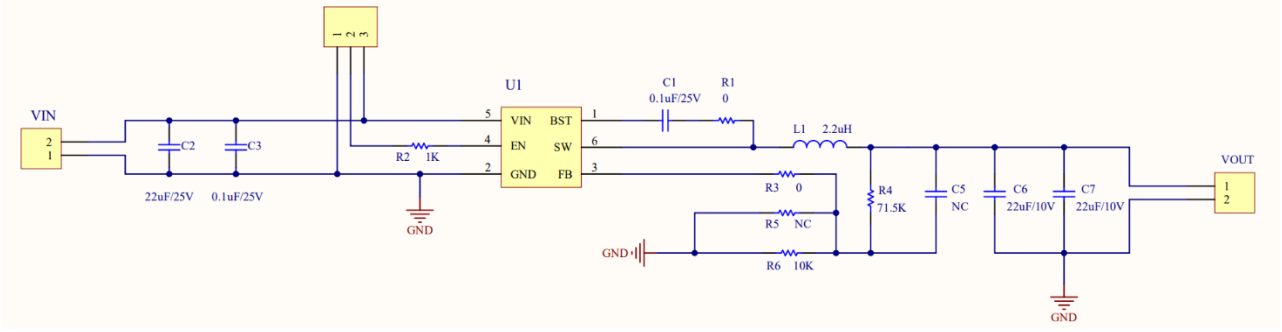


Figure 10. Typical schematic

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1\right) * V_{ref}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V.

For better accuracy, the R_{DOWN} is recommended to be lower than 100kΩ to ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current.

For a 3.3V-output application, a 10kΩ R_{DOWN} is selected and the R_{UP} is 45kΩ.

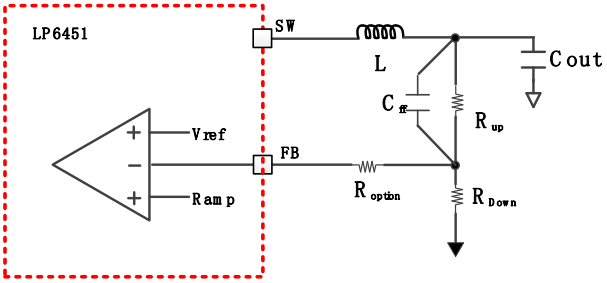


Figure 11. FB resistor divider setting

EN Design

The high precision EN pin logic high threshold allows the user to design a precise VIN voltage to enable the converter during power on. The startup sequence can be designed by adjusting the resistor divider of R_{UP_EN} and R_{DOWN_EN} with

the equation below,

$$V_{EN} = \frac{900k\Omega // R_{DOWN\_EN}}{R_{UP\_EN} + 900k\Omega // R_{DOWN\_EN}} * VIN$$

where VEN is the input voltage at which the converter is enabled.
The internal 1.2V is used as the reference, when the voltage on EN pin rising above 1.2V, a enable signal will be send to the internal logic circuit to wake up all the control circuits.
A 47pF-1nF capacitor is recommend to be soldered to avoid the high-frequency noise influence from the switching node.

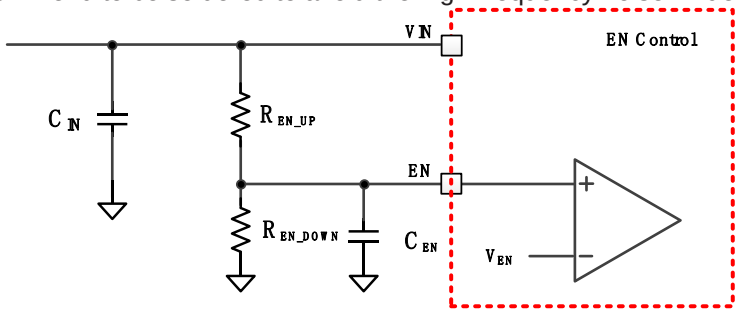


Figure 12. EN resistor divider setting

Inductor and Output Capacitor Setting

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * Fsw} * \frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.
For a typical 12V input voltage and 5.1V output voltage, a low DCR value, 2.2-μH inductor is recommended.
The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor CFF can be selected to improve the transient behavior. The typical capacitance can be 10-100pF. For this design, three 6.3V, X5R, 22μF capacitors (GRM188R60J226ME15) from Murata are soldered at the VOUT to GND.

Table 2 Recommend R/L/C values

Vout	Inductor-L	Cout	R_{UP}	R_{DOWN}	R_{option}	C_{ff}
1.2V	1μH/1.2μH	22μF*2	10 kΩ	10 kΩ	0 Ω	NA
3.3V	1.5μH/2.2μH	22μF*2	45 kΩ	10 kΩ	10 kΩ	10-100pF
5.0V	2.2μH/3.3μH	22μF*3	73.3 kΩ	10 kΩ	10 kΩ	10-100pF

Bootstrap capacitor

A 0.1-μF ceramic capacitor is needed to supply power for the high-side N-MOSFET driver. The capacitor should be at least 10V.

Input capacitor

A typical 22-μF ceramic capacitor is needed to serve as the bulk capacitor at the VIN pin of the LP6451. An additional 0.1μF is strongly recommended to provide additional high frequency filtering and should be placed to the VIN pin and GND as close as possible.

Application Waveforms (Vin=12V,L=2.2μH, Cout=22μF*3)

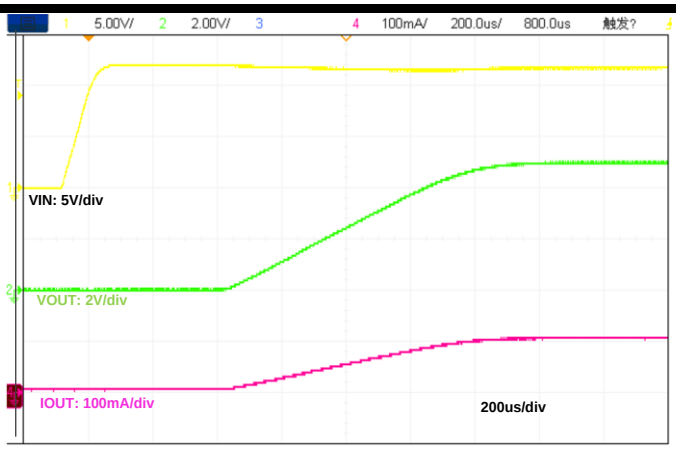


Figure 13. Startup by VIN, 50Ω load

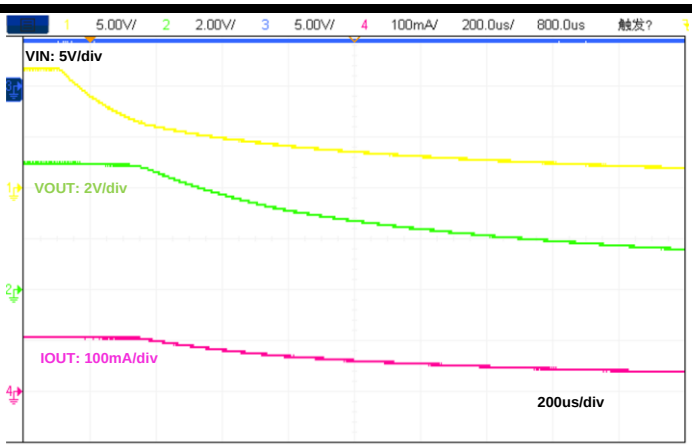


Figure 14. Shutdown by VIN, 50Ω load

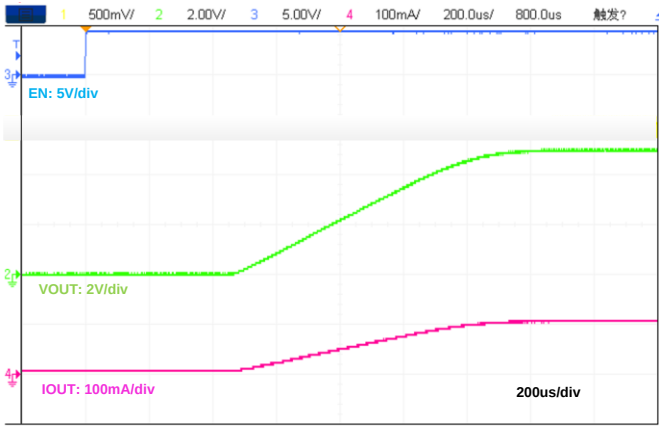


Figure 15. Startup by EN, 50Ω load

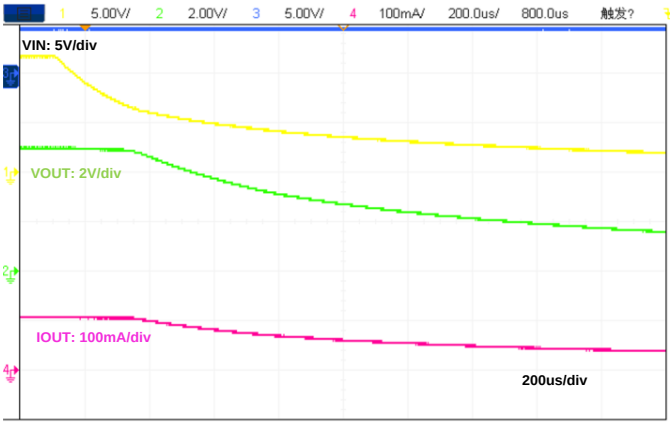


Figure 16. Shutdown by EN, 50Ω load

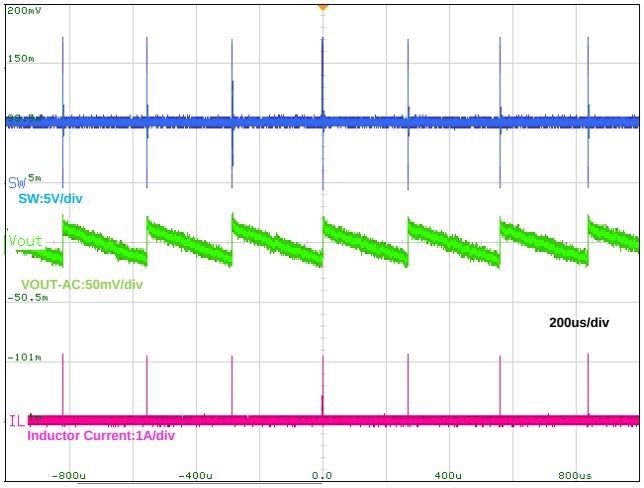


Figure 17. Switching Waveform, 0A load

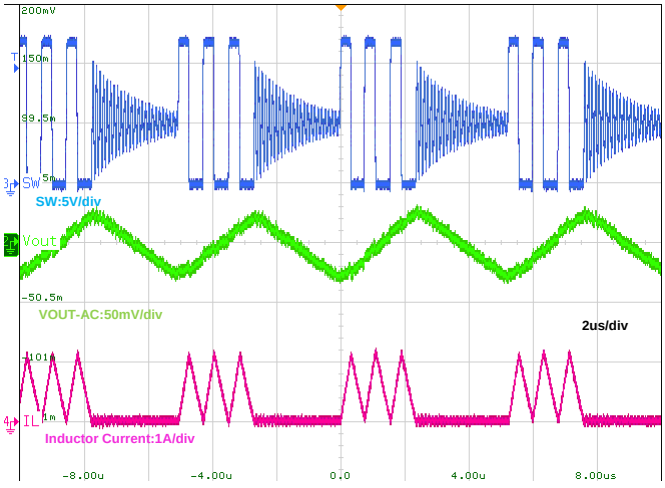


Figure 18. Switching Waveform, 250mA load

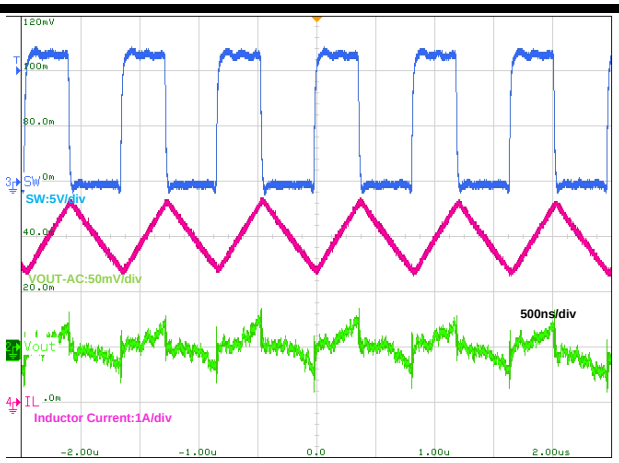


Figure 19. Switching Waveform, 3A load

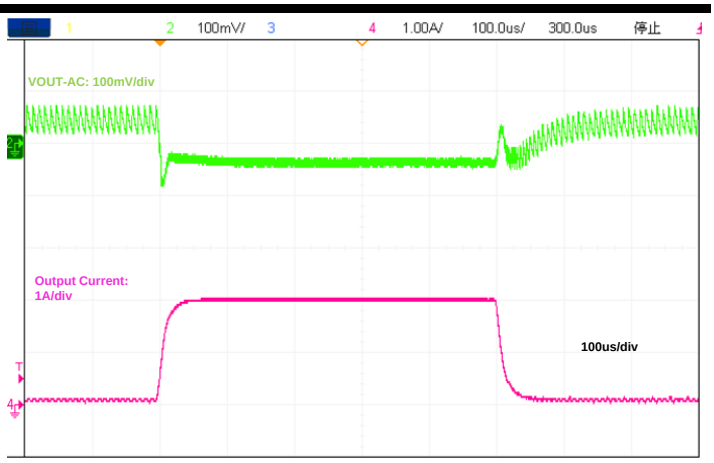


Figure 20. Load Transient, 0.1A-2A-0.1A

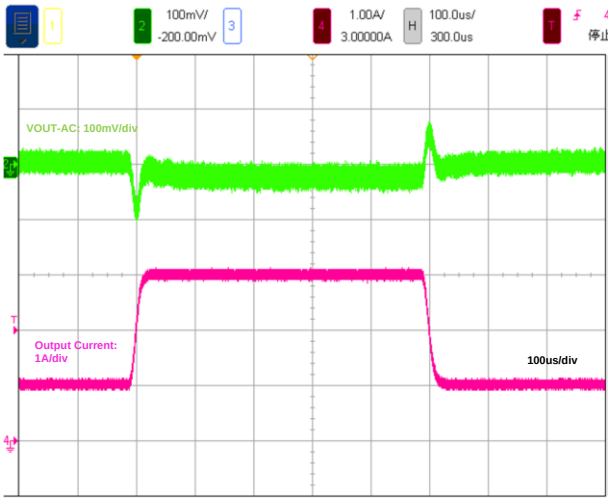


Figure 21. Load Transient, 1A-3A-1A

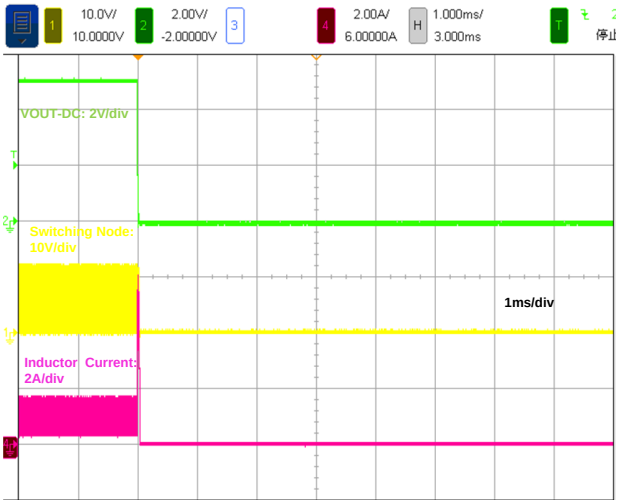


Figure 22. Output SCP, VIN=12V, VOUT=5V

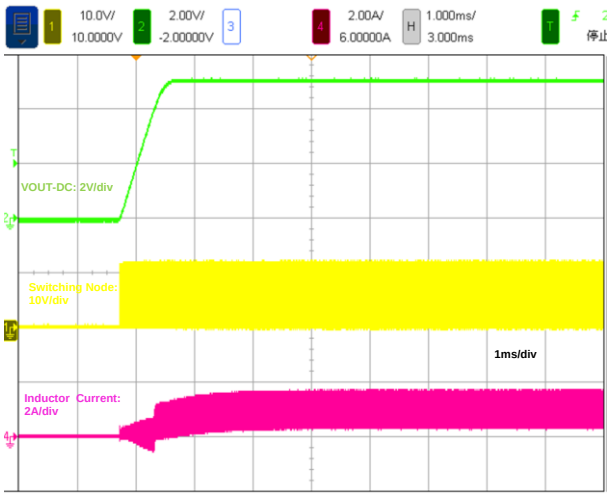


Figure 23. SCP Recovery, VIN=12V, VOUT=5V

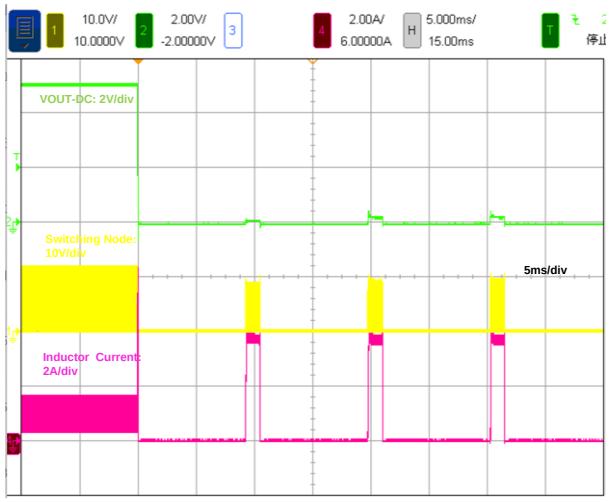
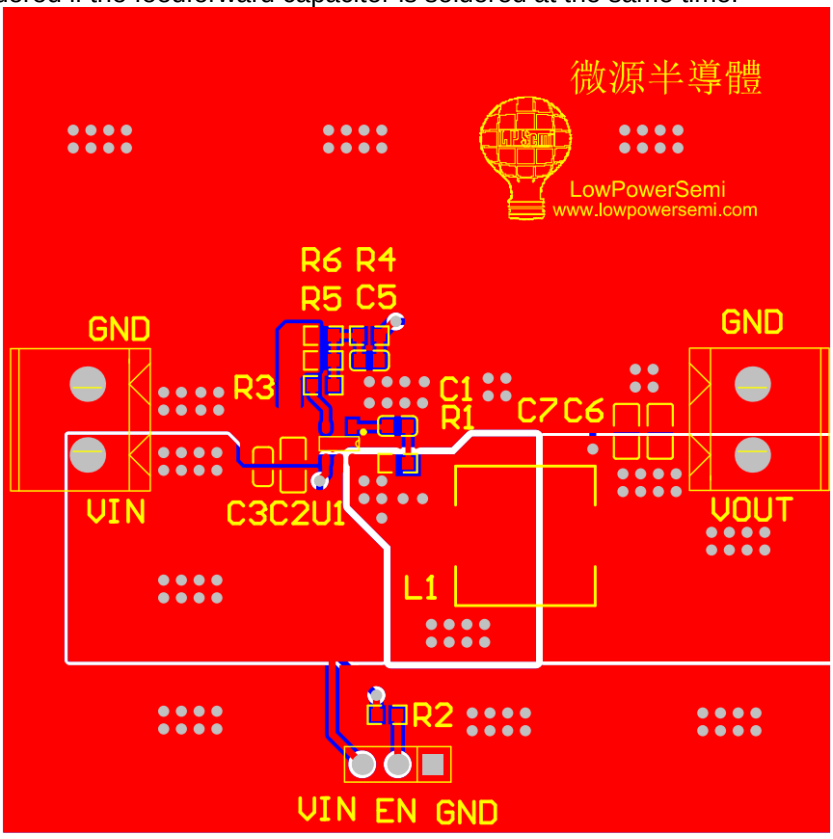


Figure 24. Output SCP, VIN=12V, VOUT=5V

PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

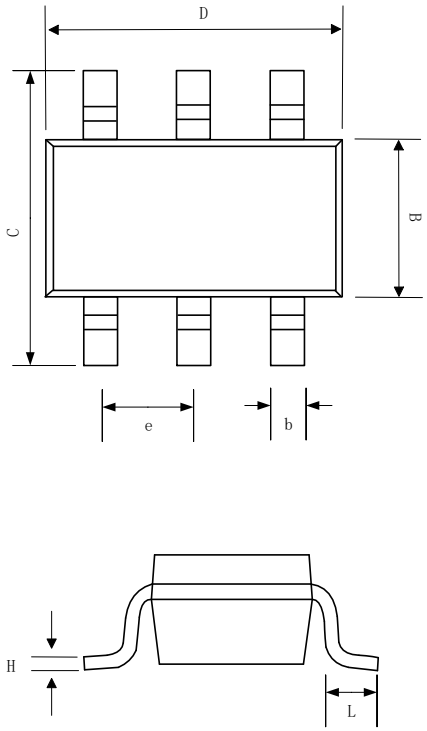
- Place input capacitor (C2) as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- R1 is reserved to slow down the switching speed for noise sensitive applications and R3 with higher than 1kΩ resistor should be soldered if the feedforward capacitor is soldered at the same time.

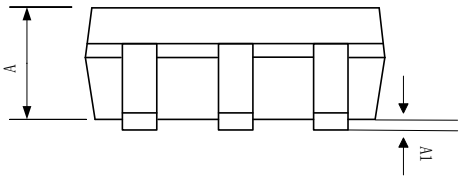


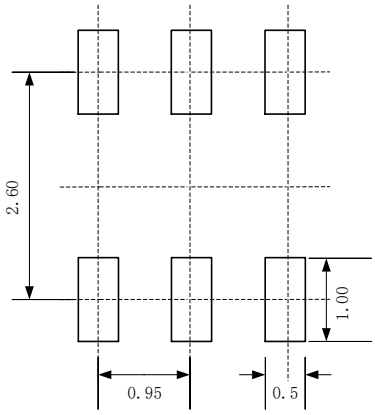
- **Figure 25 Layout example**

Packaging Information

1.6x2.9 SOT23-6 package







Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

Revision History

Revision	Date	Change Description
Rev 1p0	11/10/2021	Product Release
Rev 1p1	9/1/2022	Add SW transient specification
Rev 1p2	12/30/2022	New format update