Programmable Gamma and VCOM Buffers

General Description

The LP6299 providers a 14-channel programmable gamma buffer and a programmable VCOM buffer for applications in TFT-LCD Panel. Each of the 14-channel gamma buffers is generated using a 10-bit resolution digital-to-analog converter together with a buffer through IIC control. The 14-channel gamma buffer support dynamic switching between two gamma curves by selecting BANK select pin.

The LP6299 also features a programmable operational amplifier that drives the LCD VCOM. This unity-gain buffer is capable of rail-to-rail input and output, fast slew rate, and ±150mA output short-circuit current. The VCOM buffer voltage is IIC programmed using 7-bit resolution.

The LP6299 includes EEPROM to store two gamma codes and VCOM codes, and control it through IIC interface at the real time.

The LP6299 is available in a space saving QFN32 (0.5mm pitch) package.

Features

- IIC Interface Control
- Input Supply Voltage Range
  - 2.3V to 3.6V Logic Supply Range
  - 6.5V to 18V Analog Supply Range
- 14-Channel Programmable Gamma Buffers
  - 10-Bit, 1024-Step Resolution
  - ±100mA Output Short Circuit
  - 10V/μs Slew Rate
  - Two Bank Select
- 1-Channel Programmable VCOM Buffer
  - 7-Bits, 128-Step Current Output
  - ±150mA Output Short Circuit
  - 20V/μs Slew Rate
- Integrated EEPROM
- Available in QFN-32 (5 mm×5mm)
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT LCD Panels

Order Information

LP6299 □□□

- F: Pb-Free
- Package Type
  - QV: QFN-32

Marking Information

Device	Marking	Package	Shipping
LP6299	LPS LP6299 YWXXX	QFN-32	3K/REEL
Y: Year code. **W**: Week code. **XXX**: Batch number.			

Typical Application Circuit

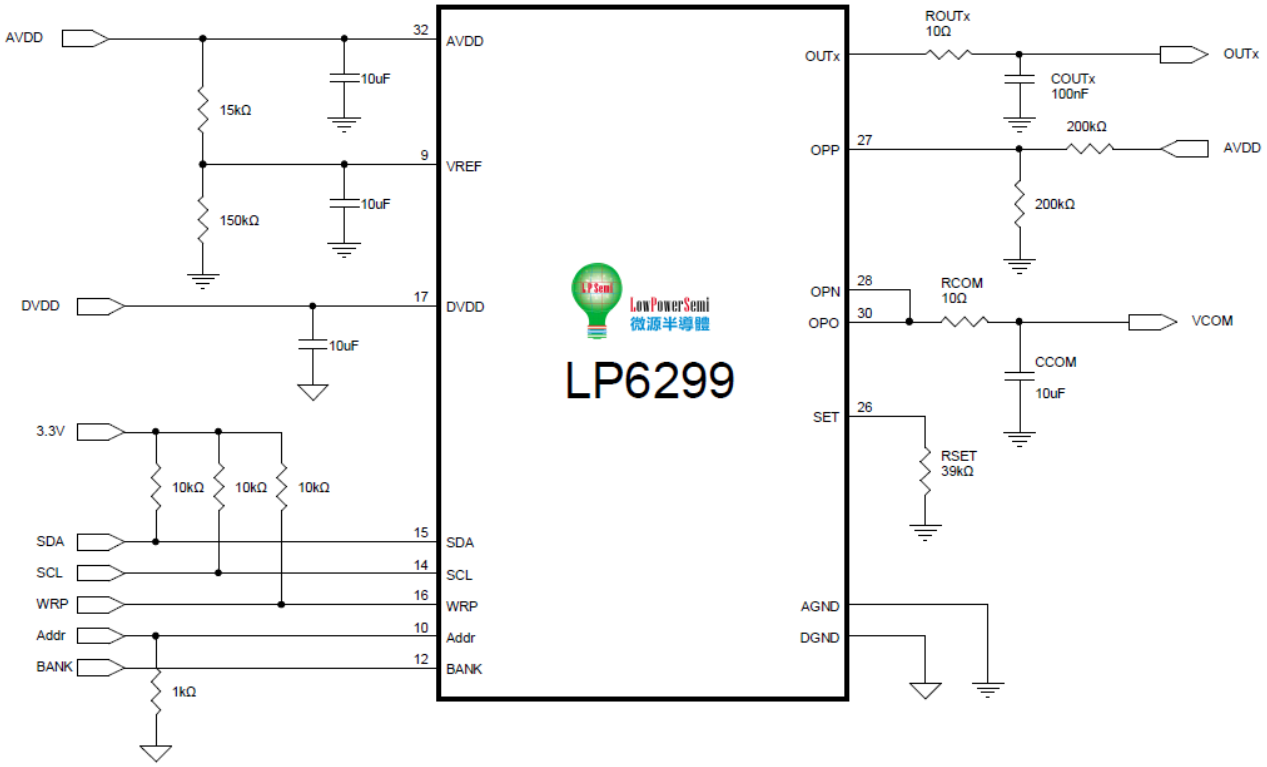


Figure 1. Typical Application Circuit

Pin Configuration

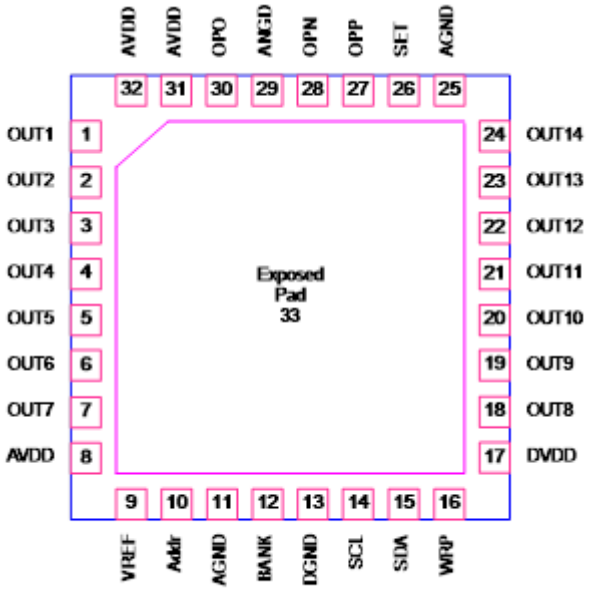


Figure 2. QFN-32 Package (5mm x 5mm)

Function Block Diagram

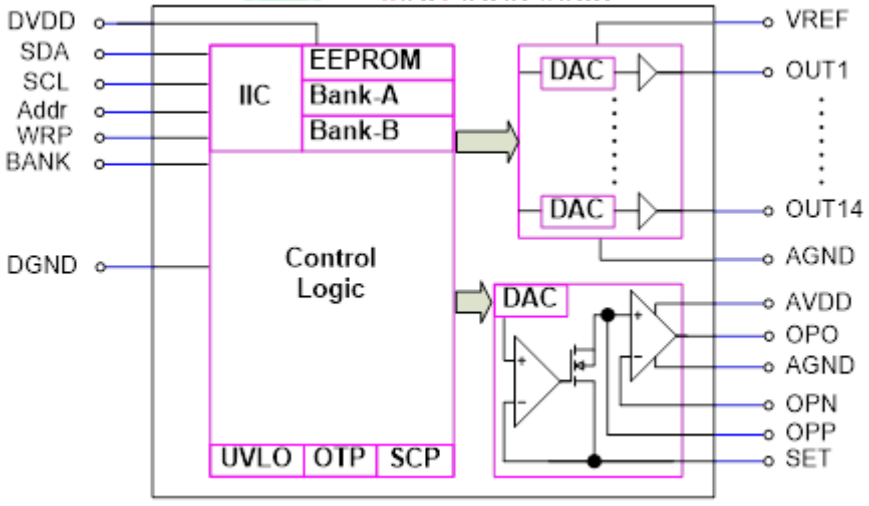


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	OUT1	Gamma Buffer Output.
2	OUT2	Gamma Buffer Output.
3	OUT3	Gamma Buffer Output.
4	OUT4	Gamma Buffer Output.
5	OUT5	Gamma Buffer Output.
6	OUT6	Gamma Buffer Output.
7	OUT7	Gamma Buffer Output.
8	AVDD	Analog Power Supply Input. Bypass AVDD to AGND with 10μF capacitor
9	VREF	Reference Input Voltage for Gamma Reference Voltage
10	Addr	IIC interface Device Address Bit0. Addr = L: IIC slave address is 0x74H. Addr = H: IIC slave address is 0x75H.
11	AGND	Analog Ground.
12	BANK	Bank Selection. BANK=L: BANK A. BANK=H: BANK B
13	DGND	Digital Ground.
14	SCL	IIC interface clock signal.
15	SDA	IIC interface data signal.
16	WRP	EEPROM Write Protection. WRP=L: Write/Read Enable. WRP=H: Write/Read Disable
17	DVDD	Digital Power Supply Input. Bypass DVDD to DGND with 10μF capacitor
18	OUT8	Gamma Buffer Output
19	OUT9	Gamma Buffer Output
20	OUT10	Gamma Buffer Output
21	OUT11	Gamma Buffer Output
22	OUT12	Gamma Buffer Output
23	OUT13	Gamma Buffer Output
24	OUT14	Gamma Buffer Output
25	AGND	Analog Ground.
26	SET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from SET pin to AGND to set the sink current
27	OPP	VCOM Amplifier Positive Input
28	OPN	VCOM Amplifier Negative Input
29	AGND	Analog Ground.
30	OPO	VCOM Amplifier Output
31	AVDD	Analog Power Supply Input. Bypass AVDD to AGND with 10μF capacitor
32	AVDD	Analog Power Supply Input. Bypass AVDD to AGND with 10μF capacitor
33	EP	Exposed Pad. Connect this pin to AGND.

Absolute Maximum Ratings Note 1

- ✧ AVDD to AGND ---------- −0.3V to +20V
- ✧ DVDD to DGND ---------- −0.3V to +7V
- ✧ SDA, SCL, WRP, BANK, Addr to DGND ---------- −0.3V to DVDD+0.3V
- ✧ VREF, OPP, OPN, OPO to AGND ---------- −0.3V to AVDD +0.3V
- ✧ OUT1~OUT14, SET to AGND ---------- −0.3V to AVDD +0.3V
- ✧ AGND to DGND ---------- −0.3V to +0.3V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40°C to +150°C
- ✧ Operation Ambient Temperature Range (T_A) ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1 Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. The functional operation of the device or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  QFN-325x5, θ_{JA} ---------- 41°C/W

  QFN-325x5, θ_{JC} ---------- 14°C/W

Electrical Characteristics

(V_{DVDD}=3.3V, V_{AVDD}=16.5V, V_{REF}=16V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
DVDD Input Supply Voltage	V_{DVDD}		2.3	--	3.6	V
DVDD UVLO Threshold	V_{UVLO}		--	--	2.2	V
DVDD Supply Current	I_{DQ}		--	0.75	1.5	mA
AVDD Input Supply Voltage	V_{AVDD}		6.5	--	18	V
AVDD Supply Current	I_{AQ}		--	10	15	mA
REF Input Voltage	V_{REF}		AVDD -4	--	AVDD	V
Thermal Shutdown Threshold	T_{SD}	Junction Temperature Rising	--	150	--	°C
Digital Input (WRP, Addr, Bank)						
Input Threshold Voltage	V_{IH}	Logic High.	0.8* DVDD	--	--	V
	V_{IL}	Logic Low	--	--	0.2* DVDD	
Input Current	I_{DIN}		-40	--	+40	nA
Gamma Buffers (OUT1~OUT14)						
OUTx Resolution			--	10	---	Bits
OUTx Integral Nonlinearity Error	INL_{OUTx}		-4	--	+4	LSB
OUTx Differential Nonlinearity Error	DNL_{OUTx}		-1	--	+1	LSB
OUTx Full Scale Error	$OUTx_{FSE}$	V_{AVDD}=16.5V	-4	--	+4	LSB
OUTx Swing	V_{GOH}	V_{AVDD}=16.5V , V_{REF}=16.2V, Code=1013, I_{OUTx}=5mA	$V_{(1013)}$ -30	$V_{(1013)}$ -10	--	mV
		V_{AVDD}=16.5V , V_{REF}=16.2V, Code=512, I_{OUTx}=50mA	$V_{(512)}$ -100	$V_{(512)}$ -50	--	
	V_{GOL}	V_{AVDD}=16.5V , V_{REF}=16.2V, Code=512, I_{OUTx}=-50mA	--	$V_{(512)}$ -50	$V_{(512)}$ +100	
		V_{AVDD}=16.5V , V_{REF}=16.2V, Code=10, I_{OUTx}=-5mA	--	$V_{(10)}$ +10	$V_{(10)}$ +30	
OUTx Short Circuit Current	I_{Short_OUTx}		--	±100	--	mA
Load Regulation	LR_{OUTx}	Code=512, I_{OUTx}=±50mA	--	±0.5	±1.5	V/A
Slew Rate	SR_{OUTx}		10	20	--	V/us
Settling Time	ts_{OUTx}		--	5	--	us
Electrically-Erasable Programmable ROM (EEPROM)						
Byte Write Time	t_{BYTE}		--	--	10	ms
Byte Read Access Time	B_{RT}		--	200	--	ns
Programmable Times			--	1000	--	Cycle

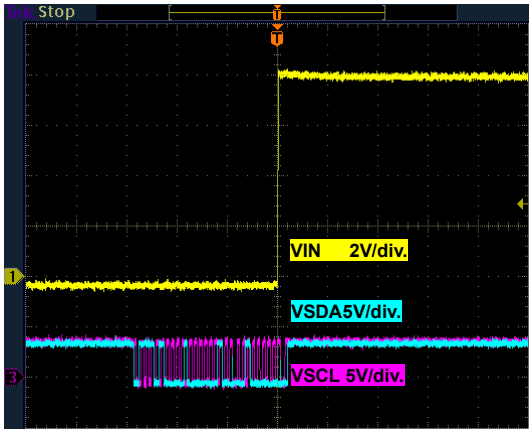
Electrical Characteristics (Continued)

(V_{DVDD}=3.3V, V_{AVDD}= 16.5V, V_{REF}=16V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCOM Buffer (VCOM)						
VCOM Resolution			--	7	--	Bits
VCOM Integral Nonlinearity Error	INL		-4	--	+4	LSB
VCOM Differential Nonlinearity Error	DNL		-1	--	+1	LSB
AVDD to SET Ration	V_{AVDD}/V_{SET}		--	20	--	V/V
SET Current	I_{SET}	Through SET	--	--	120	uA
SET Zero Scale Error	SET_{ZSE}		-1	+1	+2	LSB
SET Full Scale Error	SET_{FSE}		-4	--	+4	LSB
Output Swing	V_{OH}	V_{COM}=AVDD/2, I_{COM}=50mA	AVDD/2 -100	AVDD/2 -50	--	mV
	V_{OL}	V_{COM}=AVDD/2, I_{COM}=-50mA	--	AVDD/2 +50	AVDD/2 +100	mV
Short Circuit Current	I_{Short_OP}		--	±150	--	mA
Load Regulation	LR_{VCOM}		--	±0.5	±1.0	V/A
Slew Rate	SR_{VCOM}		20	25	--	V/us
Settling Time	ts_{VCOM}		--	5	--	us
IIC Timer Characteristics						
Input High Voltage Level	V_{IH}		1.4	--	--	V
Input Low Voltage Level	V_{IL}		--	--	0.4	V
Serial Clock Frequency	F_{SCL}		0	--	1	MHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3	--	--	us
Hold Time (Repeated) START Condition	$t_{HD, DAT}$		0.6	--	--	us
SCL Pulse-Width Low	t_{LOW}		1.3	--	--	us
SCL Pulse-Width High	t_{HIGH}		0.6	--	--	us
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6	--	--	us
Data Hold Time	$t_{HD, DAT}$		--		800	ns
Data Setup Time	$t_{SU, DAT}$		100	--	--	ns
SDA and SCL Receiving Rise / Fall Time	$t_{R,tF}$		20+0.1 CB	--	300	ns
SDA Transmitting Fall Time	t_{FF}		20+0.1 CB	--	250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6	--	--	us
Pulse Width of Suppressed Spike	t_{SP}		--	--	50	ns

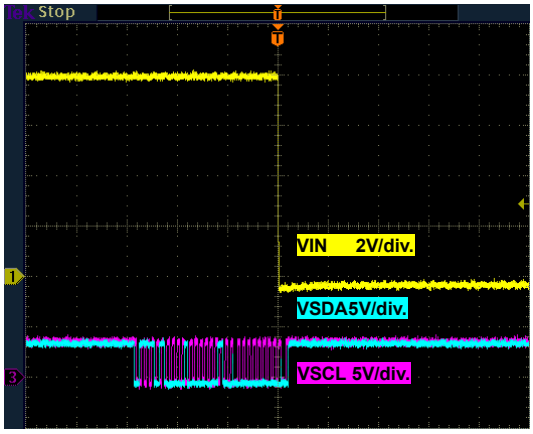
Typical Performance Curves

T_A=+25°C, V_{DVDD}=3.3V, V_{AVDD}= 16.5V, V_{REF}=16V, unless otherwise specified.



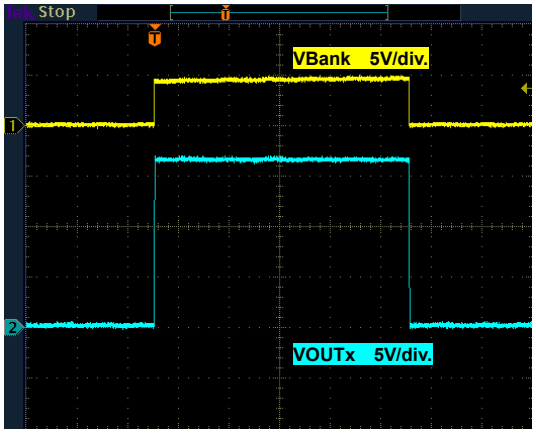
100us/div.

Figure 4.GAMMA Program Output (0V→8V)



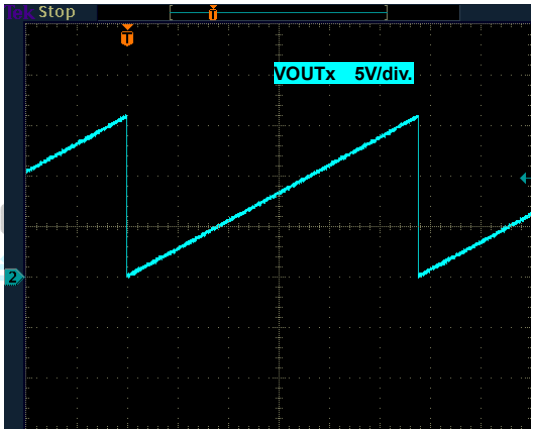
100us/div.

Figure 5.GAMMA Program Output (8V→0V)



20ms/div.

Figure 6.BANK Switching Settling Time for GAMMA



200ms/div.

Figure 7.Gamma Program Output

Typical Performance Curves (Continued)

T_A=+25°C, V_{DVDD}=3.3V, V_{AVDD}= 16.5V, V_{REF}=16V, unless otherwise specified.

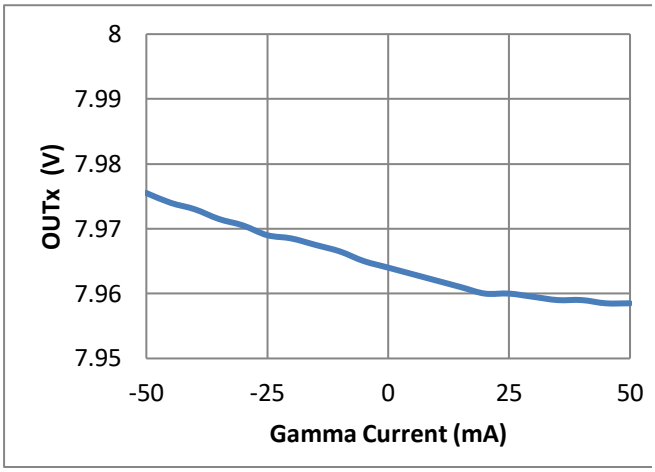


Figure 8.GAMMA Load Regulation
CODE = 512

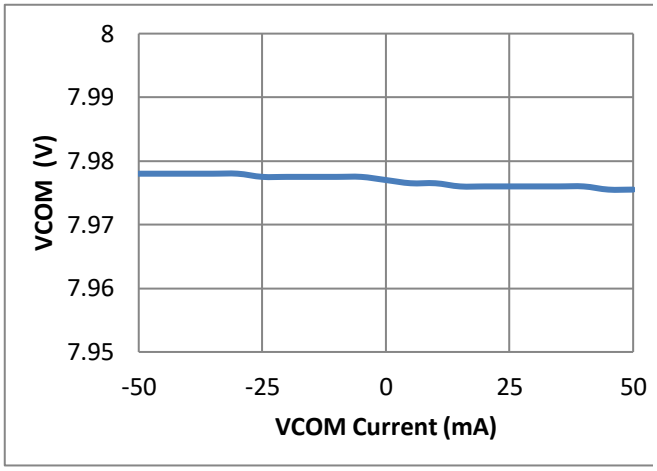


Figure 9.VCOM Load Regulation
CODE = 64

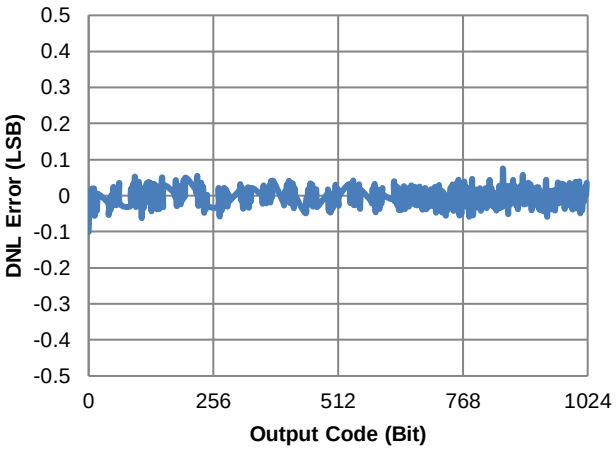


Figure 10.GAMMA DNL

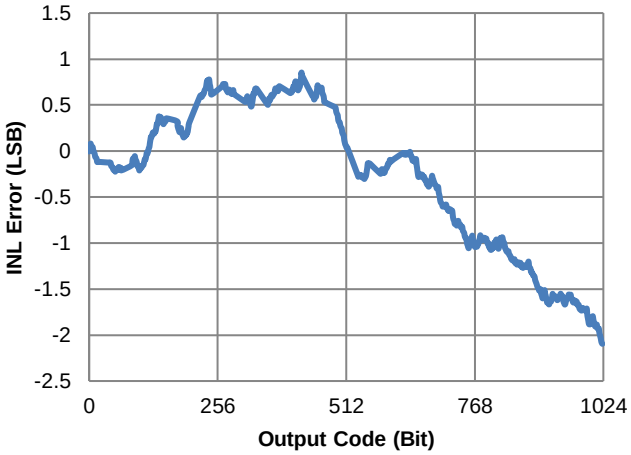


Figure 11.GAMMA INL

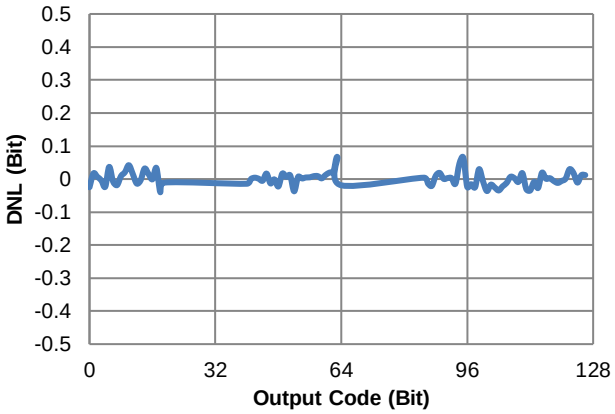


Figure 12.VCOM DNL

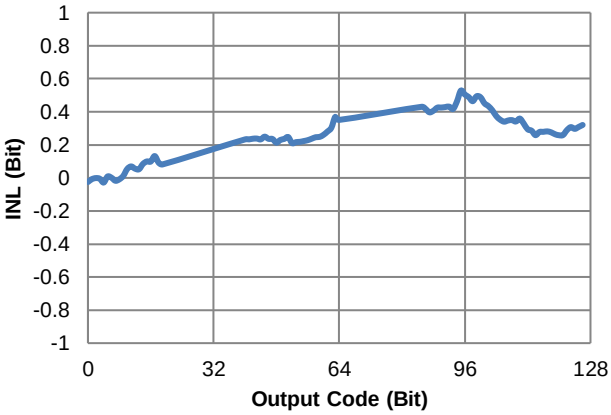


Figure 13. VCOM INL

Power On/ Off Sequence

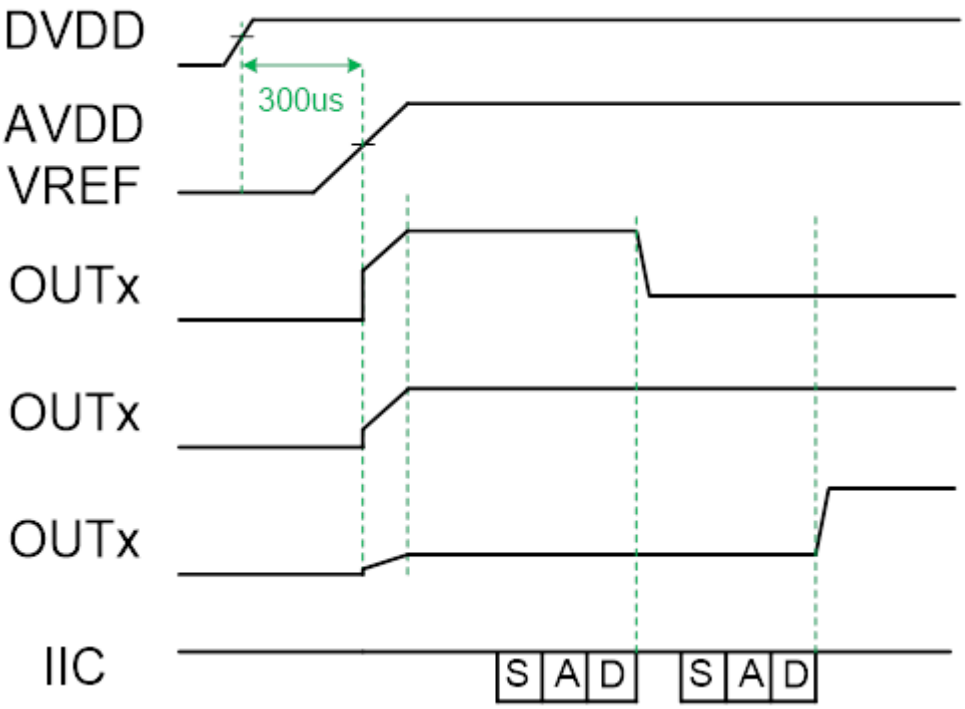


Figure 14. Power Sequence and GPM Control

Application Information

The LP6299 integrates 14 channels of programmable gamma buffers, and a programmable operational amplifier that drives the LCD VCOM. LP6299 include two register banks can store two different sets. The device uses IIC interface for setting such as output voltages, programming gamma and VCOM codes into EEPROM.

Under Voltage Lockout (UVLO)

The LP6299 has an UVLO internal circuit that enabling the device once the voltage on the DVDD voltage exceeds the UVLO threshold voltage.

Bank Select

The LP6299 have two register banks. User can program one gamma set save into Bank A, the other gamma set save into Bank B, and select it by BANK pin.

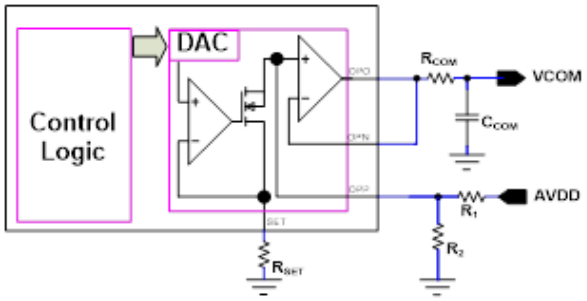
Gamma Buffer Output Setting

The 14 channel gamma voltage generators also include EEPROM to preserve the all programmed reference voltages by loading the nominal values from the EEPROM to the corresponding DAC when the device is powered. During device operation, each channel can be individually programmed by writing only to the corresponding DAC without transferring the programmed data to the EEPROM.
Gamma Buffer Output Value determined by the Ref. Voltage and the decimal value of the binary code. The Value is calculated using below Equation.

$$V_{GAMMAx} = V_{REF} \times \frac{CODE}{1024}$$

In this case, the programmed voltages will not be retained when the device is powered down. Upon power up the DACs will be loaded with the default values that were already stored in the EEPROM. Note that the programmed DAC values can be transferred to the EEPROM via writing the appropriate command to the control register. When the DAC values are transferred to the EEPROM, the programmed gamma reference voltages will be preserved when the device is powered OFF, and retained when the device is powered back ON.

Set RSET Resistor



The Device also provides the ability to reduce the flicker of an LCD Panel by adjustment of the VCOM voltage during production test and alignment. A 128-Step resolution is provide under digital control. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current. The adjustment of the output is provided by the IIC interface.

$$I_{SET} = \frac{CODE+1}{128} \times \frac{V_{AVDD}}{20 \times R_{SET}}$$

$$V_{OUT} = V_{AVDD} \times \frac{R_2}{R_2+R_1} \times \left(1 - \left(\frac{CODE}{128} \times \frac{R_1}{20 \times R_{SET}}\right)\right)$$

EEPROM Write/Read Protection

The WRP pin control the EEPROM can write or read to register by IIC interface. The WRP pin change to Low level can be write data into EEPROM from register or read data from EEPROM to register by IIC interface. If WRP is High level and IIC write/read command will be save into control byte of the register but not happened write/read event.

Over Temperature Protection

The LP6299 device enters over temperature protection if its junction temperature exceeds 150°C (TYP.). During over temperature protection none of the device's functions are available. The protection will base on the control byte (R[00h] bit6). When the R[00h] bit6 is high, the thermal sensor will disable.

Application Information (Continued)

1. IIC Interface Specification

The LP6299 can easily modify parameters by IIC bus, that slave address is show below:

Slave Address							
D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**W/R**
1	1	1	0	1	0	**Addr**	**0/1**

IIC is a two wire serial interface developed, the bus consists of a clock line (SCL) and a data line (SDA) with pull-up structures. The LP6299 works as a slave mode, and address can set by Addr pin. The data transfer protocol follows IIC-Bus Specification's standard mode (100kbps) and fast mode (400kbps).

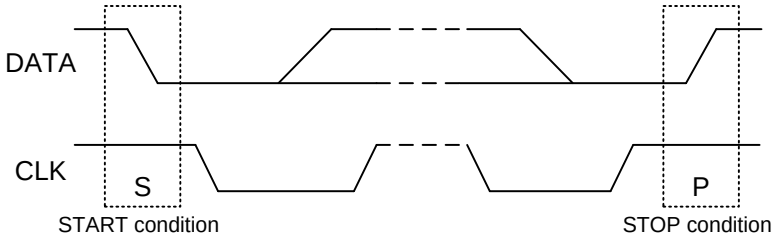


Figure 15. START and STOP Conditions

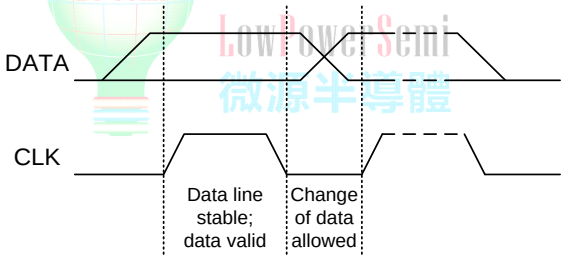


Figure 16. Bit Transfer on the Serial Interface

2. Write Data to Register

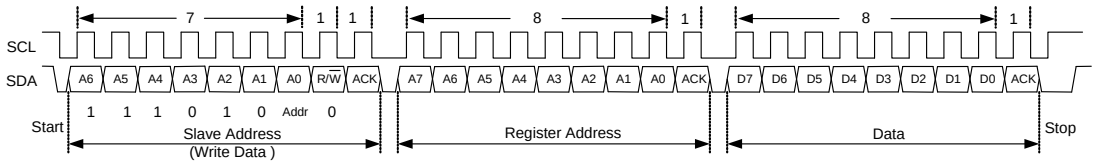


Figure 17.Write Single Byte Data to Register

3. Read Data to Register

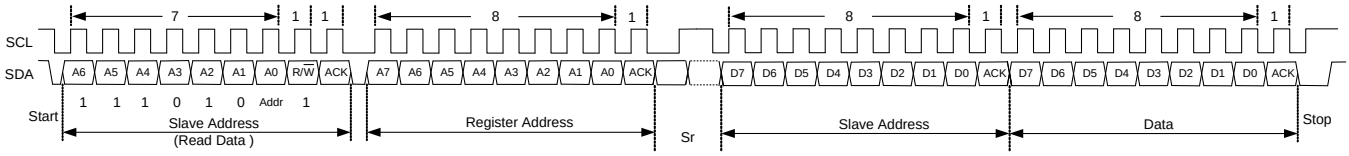


Figure 18.Read Single Byte Data from Register

Application Information (Continued)

4. IIC REGISTER MAP

The lowest bit number (0) represents the least bit, the highest bit number (7) represents the most bit, and R/W indicates whether the bit is read only (R), write only (W), or both read and write (R/W).

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	BANK	Preset EEPROM	NOTE
0x00		HOT_EN		LD_ROM	WR_ROM		OUT_EN			02h	CONTROL
0x01	DVR[6:0]									80h	DVR_VCOM
0x02	GA1[9:4]								A	20h	Gamma1 Gamma2
0x03	GA1[3:0]						GA2[9:8]			02h	
0x04	GA2[7:0]									00h	
0x05	GA3[9:4]									20h	Gamma3 Gamma4
0x06	GA3[3:0]						GA4[9:8]			02h	
0x07	GA4[7:0]									00h	
0x08	G5[9:4]									20h	Gamma5 Gamma6
0x09	GA5[3:0]						GA6[9:8]			02h	
0x0A	GA6[7:0]									00h	
0x0B	GA7[9:4]									20h	Gamma7 Gamma8
0x0C	GA7[3:0]						GA8[9:8]			02h	
0x0D	GA8[7:0]									00h	
0x0E	GA9[9:4]									20h	Gamma9 Gamma10
0x0F	GA9[3:0]						GA10[9:8]			02h	
0x10	GA10[7:0]									00h	
0x11	GA11[9:4]									20h	Gamma11 Gamma12
0x12	GA11[3:0]						GA12[9:8]			02h	
0x13	GA12[7:0]									00h	
0x14	GA13[9:4]									20h	Gamma13 Gamma14
0x15	GA13[3:0]						G14[9:8]			02h	
0x16	GA14[7:0]									00h	
0x25	GB1[9:4]								B	20h	Gamma1 Gamma2
0x26	GB1[3:0]						GB2[9:8]			02h	
0x27	GB2[7:0]									00h	
0x28	GB3[9:4]									20h	Gamma3 Gamma4
0x29	GB3[3:0]						GB4[9:8]			02h	
0x2A	GB4[7:0]									00h	
0x2B	GB5[9:4]									20h	Gamma5 Gamma6
0x2C	GB5[3:0]						GB6[9:8]			02h	
0x2D	GB6[7:0]									00h	
0x2E	GB7[9:4]									20h	Gamma7 Gamma8
0x2F	GB7[3:0]						GB8[9:8]			02h	
0x30	GB8[7:0]									00h	
0x31	GB9[9:4]									20h	Gamma9 Gamma10
0x32	GB9[3:0]						GB10[9:8]			02h	
0x33	GB10[7:0]									00h	
0x34	GB11[9:4]									20h	Gamma11 Gamma12
0x35	GB11[3:0]						GB12[9:8]			02h	
0x36	GB12[7:0]									00h	
0x37	GB13[9:4]									20h	Gamma13 Gamma14
0x38	GB13[3:0]						GB14[9:8]			02h	
0x39	GB14[7:0]									00h	

Application Information (Continued)

Set Control Signal (Register Address – 00H)

Control Signal 00H – (Default: 0x02)							
D7	D6	D5	D4	D3	D2	D1	D0
R	R/W	R	W	W	R	R/W	R
0	HOT_EN	0	LD_ROM	WR_ROM	0	OUT_EN	0

Control HOT_EN		Control LD_ROM	
Register	Bit Description	Register	Bit Description
0	Enable Thermal Sensor.	0	Read Feedback Code
1	Disable Thermal Sensor.	1	Read Bank Data to EEPROM..

Control WR_ROM		Control OUT_EN	
Register	Bit Description	Register	Bit Description
0	Read Feedback Code	0	Disable Gamma Output.
1	Write Bank Data to EEPROM..	1	Enable Gamma Output.

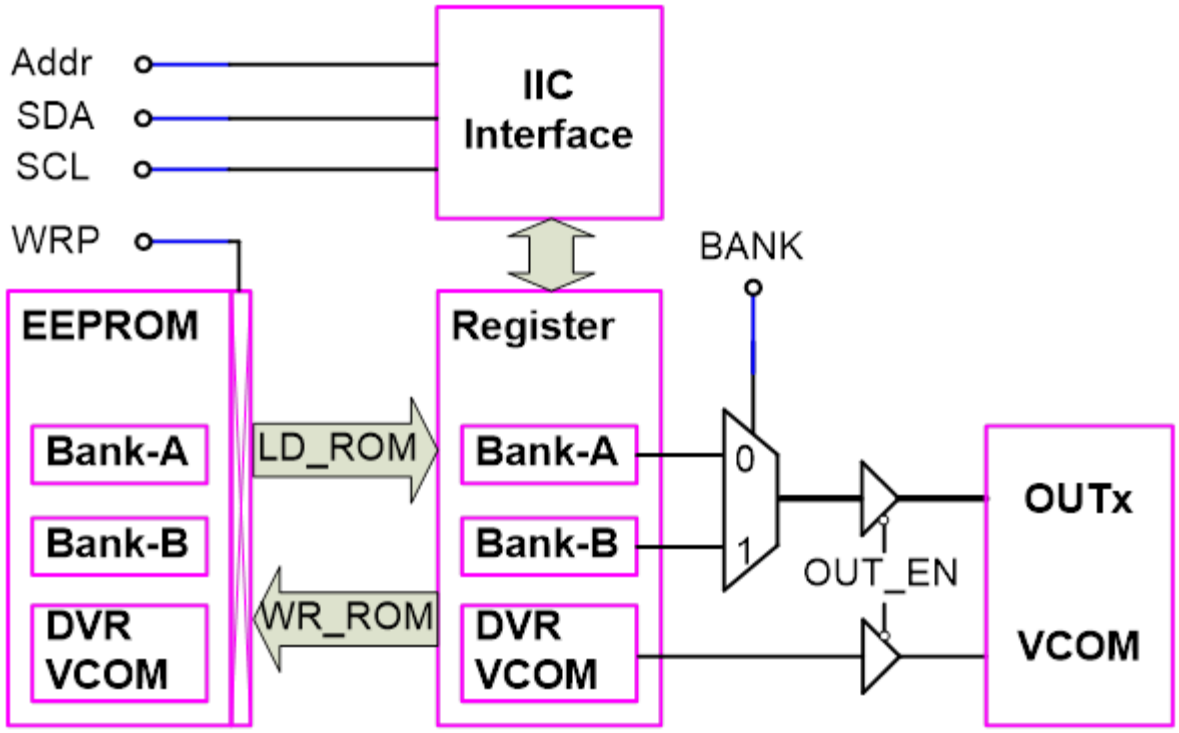


Figure 19. R[00h] Functional Block Diagram

Application Information (Continued)

5. IIC Programming Flow Chart

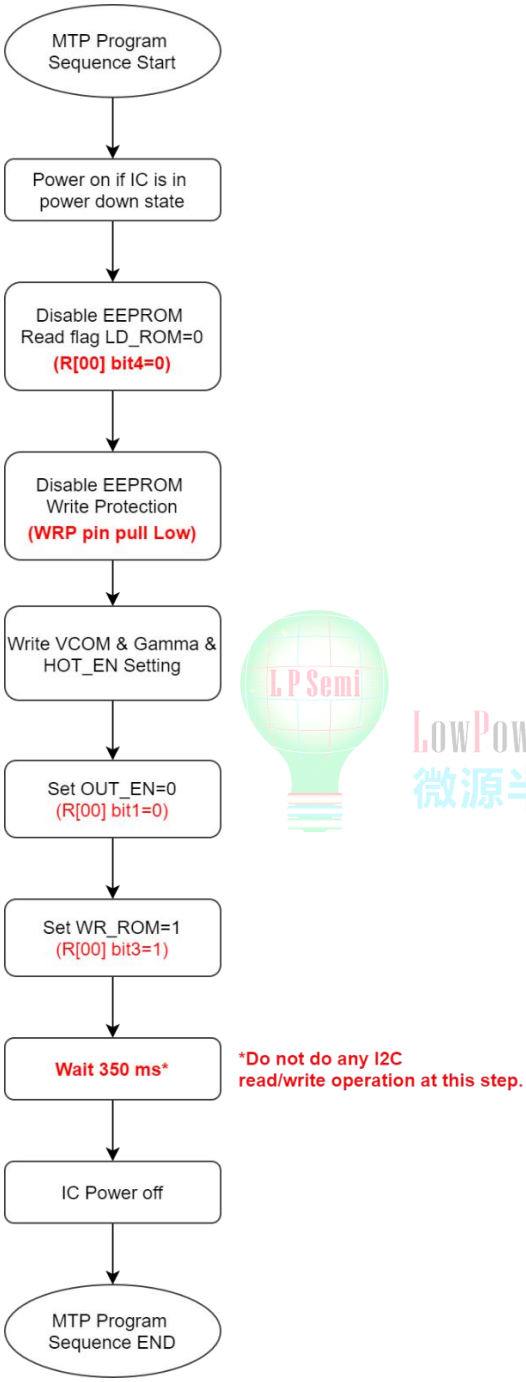


Figure 20. MTP Data Programming Flow

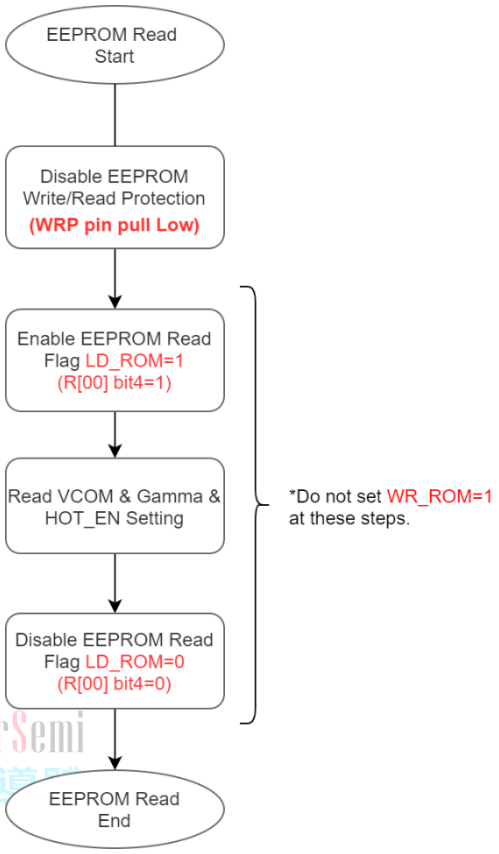


Figure 21. MTP Data Read Flow

Application Information (Continued)

Layout Guideline

The proper PCB layout and component placement are critical for all circuit. Here are some suggestions to the layout of LP6299 design.

1. Connected all ground together with one uninterrupted ground plane, which include digital ground and analog ground.
2. The input capacitor should be located as closed as possible to the VIN and ground plane.
3. All output capacitor must be closed to ground plane. The ground terminal of COUT must be located as closed as possible to ground plane.
4. The exposed pad of the chip should be connected to ground plane for maximum thermal consideration.

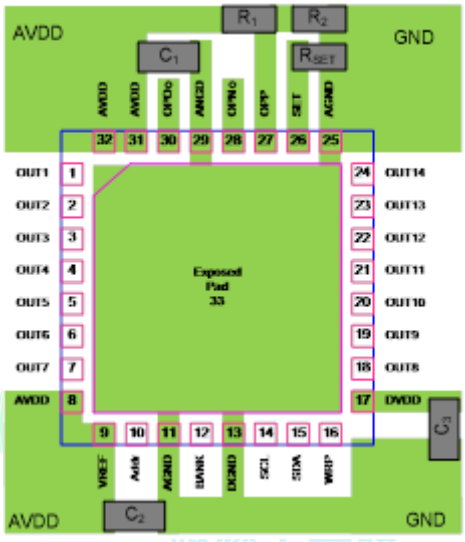
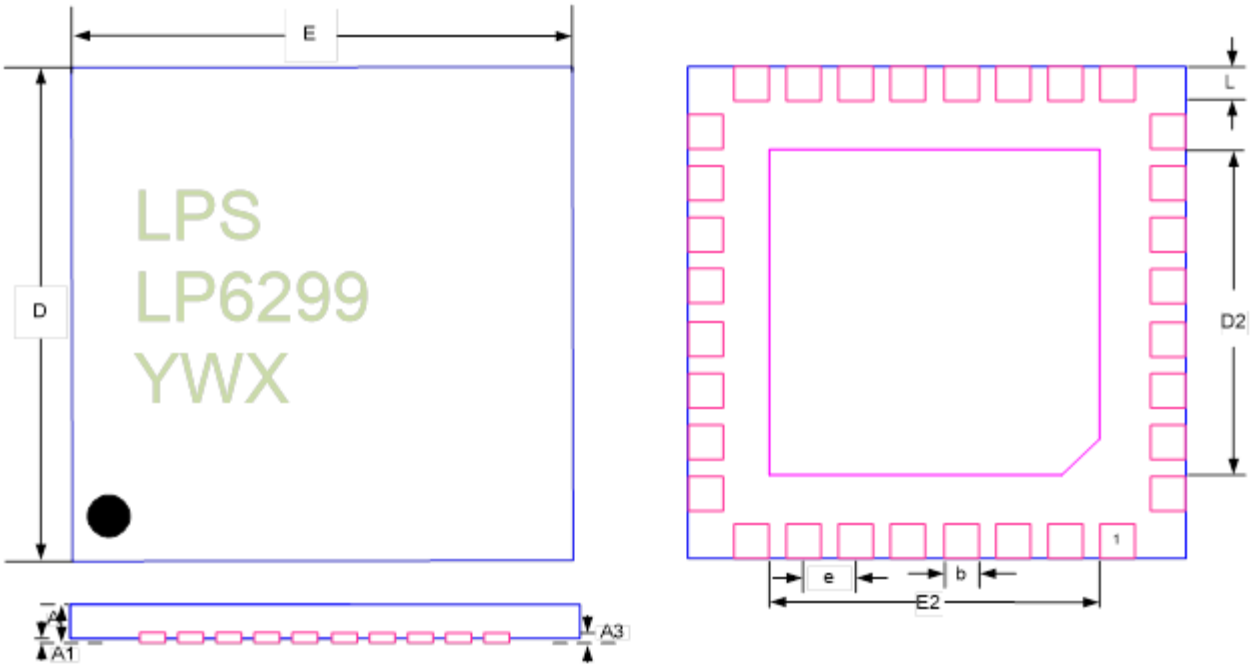


Figure 22. Recommended PCB Layout Diagram

Package Information

QFN-32 Package (5x5) pitch 0.5 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.180	0.250	0.300
A3		0.203 BSC	
D		5.000 BSC	
D2	3.450	3.500	3.550
E		5.000 BSC	
E2	3.450	3.500	3.550
e		0.500 BSC	
L	0.350	0.400	0.450