LP4080H

Ultra-high Efficiency Linear Charger for TWS Earphones

Features

- Input over-voltage protected up to 8-V
- 0.6-μA standby current from the battery
- Programmable charge current up to 300mA
- Ideal diode mode for high efficiency and low heat
- 7.5-mA fixed trickle charge
- 9-mA fixed termination current
- Programmable 4.0-V/4.2-V/4.35-V/4.4-V constant voltage options
- Automatic battery recharge control
- CHGb output for charging status indication
- ENb control to disable the charger
- RESET signal to prevent the bluetooth system on chip (SoC) firmware failure
- PWRON signal to automatically power on the earphone SoC once leaving the charging case
- Private one-wire bus to send instructions from the charging case to the linear charger for control
- Programmable general purpose output signal
- I2C interface with interrupt indication
- 4-uA ultra-low quiescent current
- 2mm X 2mm DFN-8 package
- RoHS Compliant and 100% Lead (Pb) free

Applications

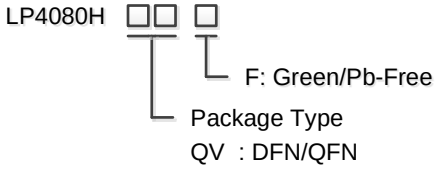
- TWS earphones
- Wireless microphone
- Smart Glasses

General Description

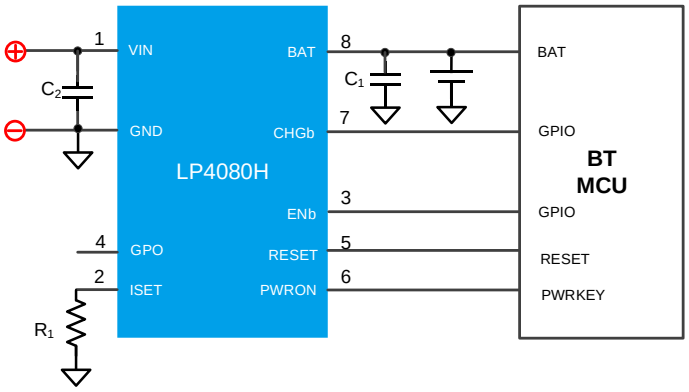
The LP4080H is an ultra-low power linear charger targeting at TWS earphone applications. It contains a linear charger to charge the Li-ion battery in the earphone with a CHGb charging status indication and an ENb input to disable the charger when needed. The constant charge current (CC) of the charger is programmable via the ISET pin by an external resistor. The charger has an ideal-diode mode for high efficiency and low heat operation. Two logic signals are offered to work with the Bluetooth SoC. The RESET outputs a reset signal to the SoC every time the earphone is placed into the charging case. The PWRON outputs a pulse signal to turn on the earphone SoC every time the earphone leaves the charging case. The GPO pin is a multifunctional output pin for system design. All these signals can also be controlled via a one-wire communication.

The whole system is in a small 8-pin 2x2 DFN package.

Order Information



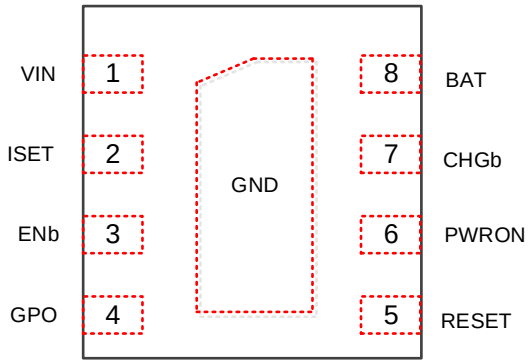
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	Note
LP4080HQVF	LPS LP4080H YWX	DFN-8	4K/REEL	
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



LP4080H Pinout

Pin Description

Pin #	Name	Description
1	VIN	Input voltage. A 220-pF input decoupling capacitor can be connected to this pin.
2	ISET	Charging current setting. Connect a resistor to this pin to program the charging current.
3	ENb	Enable control signal to the linear charger. Pull this pin high to disable the linear charger. This pin is internally pulled to GND with a resistor.
4	GPO	General purpose output. The operation of this pin is described in the one-wire section.
5	RESET	Reset signal output. This pin is open drain output.
6	PWRON	Power-on signal output. This pin is open drain output.
7	CHGb	Charging status output. This pin is open drain output.
8	BAT	Output of the linear charger.
Thermal PAD		GND pin

Absolute Maximum Ratings (Note)

VIN to GND ---------- 0.3V to 8V
Others to GND ---------- 0.3V to 6.5V
Operating Ambient Temperature Range (TA) ---------- 40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model, VIN pin) ---------- 8kV
HBM (Human Body Model, other pins) ---------- 2kV
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 125℃/W

Recommended Operating Conditions

Notes:
(1) All the values are effective capacitance or inductance.
(2) X5R and 16V or higher voltage rating are recommended.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	3		6	V
I_{CC}	Fast Charge Current	0.01		0.3	A
T_J	Operating Junction Temperature Range (T_J)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃
C_{IN}	Input Decoupling Capacitance(1) (2)			1	nF
C_{BAT}	BAT Capacitance(1) (3)	1	10		μF

Electrical Characteristics

(The specifications are at V_{VIN} = 5.0V , L=2.2μH, T_J = -40°C to +85°C and T_J = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{VIN}	VIN operation range		3		6	V
V_{UVLO}	VIN UVLO	VIN voltage falling	2.2	2.4	2.6	V
V_{UVLO_hys}	VIN UVLO hysteresis		50	100	150	mV
$R_{ds,on}$	PFET on resistance			0.5		Ω
I_{q_bat}	BAT Input quiescent current	V_{IN} = 0V, V_{BAT}=4.6V, ENb=0V		0.6	1	uA
V_{POR}	BAT Power-on-reset (POR)		1.6		2.4	V
V_{POR_HYS}	BAT POR hysteresis			100		mV

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INCASE}	In-case detection threshold		0.5		1	V
Charge Management						
V_{TRK}	Trickle charge voltage threshold	battery voltage rising	2.8	2.9	3.0	V
V_{TRK_HYS}	Trickle charge voltage hysteresis	battery voltage falling		100		mV
I_{TRK}	Trickle charge current		5	7.5	10	mA
I_{CC}	CC current	From -10°C to 85°C, R_{ISET} = 1kΩ	285	300	315	mA
		From -10°C to 85°C, R_{ISET} = 2kΩ	140	150	160	mA
		From -10°C to 85°C, R_{ISET} = 6kΩ	45	50	55	mA
V_{CV}	CV voltage	From -10°C to 85°C, 4.0V	3.96	4.0	4.04	V
		From -10°C to 85°C, 4.2V	4.158	4.2	4.242	V
		From -10°C to 85°C, 4.35V	4.306	4.35	4.394	V
		From -10°C to 85°C, 4.4V	4.356	4.4	4.444	V
$V_{recharge}$	Recharge threshold	Below CV voltage		-150		mV
I_{TERM}	Charge termination current		7	10	13	mA
$T_{foldback}$	Thermal foldback threshold		100	120	140	°C
V_{RCP}	RCP comparator threshold	From -20 to 125°C	0	25	50	mV
$V_{forward}$	Forward voltage regulation			50		mV
I_{CHGb}	CHGb output current capability	5mA current source, ref to GND			100	mV
t_{safe}	Safety timer[1]		2.5	3.75	5.0	hr
RESET						
t_{dreset}	Reset deglitch timer[1]		5	7.5	10	s
t_{pulse_reset}	RESET pulse width[1]		100	150	200	ms
V_{Hreset}	RESET output high level	Loaded with 10kΩ resistor, ref to BAT			-100	mV

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWRON						
t_{dpwron}	PWRON deglitch timer[1]		0.5	0.75	1	s
t_{pulse_pwron}	PWRON pulse width[1]		1.5	2.25	3	s
V_{Hpwron}	PWRON output high level	Loaded with 10kΩ resistor, ref to BAT			-100	mV
GPO						
V_{Lgpo}	GPO low output[1]	5mA current source ,ref to GND			100	mV
V_{Hgpo}	GPO high output[1]	Loaded with 10kΩ resistor, ref to BAT			-100	mV
I_{GPO}	GPO HiZ leakage	BAT=4.2V, GPO=4.0V, HiZ			1	uA
ENb						
V_{HENb}	ENb logic input high[1]	BAT=3.8V			1.2	V
V_{LENb}	ENb logic input low[1]	BAT=3.8V	0.4			V
One-wire timing						
	One-wire logic input high[1]	BAT=3.8V			1.2	V
	One-wire logic input low[1]	BAT=3.8V	0.4			V
t_{PRE_START}	Pre_start time[1]	Pre-start operating time before receiving the one-wire code	1	2	3	ms
t_{START}	Start bit time[1]	Start time after a falling edge sensed at VIN pin.	8	10	12	ms
t_{bit}	Code bit time[1]	1 bit code (‘0’ or ‘1’) cycle time	0.8	1	1.2	ms
t_{1h}	Code ‘1’ high time[1]	Code 1 high level time	704	880	1056	us
t_{1l}	Code ‘1’ low time[1]	Code 1 low level time	96	120	144	us
t_{0h}	Code ‘0’ high time[1]	Code 0 high level time	96	120	144	us
t_{0l}	Code ‘0’ low time[1]	Code 0 low level time	704	880	1056	us
t_{stop}	Stop time[1]	Stop time after a rising edge sensed at VIN pin.	0.8	1	1.2	ms

Typical Characteristics

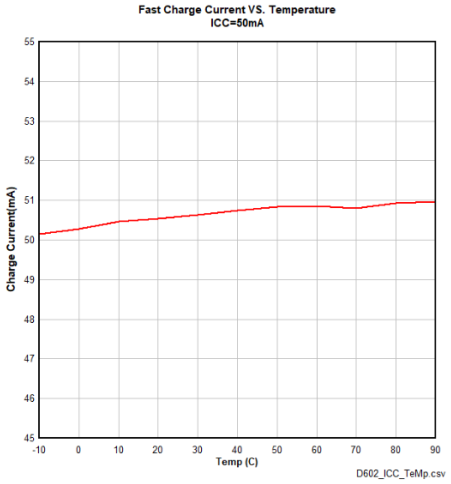


Figure 1. Fast charge current VS. Temperature.

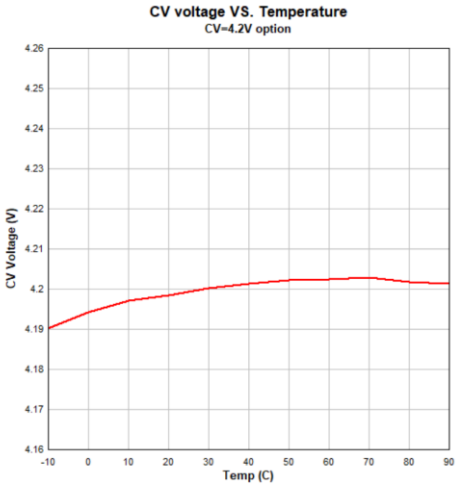


Figure 2. Floating voltage VS. Temperature.

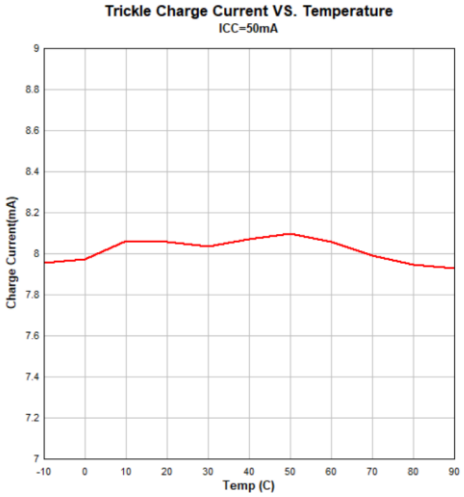


Figure 3. Trickle charge current VS. Temperature.

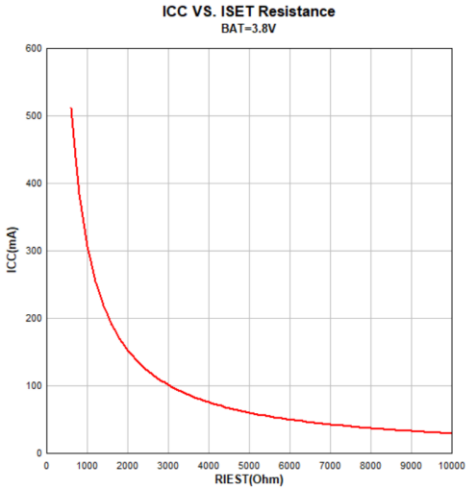


Figure 4. Fast charge current VS. R_{ISET}

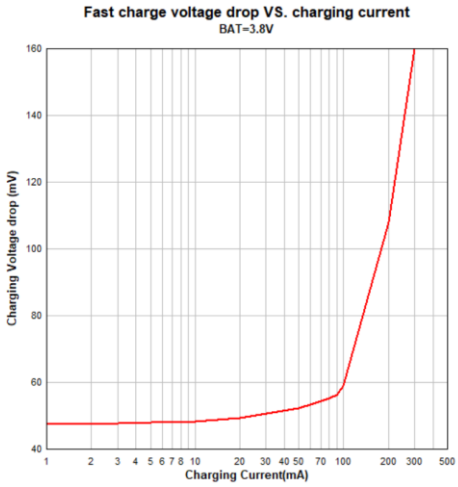
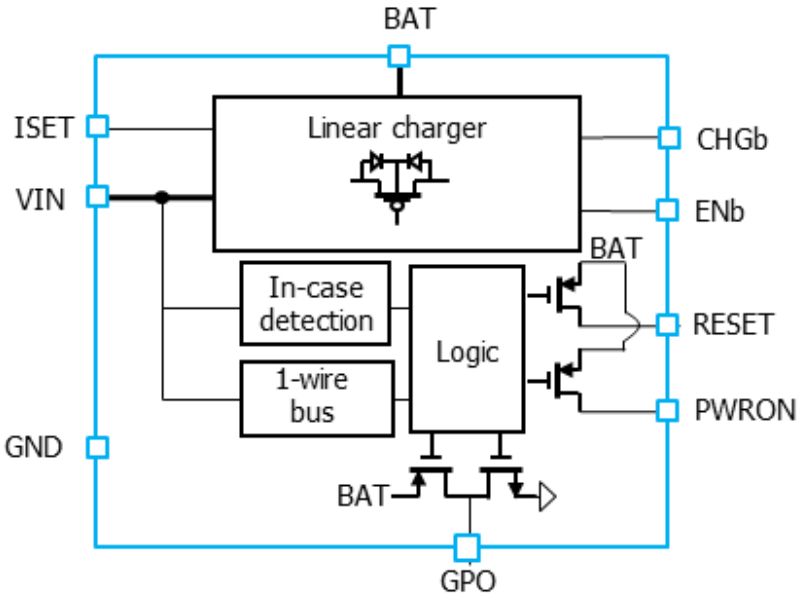


Figure 5. Minimum voltage drop VS. ICC

Functional Block Diagram


BAT
ISET
VIN
GND
Linear charger
In-case detection
1-wire bus
Logic
BAT
BAT
CHGb
ENb
RESET
PWRON
GPO

Detailed Description

Overview

The LP4080H is a charger target at TWS earphone applications. It contains a linear charger to charge the Li-ion battery in the earphone with a CHGb charging status indication and an ENb input to disable the charger when needed. The charger has an ideal-diode mode to achieve high efficiency and low heat performance when fast charge is needed. Two logic signals are offered to work with the Bluetooth SoC. The RESET outputs a reset signal to the SoC every time the earphone is placed into the charging case. The PWRON outputs a 2.25-s signal to turn on the earphone SoC every time the earphone leaves the charging case. The LP4080H integrates a general-purpose output pin as well, which is programmable by the one-wire protocol. The LP4080H supports no input decoupling capacitor to save the P-channel isolation MOSFET when the earphone is in a UART communication session with the charging case. When the linear charger is not in operation, the BAT leaks 0.6-μA current.

Power-on Reset

When the BAT pin is powered above the POR threshold, the LP4080H will perform a power-on reset. All the data in the register will be reset to default value.

Input section

The input management monitors the VIN pin to determine when to enable the charger. When the VIN voltage is higher than the under-voltage lockout (UVLO) threshold continuously for 300ms, the charger works. When the VIN voltage is lower than the falling edge of the UVLO threshold, the linear charger will be turned off immediately.

Linear Charger

The charger is a typical linear charger with three charging modes, i.e., trickle, CC, and CV modes. When the VIN voltage rises above the UVLO threshold, the charge cycle will start. When the VIN voltage falls below the UVLO falling thresholds, the charger stops. The ENb pin enables the charger when pulled to GND or left floating. Pulling the pin high will disable the charger. The charger has an open-drain CHGb pin that pulls low to indicate the charging status. The CHGb outputs high impedance when the end-of-charge (EOC) condition is reached.

Trickle charge:

The trickle-charge current is fixed at 7.5-mA current. The trickle-charge voltage threshold is fixed to 2.9V.

CC charge:

The constant current is programable via the ISET pin with a resistor. The resistance calculation equation is given below.

$$ICC = \frac{300}{\text{RISET}} \qquad (1)$$

The recommend ISET range is 10mA to 300mA.

The ISET pin can be used to monitor the charging current by sensing the ISET voltage.

CV charge:

The LP4080H supports four CV voltage options, which are 4.0-V, 4.2-V, 4.35-V and 4.4-V. The default CV voltage is 4.2V and can be programed by the one-wire bus if other CV voltage is needed.

EOC:

EOC is reached when the charge current reaches 9-mA and the battery voltage is higher than the recharge threshold. The CHGb is latched once EOC is triggered. The charge cycle continues until the safety timer is expired.

Safety timer:

A typical 3.75-hour safety timer is offered to terminate the charging cycle if the total charge time exceeds the 3.75-hour limit. This timer is refreshed when a valid VIN is inserted and the VIN is above the UVLO threshold or the recharge function is triggered.

Recharge:

A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage. CHGb output turns low when

the recharge cycle starts.

Ideal diode mode:

When the power supply to the VIN pin has a current capability lower than the ISET programmed CC charge current, the linear charger will enter an ideal diode mode. The power MOSFET for the charger will be fully turned on or clamped at a very low dropout voltage, which reduces the forward voltage of the ideal diode between the VIN and the BAT pins. The ideal diode has a reverse-current protection (RCP) comparator to prevent current reversing from the BAT pin to the VIN pin. A forward voltage regulation loop is integrated to avoid the conflict with the RCP comparator when the charging current reduces. The target regulated forward voltage is 50mV higher than the RCP threshold.

Charge current foldback:

When the die temperature reaches 120oC, the charge current will be reduced. The charger current recovers when the die temperature drops.

Charge Status Indication:

CHGb is an open-drain logic output that pulls low when the charger is in trickle, CC (including the ideal diode emulation mode), or CV mode. The CHGb is pulled to high by an external pull-up resistor.

Enable Control:

ENb pin controls the charger function with a default 1MΩ pull down resistor. The charger function is always enabled if no ENb input is toggled. The ENb control function is invalid and the charger function is forced enabled under these two conditions even the ENb is toggled high:

The BAT voltage is below the POR threshold.

The beginning 300mS after BAT POR.

RESET and PWRON outputs

The LP4080H integrates the earphone insertion and removal detection circuits as well. The insert signal is set to 1 when the VIN voltage is higher than the in-case detection threshold. The insert signal is set to 0 when the VIN falls to ground.

The RESET and PWRON are open drain outputs. A resistor pulled to ground should be connected to each pin.

RESET

When the VIN voltage is higher than the in-case detection threshold, an internal reset timer starts. The VIN voltage falling below the in-case detection threshold will clear the timer. If the timer lasts for 7.5s, the RESET output is set to high for 150ms and then falls to low.

The RESET signal can be stopped via the one-wire operation. If a one-wire signal sets a RESET STOP bit before the reset timer expires, no reset signal will be sent. The RESET STOP bit is cleared at the VIN power on reset.

PWRON

When the VIN voltage falls below in-case detection threshold for 0.75s (indicating the earphone has left the case), the PWRON pin will output a 2.25s high pulse to turn on the earphone SoC automatically.

For applications that has a Hall sensor to indicate the opening of the case, the charging case can send a one-wire signal to start the PWRON signal immediately and stop sending a repeating PWRON signal when the earphone leaves the case. A PWRON STOP bit will be set during the operating, which stops the 2.25s high pulse. The PWRON STOP bit will be cleared during the power-on reset.

Logic Output Signals --GPO

The LP4080H offers a general-purpose output (GPO) pin to extend the earphone system feasibility. The charging case sends one-wire instructions to change the GPO output state. Output high, output low and output high-Z are supported.

One typical application for the GPO is to achieve ship-mode as shown in figure 5. The VDD pin can be pulled below the UVLO threshold of the Li-ion battery protection chip by GPO pin in series with a resistor R2. The Li-ion battery protection chip is shut-down and turns off the battery discharge power path.

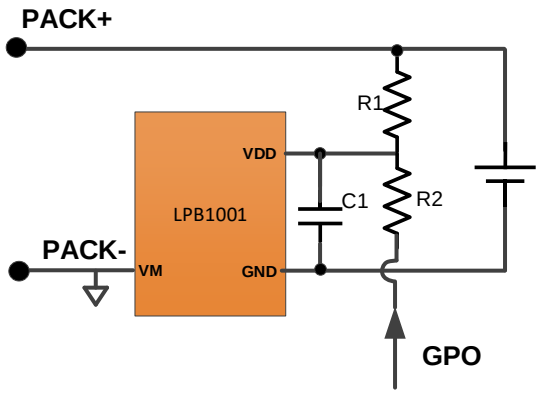


Figure 6. One GPO application example

Another typical application for the GPO is to reset some Bluetooth SoC where the reset signal is logic low active. The 1-wire instruction can change the GPO output state.

Standby state

The LP4080H enters three different standby states as described below:

The LP4080H enters Standby (Timeout) state when the battery is fully charged and the charging safety timer is expired.

The LP4080H enters Standby (Out of case) when the earphone leaves the charging case and the PWRON signal transmission is completed.

The LP4080H enters Standby (In case) when each of the following conditions are met:

The one-wire transmission to program the CV voltage or the GPO code is completed.

The earphone is in the charging case and the VIN voltage stays higher than the in-case detection threshold but lower than the UVLO threshold.

The LP4080H only consumes 0.6-uA quiescent current in standby state from the battery.

The LP4080H exits standby state with each of the following conditions are met:

The battery POR event occurs.

The battery starts a charging cycle, including the earphone insert charging event or a battery recharge event

One-wire communication is active.

The earphone insertion event is triggered.

One-wire bus

The LP4080H has a one-wire bus to accept private instructions from the charging case. Each one-wire communication session starts with a PRE_START pulse followed by a START bit, a 16-bit frame, and then a STOP bit. When LP4080H receives an instruction successfully, an ACK signal will be sent back to the MCU in the charging case (marked blue). The ACK consists of a start bit and a 7-bit header code. The LP4080H integrates 15 instructions.

The one-wire bus is not valid when the battery voltage drops below 2.7V.

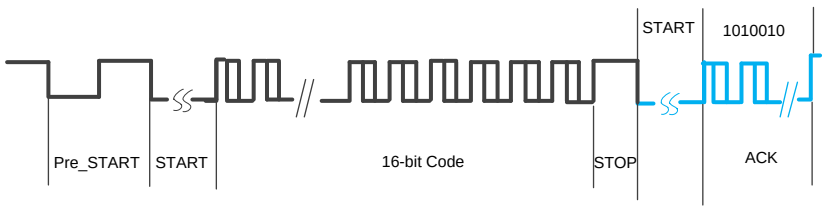


Figure 7 One-wire communication protocol

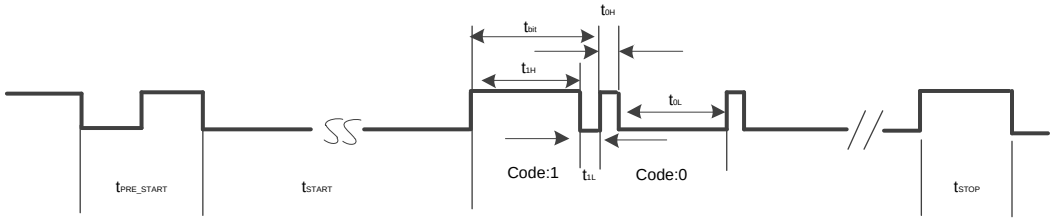


Figure 8. one-wire timing sequence

Table 1. one-wire instructions list

Code	Description	Function
0xA417	Clear RESET-STOP	RESET-STOP bit is cleared, no other bits are affected
0xA43E	Set RESET-STOP	RESET-STOP bit is set, no other bits are affected
0xA46C	Set RESET high	RESET outputs high. The RESET pin will be pulled to BAT pin internally.
0xA445	Clear RESET bit	RESET outputs low
0xA49A	Clear PWRON-STOP	PWRON-STOP bit is cleared. PWRON signal will be sent when the headphone leaves the charging case.
0xA4B3	Set PWRON-STOP	PWRON signal will not be sent when the headphone leaves the charging case.
0xA4E1	Set PWRON high	PWRON outputs high. The PWRON pin will be pulled to BAT pin internally.
0xA4C8	Clear PWRON bit	PWRON outputs low
0xA50D	Set GPO Low	The GPO pin will be pulled to GND.
0xA524	Set GPO Float	The GPO pin will be High-Z state.
0xA55F	Set GPO High	The GPO pin will be pulled to BAT pin internally.
0xA576	Set CV-4.2V	the CV voltage of the charger is set to 4.2V.
0xA580	Set CV-4.35V	the CV voltage of the charger is set to 4.35V.
0xA5A9	Set CV-4.4V	the CV voltage of the charger is set to 4.4V.
0xA5D2	Set CV-4.0V	the CV voltage of the charger is set to 4.0V.

Application Information

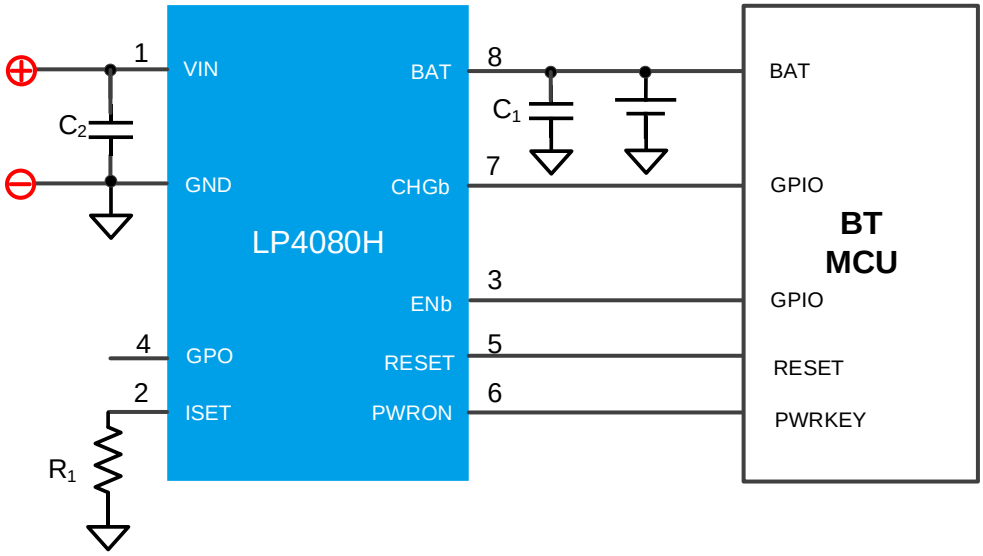


Figure 9. Typical Application Circuit

A typical application consists of the multi-function-in-one power management IC of LP4080H and a host bluetooth MCU. When powering up in default mode, the battery CV voltage of LP4080H is 4.2V. The MCU can change the default CV value by one-wire interface.

Set the input capacitor

The input capacitor should not be higher than 1-nF if the UART communication baud rate is higher than 400kbps. A 220pF capacitor is recommended to filter out the high frequency noise.

Programming the charging current:

The charging current of LP4080H is programmable by setting different resistors at the ISET pin. This pin can be used to monitor the charging current as well. According to the equation (1), the RISET resistor can be calculated.
For the fast-charging application, working with the LP7810, the charging current should set to a value higher than the current from the LP7810 VOL and VOR (EICC value) to achieve the low dropout and low heat performance. For example, a 5C fast charging current is needed for a 50-mAh battery, the charging current will be 250mA. Then the LP7810 should set the EICC register to 250mA while the LP4080H should be set to 300mA to ensure a constant 250mA from the upstream controller.

A 0402 size, 1KΩ value with ±1% accuracy is recommended in this application.

Set the BAT capacitor:

A minimum 1uF capacitor is needed at the BAT pin. For this application, a 10V, X5R, 1-uF capacitor is recommended.

Typical Waveforms:

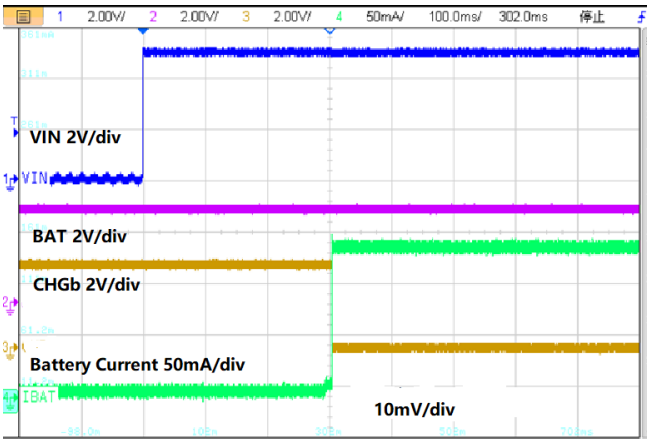


Figure 10. Startup by VIN , VIN=5V, RISET=2KΩ

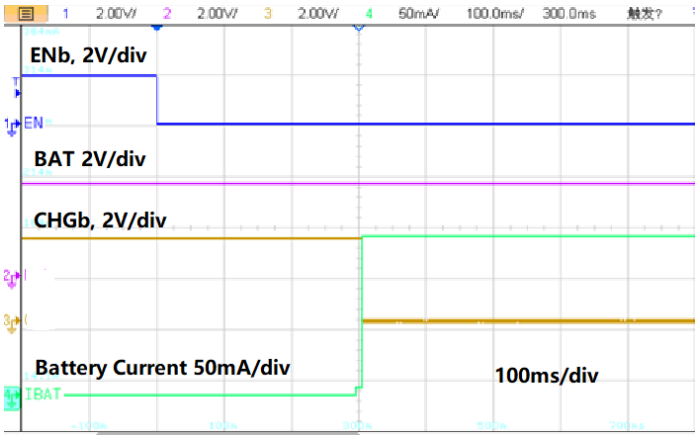


Figure 11. Startup by EN , VIN=5V, RISET=2KΩ

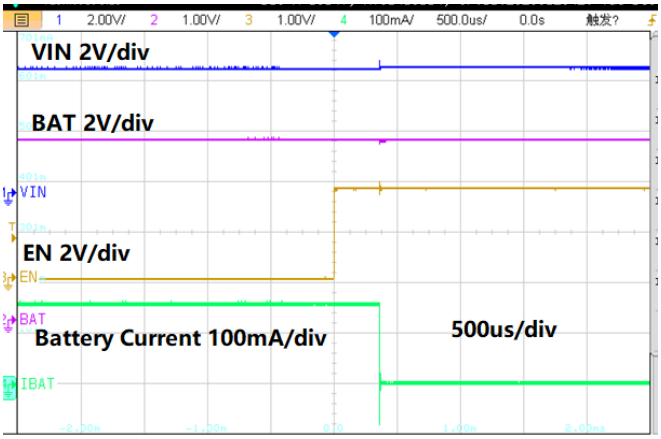


Figure 12. Shutdown by Enb,

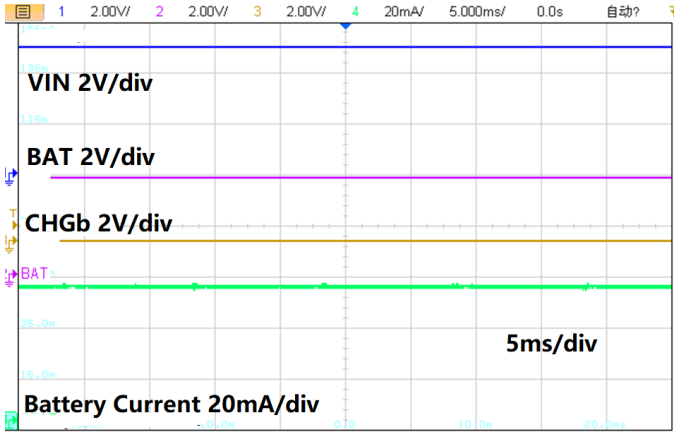


Figure 13. Charging waveform,

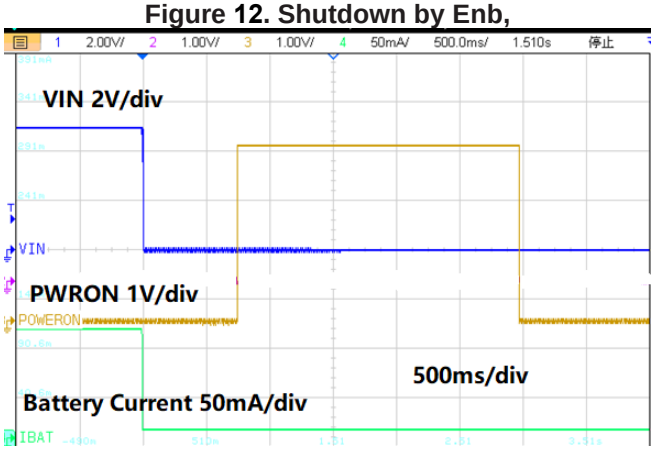


Figure 14. Leaving case PowerON

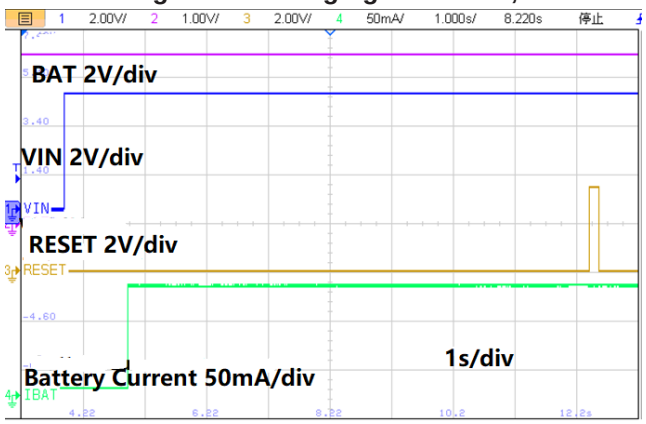


Figure 15. Insert Case RESET waveform

PCB Layout Guidelines

The LP4080H is a charger targeting TWS earphone applications. PCB rules should be guaranteed to achieve the design targets. The input capacitor and battery output capacitor should be placed as close the pin as possible to minimize the parasitic inductance. The DC-DC high frequency noise introduced by SoC PMIC should be restricted carefully to avoid the abnormal operation for applications when the input capacitance is less than 1nF.

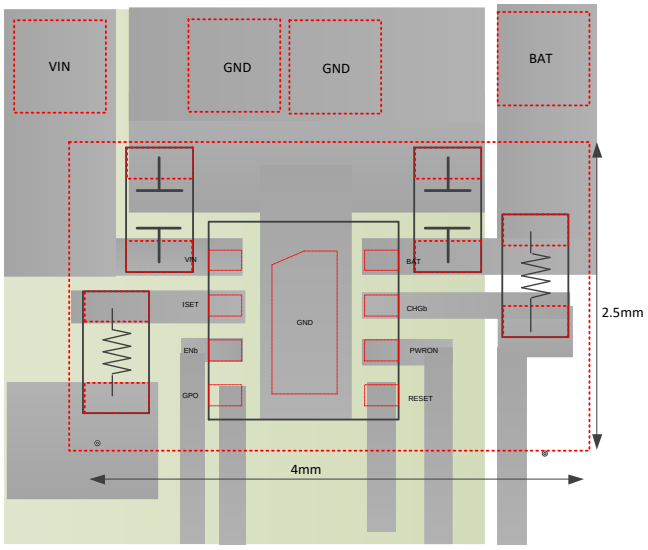
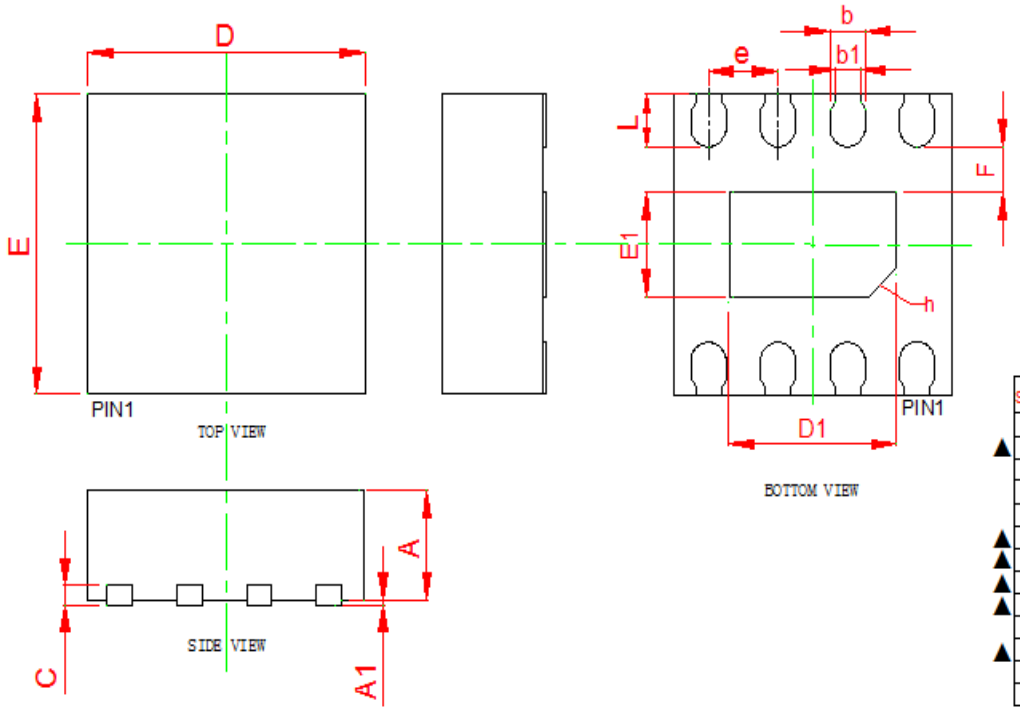


Figure 16. PCB layout example

Packaging Information

DFN-8



	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
	A	0.700	0.750	0.800
▲	A1	0.000	0.020	0.050
	b	0.200	0.250	0.300
	b1		0.18REF	
	C	0.180	0.200	0.220
▲	D	1.900	2.000	2.100
▲	E	1.900	2.000	2.100
▲	D1	1.100	1.200	1.300
▲	E1	0.600	0.700	0.800
	e	0.475	0.500	0.525
▲	L	0.300	0.350	0.400
	F	0.280	0.300	0.320
	h	0.230	0.280	0.330

Revision History

Revision	Date	Change Description
Rev 0.1p0	8/23/2021	Product Brief
Rev 1p0	1/11/2021	Initial Release
Rev 1p1	10/5/2022	Format update