20V/3A N-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM3414 is N-channel logic enhancement mode power field effect transistor, which are produced by using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suitable for low voltage applications, notebook computer power management and other battery powered circuits where high-side switching is needed.

Features

- 20V/3A, $R_{DS(ON)}$ < 62mΩ(max.)@VGS=4.5V
- 20V/2.5A, $R_{DS(ON)}$ < 86mΩ(max.)@VGS=2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOT23 Package

Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

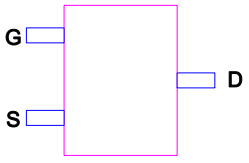
Order Information

LPM3414 □ □ □

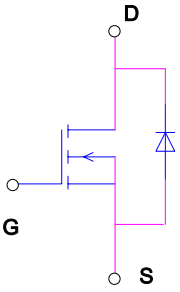
- F: Pb-Free
- Package Type
  - B3: SOT23-3

Pin Configurations

(SOT-23)
TOP VIEW



SOT23L(Top View)



Pin Description

Pin Number	Pin Description
1	Gate Pin
2	Source Pin
3	Drain Pin

Absolute Maximum Ratings

Absolute Maximum Ratings TA=25℃ Unless Otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		VDS	20	V
Gate-Source Voltage		VGS	±8	V
Continuous Drain Current	TA=25℃	ID	3	A
	TA=70℃		2.5	
Pulsed Drain Current		IDM	12	
Power Dissipation	TA=25℃	PD	1.4	W
	TA=70℃		0.9	
Junction and Storage Temperature Range		TJ, TSTG	-55 to 150	℃

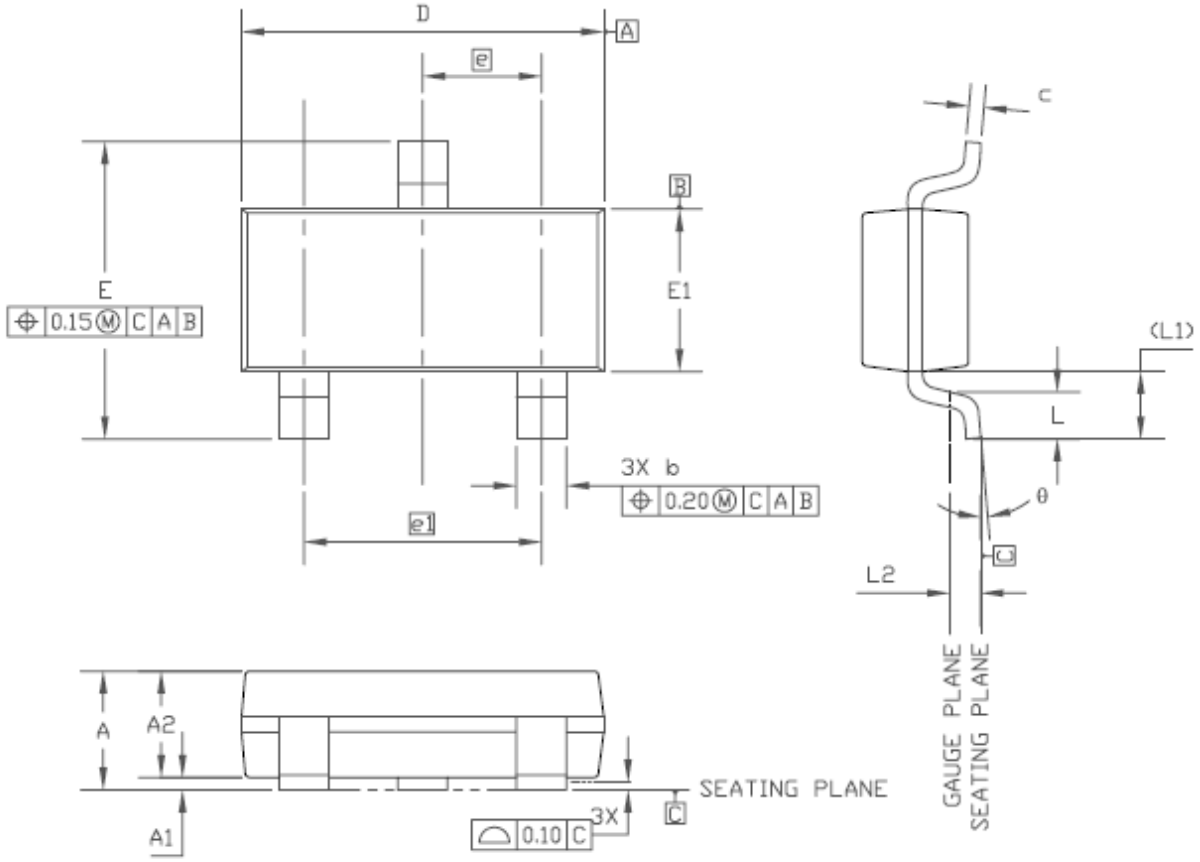
Thermal Characteristics			
Parameter	**Symbol**	**Typ.**	**Units**
Maximum Junction-to-Ambient	RθJA	125	℃/W

Electrical Characteristics

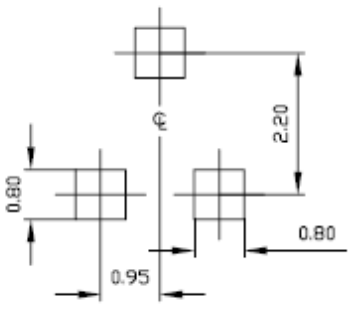
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
STATIC PARAMETER						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA , V_{GS}=0V	20			V
I_{DSS}	Zero-Gate Voltage Drain Current	V_{DS}=16V,V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V,V_{GS}=±8V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	I_D=250μA	0.4	0.6	1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=3A		41	50	mΩ
		T_J=125℃		58	70	
		V_{GS}=2.5V, I_D=3A		52	62	mΩ
		V_{GS}=1.8V, I_D=2.5A		67	86	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V,I_D=3A		11		S
VSD	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
IS	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	V_{DS}=10V,V_{GS}=0V		436		pF
CDSS	Output Capacitance	f = 1MHz		66		pF
Crss	Reverse Transfer Capacitance			44		pF
Rg	Gate Resistance	V_{DS}=0V,V_{GS}=0V f = 1MHz		3		Ω
SWITCHING PARAMETERS						
Qg	Total Gate Charge	V_{DS}=10V,V_{GS}=4.5V		6.2		nC
Qgs	Gate Source Charge	I_D=3A		1.6		nC
Qgd	Gate Drain Charge			0.5		nC
t D(ON)	Turn-On Delay Time	V_{DS}=10V,V_{GS}=5V		5.5		nS
tr	Turn-On Rise Time	R_L=2.7Ω		6.3		nS
t D(OFF)	Turn-Off Delay Time			40		nS
tf	Turn-Off Fall Time			12.7		nS
trr	Body-Diode Reverse Recovery Time	I_F=3A,d I/dt=100/μS		12.3		nS
Qrr	Body-Diode Reverse Recovery Charge	I_F=3A,d I/dt=100/μS		3.5		nC

Packaging Information

SOT−23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°