LP6280A

Dual Output Power Supply for LCD Bias

Features

- Input voltage range: 2.7V to 5.5V
- Programmable output voltages
  - VOP output voltage: 4V to 6V with 0.1V per step
  - VON output voltage: -6V to -4V with 0.1V per step
- 150mA positive operation current and support 200mA load transient at VOP
- 150mA negative sink current at VON
- 85% efficiency at VIN=4.4V, VOP/VON = +/-5.4V, 150mA output per channel
- I2C Interface
  - Flexible Output Voltage Programming
  - Programmable Active Output Discharge
- Protections
  - Input under-voltage lockout (UVLO)
  - Boost cycle-by-cycle current-limit protection
  - Output current limit and short circuit protection
  - Thermal shutdown protection
- Packaging
  - WLCSP 15 balls (1.19mm x 1.96mm)
  - RoHS Compliant and Halogen Free
  - 100% Lead (Pb) Free

Order Information

LP6280A □□

F: Pb-Free

Package Type

HV: WLCSP-15

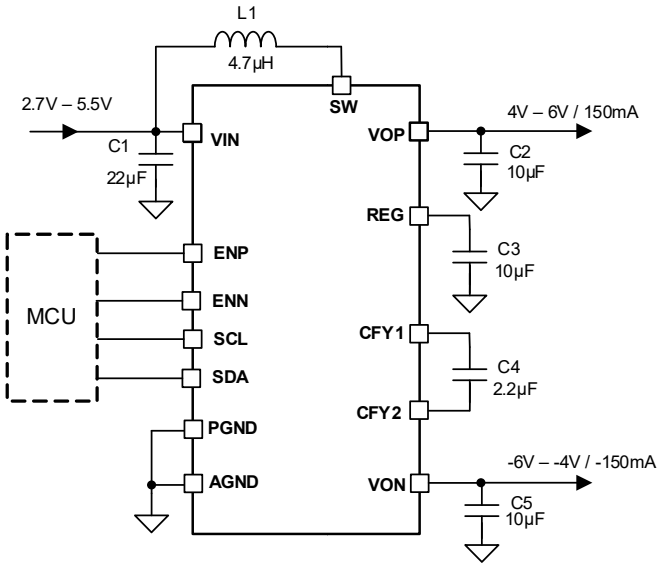
General Description

The LP6280A is designed to supply positive/negative driven applications. The device uses a single inductor scheme to provide both output currents. The integrated synchronous Boost converter provides a regulated voltage for a LDO and a charge pump. The LDO provides a regulated and programmable positive bias VOP and the charge pump provides a regulated and programmable negative bias VON. The device offers low noise, small solution size and high efficiency. The other feature includes under-voltage lockout (UVLO), internal soft-start, Boost cycle-by-cycle current limit and output over load and short circuit protection as well as thermal shutdown. The LP6280A is available in a space saving WLCSP 15-ball (0.4mm pitch) package.

Applications

- Small-, Medium-Size Bipolar LCD Displays
  - Smartphone, Tablet
  - Camera, GPS
  - Home Automation, Point-of-Sales
  - Wearables (Smart Watch, Activity Tracker)
- General Split-Rail Power Supply for
  - Differential Audio, Headphone Amplifier
  - Instrumentation, Operational Amplifier,Comparator
  - DAC/ADC

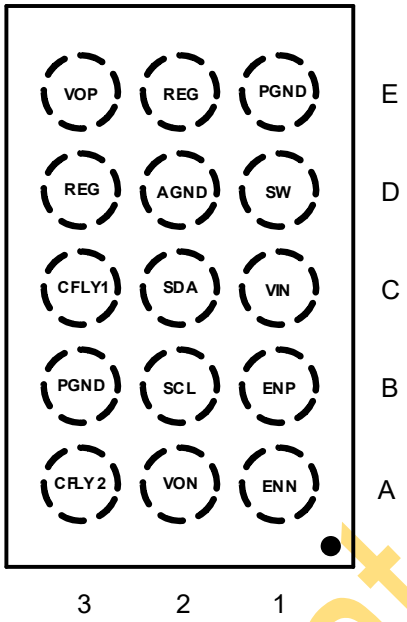
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Moisture Sensitivity Level	Shipping
LP6280A	LPS LP6280A YWX	WLCSP-15	MSL1	3K/REEL
Marking indication: Y: Year Code. W: Week Code. X: Batch Numbers.				

Pin Diagram

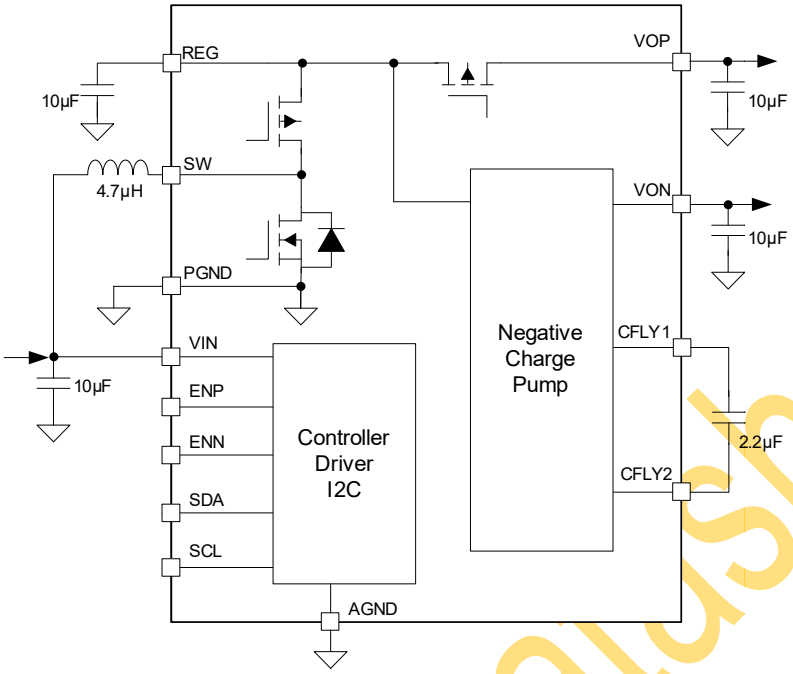


15-ball WLCSP (Top View)

Pin Description

Pin	Name	Description
A1	ENN	Enable input for VON rail.
A2	VON	Negative voltage output. Decouple this pin to PGND with a 10μF or higher ceramic capacitor as close to this pin as possible.
A3	CFLY2	Negative input for the external flying capacitor. Connect a terminal of a 2.2μF ceramic capacitor close to this pin.
B1	ENP	Enable input for VOP rail.
B2	SCL	I2C interface clock signal.
B3, E1	PGND	Power ground.
C1	VIN	Supply voltage input. Connect a 10μF ceramic capacitor from this pin to PGND.
C2	SDA	I2C interface data signal.
C3	CFLY1	Positive input for the external flying capacitor. Connect a terminal of a 2.2μF ceramic capacitor close to this pin.
D1	SW	Switching node output. Connect a terminal of an external inductor to this switching node. Short and wide trace is required for SW connection.
D2	AGND	Analog ground. Control circuitry returns current to this pin.
D3, E2	REG	Boost converter regulated output. Decouple this pin to PGND with a 10μF or higher ceramic capacitor as close to this pin as possible.
E3	VOP	Positive voltage output. Decouple this pin to PGND with a 10μF or higher ceramic capacitor as close to this pin as possible.

Functional Block Diagram



Absolute Maximum Ratings (1)

- VIN, SW, REG, VOP, VCFLY1, SDA, SCL Voltage to GND ---------- -0.3V to 7V
- VENN, VENP Voltage to GND---------- -0.3V to VIN+0.3V
- VON, VCFLY2 Voltage to GND ---------- -7V to 0.3V
- Maximum Junction Temperature (T_J) ---------- 150℃
- Storage Temperature Range ----------40℃ to 150℃
- Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

- HBM(Human Body Model) ---------- 2KV
- MM(Machine Model) ---------- 200V

Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage	2.7		5.5	V
I_{VOP}	Positive Output Current	0		150	mA
I_{VON}	Negative Output Current	0		150	mA
V_{VOP}	Positive Output Voltage	4.0	5.5	6.0	V
V_{VON}	Negative Output Voltage	-6.0	-5.5	-4.0	V
T_J	Operating Junction Temperature Range (T_J)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃
θ_{JA}	Thermal Resistance		85		℃/W
θ_{JC}	Thermal Resistance		1		℃/W
L	Boost Inductance(2)	3.76	4.7	5.64	μH
C_{IN}	Input Capacitance (2) (3)	4	10	30	μF
C_{REG}	Boost Output Capacitance(2) (3)	4	10	30	μF
C_{FLY}	Flying capacitance(2) (3)	0.9	2.2	2.64	μF
C_{VOP}, C_{VON},	Output Capacitance(2) (3)	4	10	30	μF

Note:

(1) The transient output current is allowed up to 150mA with higher output voltage drop.

(2) The values recommended in the table are effective inductance and capacitance.

(3) X7R, 0603 size and 10V (or 16V) voltage rating capacitors are recommended

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = 3.7V, V_{OP} = 5V, V_{ON} = -5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range		2.7		5.5	V
I_Q	Input Supply Current	VENN and VENP are tied to AGND			1	μA
I_Q	Input Supply Current			1		mA
V_{IN_UVLO}	Under Voltage Lockout of V_{IN}	V_{IN} Rising	2.2	2.4	2.65	V
$V_{IN\_UVLO\_HYS}$	V_{UVLO} Hysteresis	V_{IN} Falling		300		mV
SWITCHING BOOST CONVERTER						
F_{SW}	Switching Frequency	The old DS is OSC frequency	0.96	1.2	1.44	MHz
I_{LIM}	Switch Current Limit			1.5		A
D_{MAX}	Maximum Duty Cycle			90		%
R_{DSON_HS}	High-side MOSFET On-resistance			0.3		Ω
R_{DSON_LS}	Low-side MOSFET On-resistance			0.3		Ω
POSITIVE OUTPUT VOLTAGE LDO						
V_{OP}	Positive Output Voltage Range	21 steps, each step 100mV	4.0		6.0	V
V_{OP_ACC}	Positive Output Voltage Accuracy		-1.0		+1.0	%
I_{OP}	Positive Output Current Range		0		150	mA
V_{DROP}	Dropout voltage	V_{OP}=5V, I_{OP}=150mA		350		mV
	Line Regulation	V_{IN}=2.5V~4.2V, I_{OP}=150mA		1		%
	Load Regulation	I_{OP}=10mA to 150mA, V_{OP}=5.4V		1		%
R_{DIS_P}	VOP Discharge Resistance	V_{OP} = 5.4V		40		Ω
$V_{ENP(H)}$			1.2			V
$V_{ENP(L)}$					0.4	V
I_{ENP}	ENP Sink Current	V_{ENP}=2V		10		μA
I_{LIM}	Output Current Limit			0.30		A
I_{SCP}	Short Circuit Protection	V_{OP} < 40% of regulation		0.15		A

Electrical Characteristics (Continued)

(The specifications are at T_A=25℃, V_{IN} = 3.7V, V_{OP} = 5V, V_{ON} = -5V, unless otherwise noted.)

NEGATIVE OUTPUT VOLTAGE CHARGE PUMP						
F_{CP}	Negative Charge Pump Switching Frequency		0.96	1.2	1.44	MHz
V_{ON}	Negative Output Voltage Range	21 steps, each step 100mV	-6.0		-4.0	V
V_{ON_ACC}	Output Voltage Accuracy		-1.5		+1.5	%
I_{ON}	Negative Output Current Range		-150		0	mA
V_{DROP}	Dropout voltage	V_{OP}=5V, I_{OP}=150mA		350		mV
	Line Regulation	V_{IN}=2.5V~4.2V, I_{OP}=-150mA		1		%
	Load Regulation	I_{ON}=-150mA to -10mA, V_{ON}=-5.4V		1.5		%
R_{DIS_N}	VON Discharge Resistance	V_{ON}=5.4V		30		Ω
$V_{ENN(H)}$			1.2			V
$V_{ENN(L)}$					0.4	V
I_{ENN}	ENN Sink Current	V_{ENN}=2V		10		μA
I_{SHORT}	Output Short Current			0.15		A
THERMAL SHUTDOWN PROTECTION						
T_{SHUT}	Thermal Shutdown	Temperature Rising		140		℃
T_{SHUT_HYST}	Thermal Shutdown Hysteresis	Temperature Falling		30		℃

Electrical Characteristics (Continued)

(The specifications are at T_A=25℃, V_{IN} = 3.7V, V_{OP} = 5V, V_{ON} = -5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I2C Compatible Timing Specifications (SCL, SDA), referred to Figure 8						
f_{SCL}	SCL clock frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7			us
		Fast Mode	1.3			us
$t_{HD, SDA}$	Hold time for a repeated START condition	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU, DAT}$	Data setup time	Standard Mode	0.25			us
		Fast Mode	0.1			us
$t_{HD, DAT}$	Data hold time	Standard Mode	0.05		3.45	us
		Fast Mode	0.05		0.9	us
t_{RDA}	Rise time of SDA signal	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
t_{FDA}	Fall time of SDA signal	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0		-	
		Fast Mode	0.6		-	
C_B	Capacitive load for SCL and SDA		-	-	0.2	nF

Typical Characteristics

VIN=3.7V, VOP=5V,VON=-5V, TA=+25°C, unless otherwise noted.

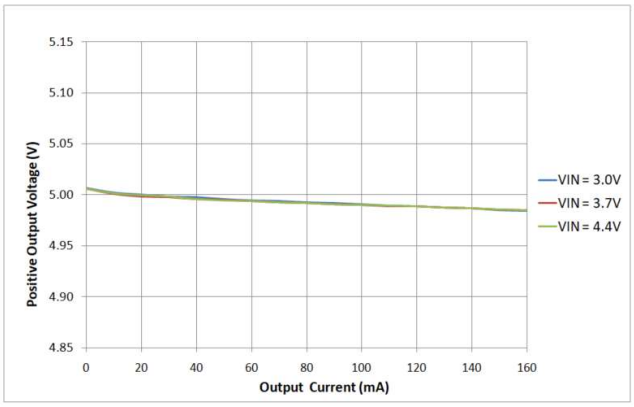


Figure 1. Positive Output Voltage V_{OP} vs. Output Current

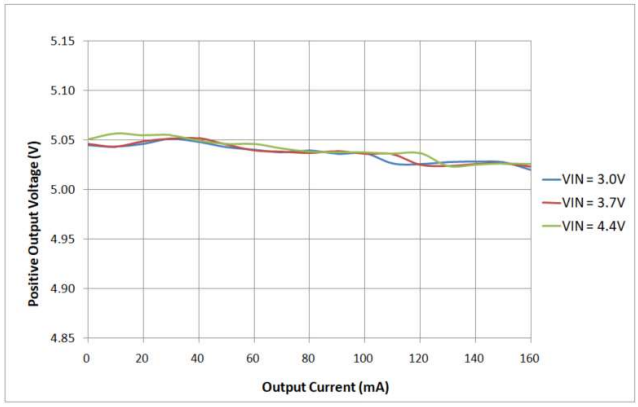


Figure 2. Negative Output Voltage V_{ON} vs. Output Current

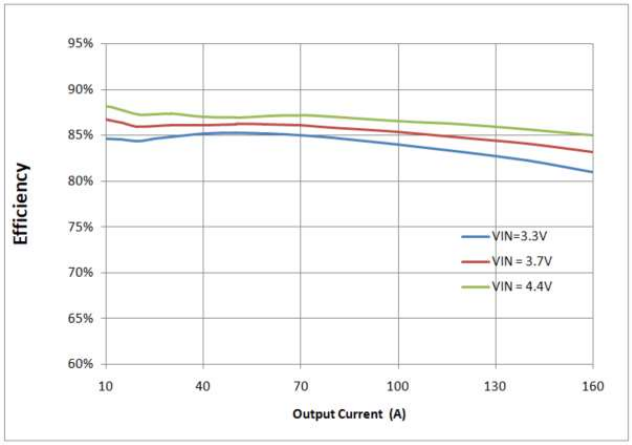


Figure 3. Efficiency (V_{VOP} = 5V, V_{VON} = -5V)

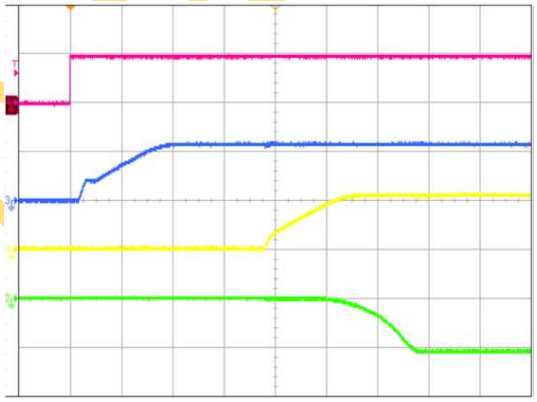


Figure 4. VOP and VON Enable

CH1: ENP = ENN = 0 to 1, 5V/div, CH2: V_{REG}, 5V/div, CH2: V_{OP}, 5V/div, V_{ON}, 5V/div, Time: 500us/div)

Typical Characteristics (Continued)

VIN=3.7V, VOP=5V,VON=-5V, TA=+25°C, unless otherwise noted.

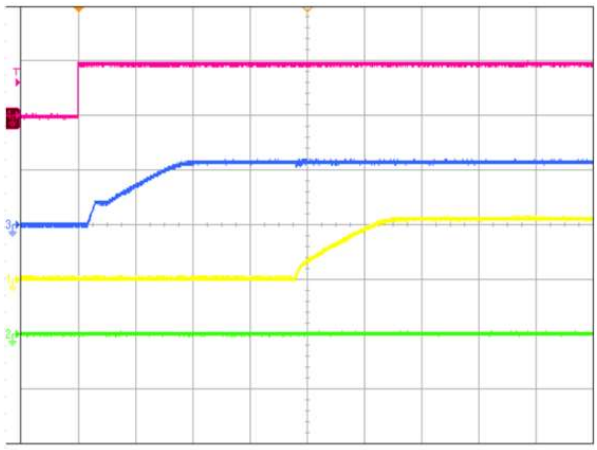


Figure 5. VON Enable

CH1: ENP = ENN = 0 to 1, 5V/div, CH2: V_{REG}, 5V/div, CH2: V_{OP}, 5V/div, V_{ON}, 5V/div, Time: 500us/div)

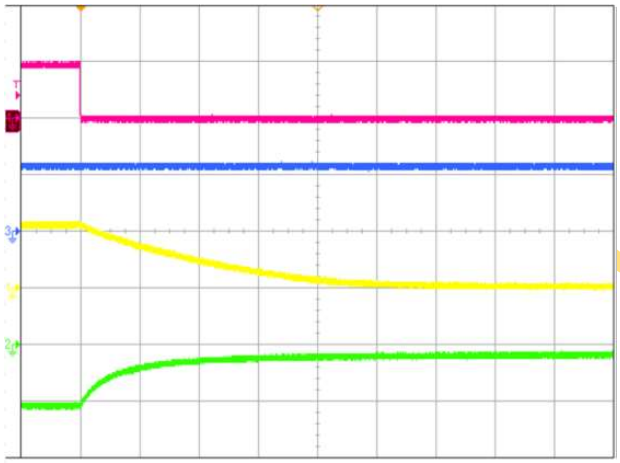


Figure 6. VOP and VON Disable

CH1: ENP = ENN = 1 to 0, 5V/div, CH2: V_{REG}, 5V/div, CH2: V_{OP}, 5V/div, V_{ON}, 5V/div, Time: 500us/div)

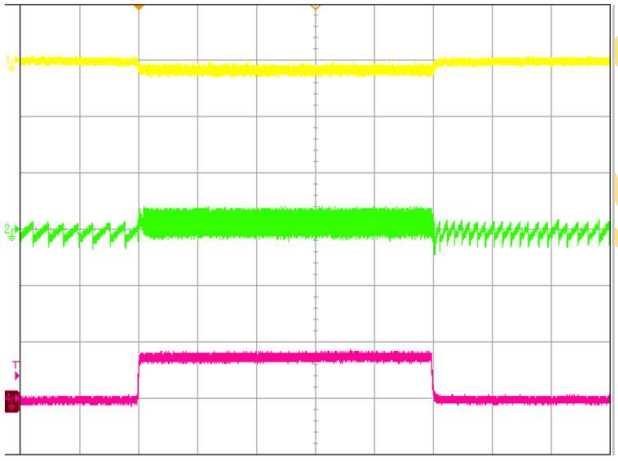


Figure 7. Load transient response`

(CH1: V_{OP}, 100mV/div, CH2: VON, 100mV/div, CH3: Iout, 100mA/div, Time: 500us/div)

Detailed Description

Overview

The LP6280A supports input voltage range from 2.7 V to 5.5 V, operates with a single inductor scheme to provide a high efficiency with a small solution size. The synchronous boost converter generates a positivevoltage that is regulated down by an integrated LDO, providing the positive supply rail (V_{OP}). The negativesupply rail (V_{ON}) is generated by an integrated negative charge pump (or CPN) driven from the boost converter output pin REG.

Undervoltage Lockout (UVLO)

The LP6280A integrates an undervoltage lockout block (UVLO) that enables the device once the voltage on the VIN pin exceeds the UVLO threshold. No output voltage will be generated as long as the enable signals are not pulled HIGH. The device, as well as all converters (Boost converter, LDO, CPN), will be disabled as soon as the VIN voltage falls below the UVLO threshold.

Power Enable

The LDO (VOP) and the negative charge pump (VON) are turned on/off by external enable signals. ENP pin is enable control input for VOP and ENN is enable control input for VON. If any enable signal is pulled high, Boost will be enabled once V_{IN} meets UVLO voltage level.

Boost Converter

The LP6280A integrates a PWM synchronous Boost converter operating with current mode control and 1.2MHz (typ) switching frequency. The device is designed for high efficiency over wide output current range.

VOP and VON Discharge

When VIN falls below UVLO threshold or both ENP and ENN pins are pulled low, all regulators will be turned off. If both ENP and ENN go low, VOP and VON will be actively discharged to GND.

Power Sequencing

The LP6280A Boost powers up if any of ENP and ENN is pulled high. If the Boost powers up successfully within 2ms, Boost Power Good signal is sent to enable VOP and/or VON rail(s). VOP startup time is about 1ms and VON startup time is about 1.5ms. VOP and VON rails can be enabled sequentially or simultaneously. Similarly, VOP and VON rails can be disabled sequentially or simultaneously. Boost powers off only when both ENP and ENN are pulled low.

Thermal Shutdown Protection

The LP6280A device enters over temperature protection if its junction temperature exceeds 140°C (typical). During over temperature protection the device is shut down. Once the junction temperature falls below the hysteresis threshold, the device restarts.

I2C Interface Specification

The LP6280A can easily modify parameters by I2C bus and the slave address is 0x3E. I2C is a two wire serial interface developed, the bus consists of a clock line (SCL) and a data line (SDA) with pull-up structures. The LP6280A works as a slave mode, and address is 0x3E. The data transfer protocol follow I2C-Bus Specification's standard mode (100kbps) and fast mode (400kbps).

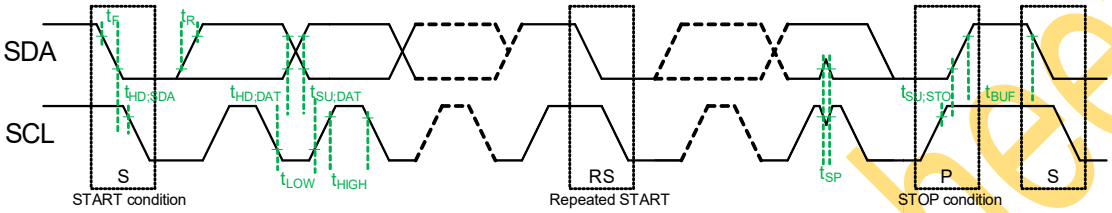


Figure 8. START and STOP Conditions

Write Data to Register

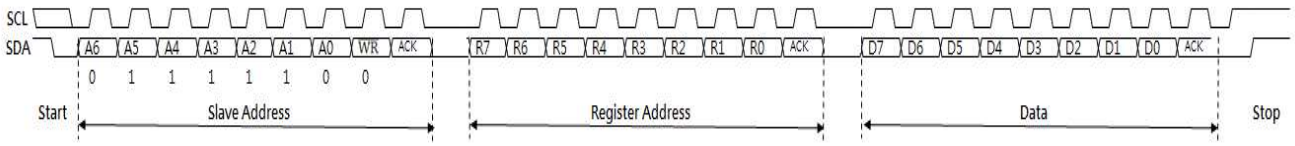


Figure 9. Write Single Byte Data to Register

Read Data to Register

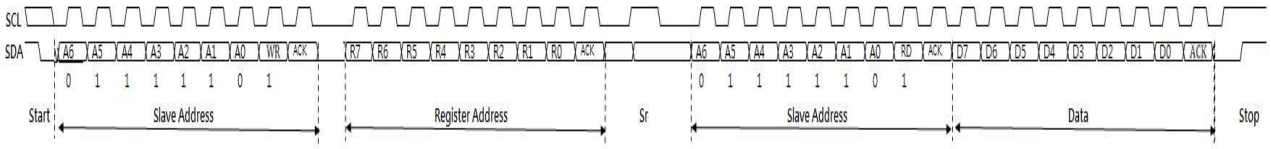


Figure 10. Read Single Byte Data from Register

Register Maps

Address	Description	Default	D7	D6	D5	D4	D3	D2	D1	D0
00H	SetVOP Voltage	0x0F	--		--	VOP [4:0]				
01H	SetVON Voltage	0x0F	--		--	VON [4:0]				
03H	Set Discharge Resistor Enable	0x03	--	--	--	--	--	--	DIS_VOP	DIS_VON
FFH	Set Control Register	0x00	WR	--	--	--	--	--	--	--

Set VOP Voltage (Register Address – 00H)

VOP Voltage							
Addr: 00H	Default Value: VON Register=0x0F, (VOP =5.5V)						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	VOP[4]	VOP [3]	VOP [2]	VOP [1]	VOP [0]

VOP [4:0]			
Register	Volt (V)	Register	Volt (V)
00000	4.00	10000	5.60
00001	4.10	10001	5.70
00010	4.20	10010	5.80
00011	4.30	10011	5.90
00100	4.40	10100	6.00
00101	4.50	10101	Reserved
00110	4.60	10110	Reserved
00111	4.70	10111	Reserved
01000	4.80	11000	Reserved
01001	4.90	11001	Reserved
01010	5.00	11010	Reserved
01011	5.10	11011	Reserved
01100	5.20	11100	Reserved
01101	5.30	11101	Reserved
01110	5.40	11110	Reserved
01111	5.50	11111	Reserved

Set VON Voltage (Register Address – 01H)

VON Voltage							
Addr: 01H	Default Value : VON(Register)=0x0FH, VON =-5.5V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	VON[4]	VON [3]	VON [2]	VON [1]	VON [0]

VON[4:0]			
Register	Volt (V)	Register	Volt (V)
00000	-4.00	10000	-5.60
00001	-4.10	10001	-5.70
00010	-4.20	10010	-5.80
00011	-4.30	10011	-5.90
00100	-4.40	10100	-6.00
00101	-4.50	10101	Reserved
00110	-4.60	10110	Reserved
00111	-4.70	10111	Reserved
01000	-4.80	11000	Reserved
01001	-4.90	11001	Reserved
01010	-5.00	11010	Reserved
01011	-5.10	11011	Reserved
01100	-5.20	11100	Reserved
01101	-5.30	11101	Reserved
01110	-5.40	11110	Reserved
01111	-5.50	11111	Reserved

Set Discharge Resistor Enable (Register Address – 03H)

Discharged Resistor Enable/Disable							
Addr: 03H	Default Value : DIS_VO(Register)=0x03H						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	DIS_VOP	DIS_VON

DIS_VOP		DIS_VON	
Register	DIS_VOP	Register	DISP_VOP
0	Disable	0	Disable
1	Enable	1	Enable

Set Control Register (Register Address – FFH)

Control Register							
Addr: FFH	Write : Control(Register)=0x80H, Read : Control(Register)=0x00H						
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R
W_EPROM	0	0	0	0	0	0	0

W_EPROM	
Register	Bit Description
0	Disable any registers data write into the EPROM
1	Enable all register's data to write into the EPROM

Application Information

The device can be used for any applications that require positive and negative supplies, ranging from ±4V to ± 6V and current up to 150mA. The positive and negative output voltages are independently programmable by I2C interface and their sequencing is also independently programmable by external signals at ENP and ENN pins.

Boost Input Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended at input VIN pin. A minimum effective capacitance of 4μF is required at VIN pin. Considering capacitance de-rating with higher temperature and DC bias voltages, X7R, and 10V or 16V voltage rating are recommended.

Boost Inductor Selection

A 4.7μH inductor is recommended as shown in the table of Recommended Operating Conditions. In general, lower inductor DCR and larger inductor size support higher Boost conversion efficiency.

Boost Output Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended as shown in the table of Recommended Operating Conditions. A minimum effective capacitance of 4μF is required. Higher capacitor values and higher voltage ratings can be used to improve load transient response.

LDO Output Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended as shown in the table of Recommended Operating Conditions. A minimum effective capacitance of 4μF is required. Higher capacitor values and higher voltage ratings can be used to improve load transient response.

Charge Pump Output Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended as shown in the table of Recommended Operating Conditions. A minimum effective capacitance of 4μF is required. Higher capacitor values and higher voltage ratings can be used to improve load transient response.

Flying Capacitor Selection

A 2.2μF low ESR ceramic capacitor is recommended as shown in the table of Recommended Operating Conditions. Flying capacitor values directly impact the VON output voltage accuracy and load transient response. A minimum effective capacitance of 0.9μF is required at a DC bias of V_{ON} + 0.3V. For proper operation, the flying capacitor effective value must be lower than the Boost effective output capacitance.

Power-on and Power-off Sequence

If VOP and VON target voltages are set at higher than 5.2V, the power-on and power-off sequence is recommended as shown in Figure 11. If VOP and VON target voltages are set at lower than or equal to 5.2V, the power-on and power-off sequence is recommended as shown in Figure 12.

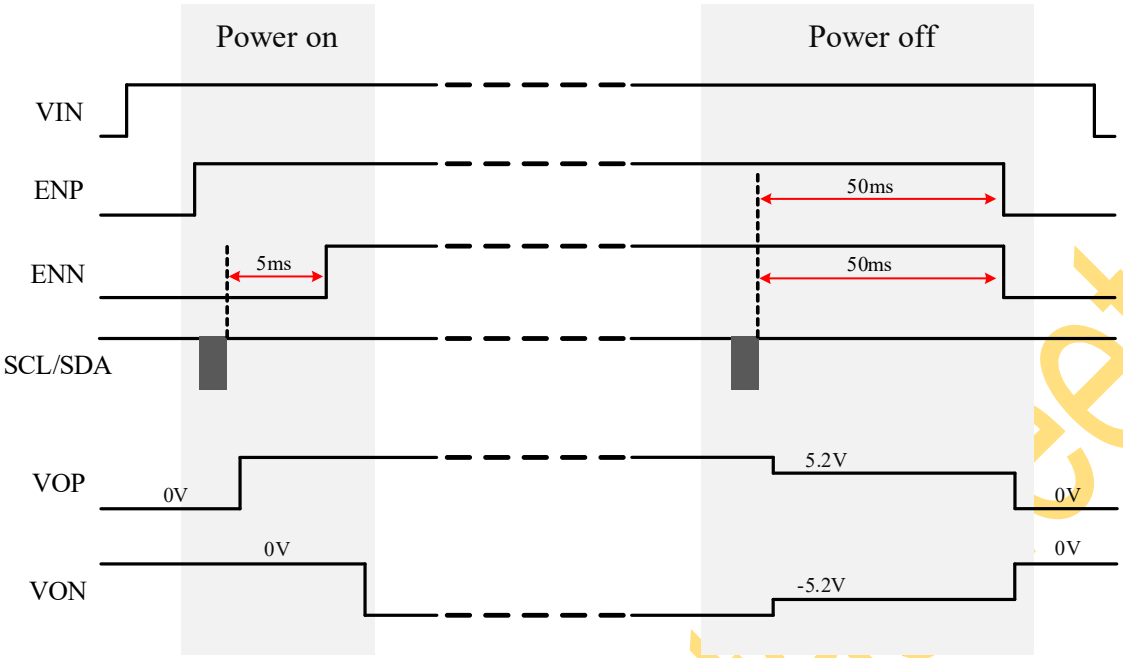


Figure 11. Power on/off sequence (VOP/VON >5.2V)

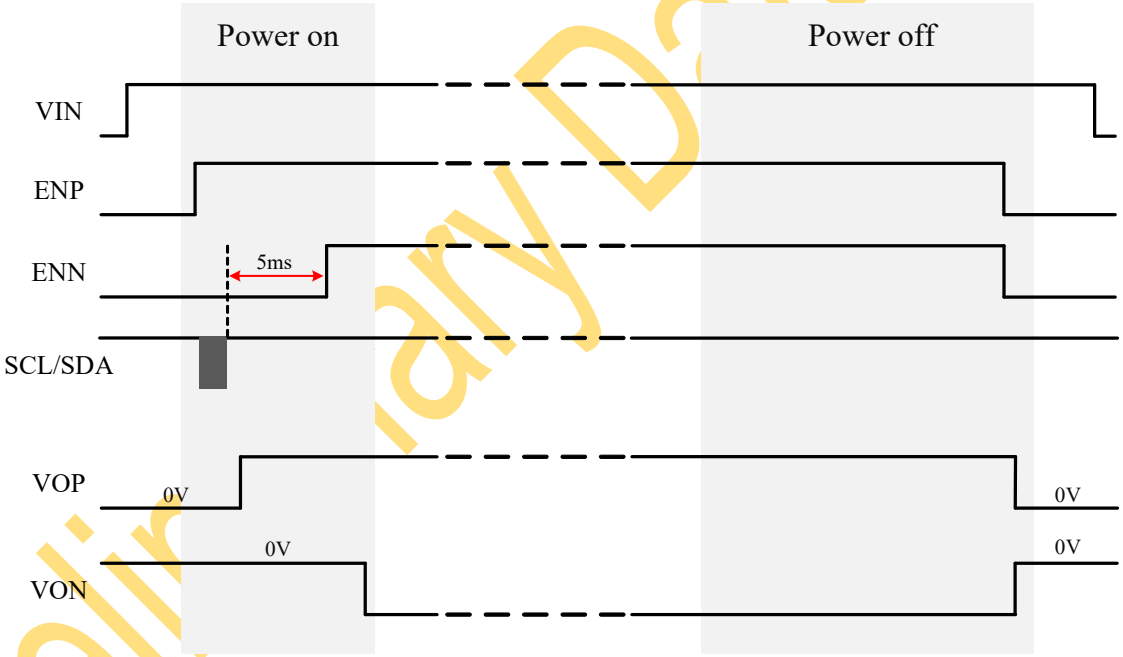


Figure 12. Power on/off sequence (VOP/VON≤5.2V)

PCB Layout Guideline

Appropriate PCB layout is important in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the LP6820A, the following PCB layout guidelines are recommended.

1. Decouple VIN, REG, VOP and VON pins to PGND on the top layer and place decoupling capacitors as close to the pins as possible. Always avoid vias when possible because they have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitics especially for power traces.
2. Connect AGND and PGND ground together with at least one uninterrupted ground plane, which include power ground and analog ground.
3. Place the flying capacitor as close as possible to the CFY1 and CFY2 pins and connect flying capacitors to the IC pins with short and wide traces.
4. Minimize trace length of SW node if possible to help reduce EMI emissions and noise that may couple into other portions of the converter.

An example of 2-layer PCB layout is shown in Figure 13.

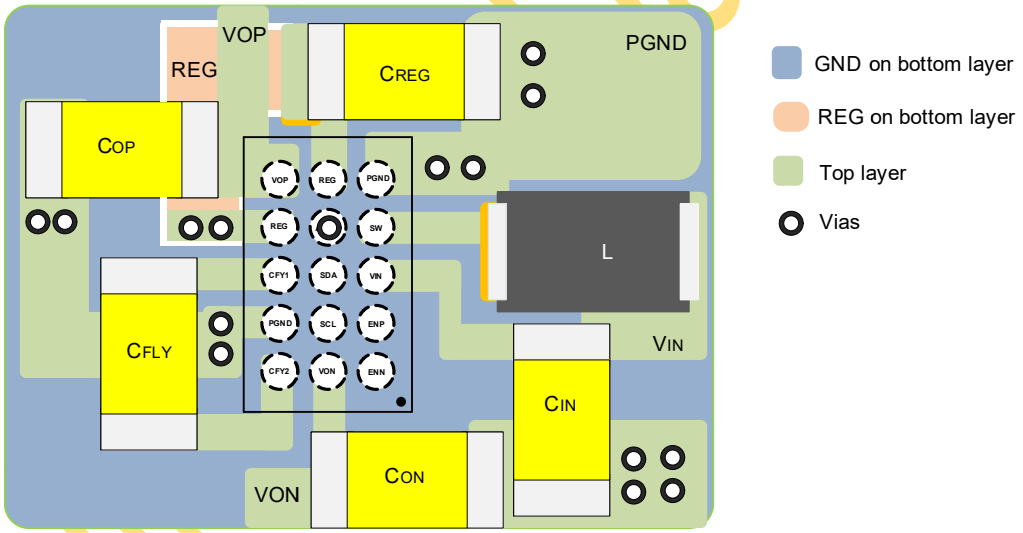
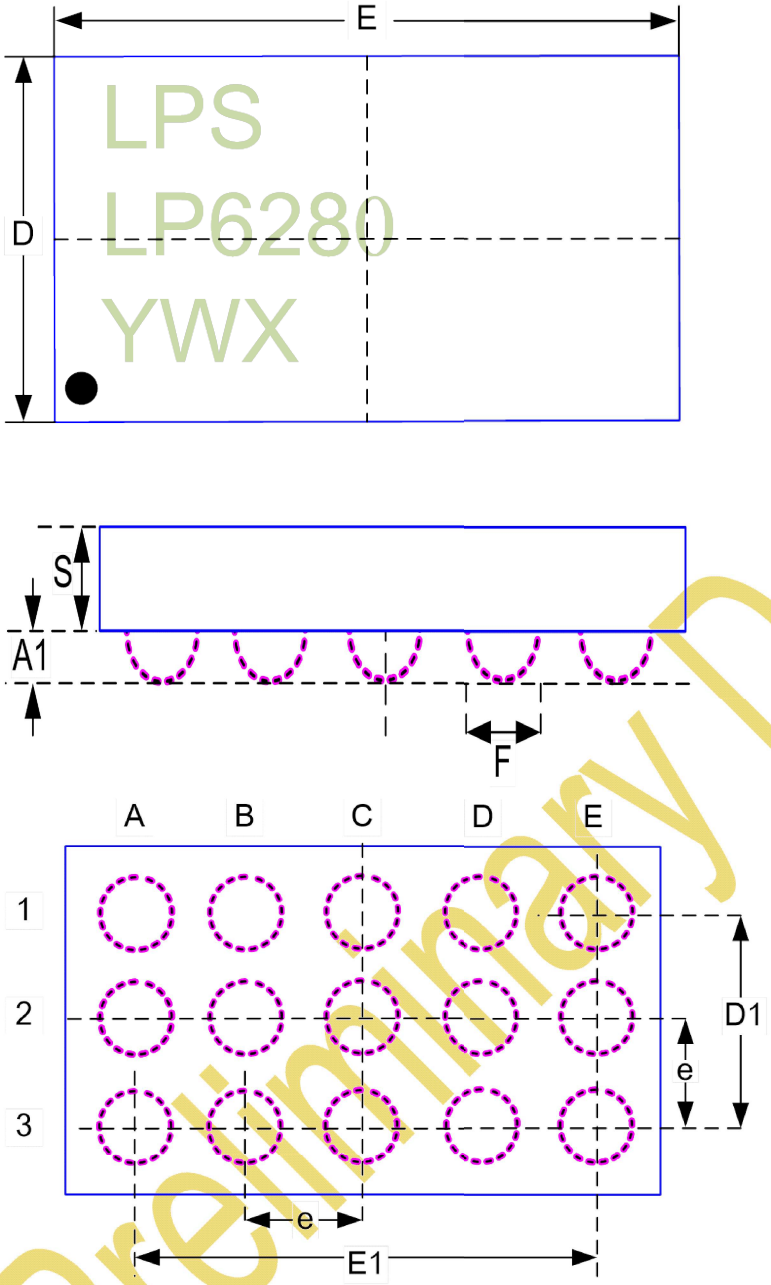


Figure 13. PCB Layout Example

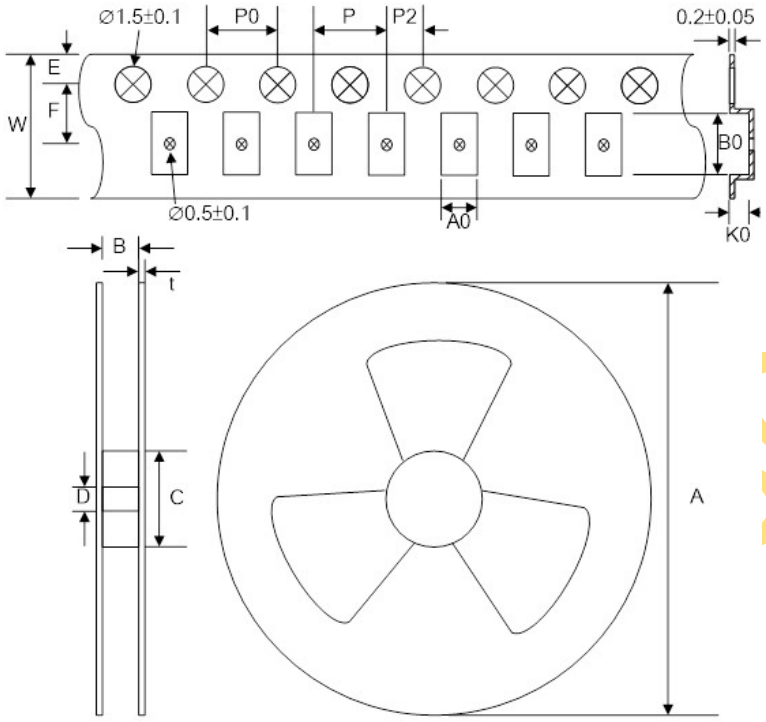
Package Information

WLCSP-15-ball Package (1.17×1.94) pitch 0.4 (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
D	1.145	1.185
E	1.915	1.955
S	0.402	0.428
D1	0.750	0.850
E1	1.550	1.650
A1	0.165	0.205
F	0.210	0.250
e	0.4	

Carrier information



Device	Package Type		Pins	SPQ	A (mm)	B (mm)	C (mm)	D (mm)	t (mm)
LP6280A	WLCSP		15	3000	ø180±1	9.5±0.5	ø60±1	ø13±0.2	1.1±0.25
	W (mm)	E (mm)	F (mm)	P (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P2 (mm)
	8±0.3	1.75±0.1	3.5±0.05	4	1.82±0.05	2.74±0.05	0.75±0.05	4	2