200mA,Ultra-low Noise LDO Regulator

General Description

The LP3993B is designed for portable applications with demanding performance and space requirements. The LP3993B performance is optimized for high voltage systems to deliver ultralow noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the input system life. The LP3993B also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The other features include ultralow dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

Features

- Ultra-Low-Noise for RF Application
- Input Voltage up to 28V
- Low Dropout : 300mV @ 100mA
- Output Current 200mA
- Ultra-Fast Response in Line/Load Transient
- Current Limiting and Thermal Shutdown Protection

Applications

- PMP/PDA/MP3 players
- Cellular and Mobile phone
- RF Module
- Sensor Module

Order Information

LP3993B □ □ □ □ □

F: Pb-Free

Package Type

X3: SOT89-3

Output Type

28: 2.8V

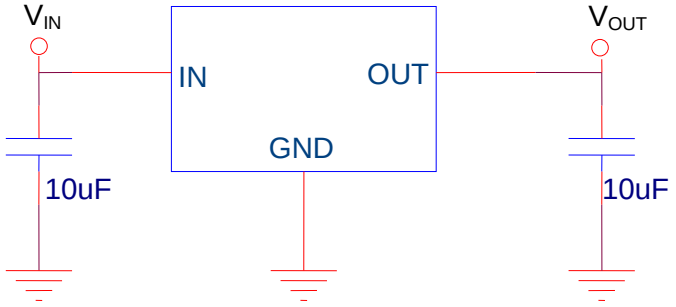
30: 3.0V

33: 3.3V

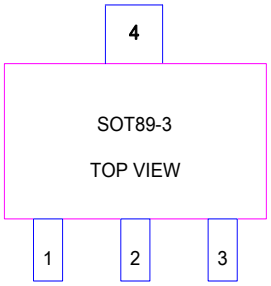
36: 3.6V

50: 5.0V

Typical Application Circuit



Functional Pin Description

Package Type	Pin Configurations
SOT89-3	

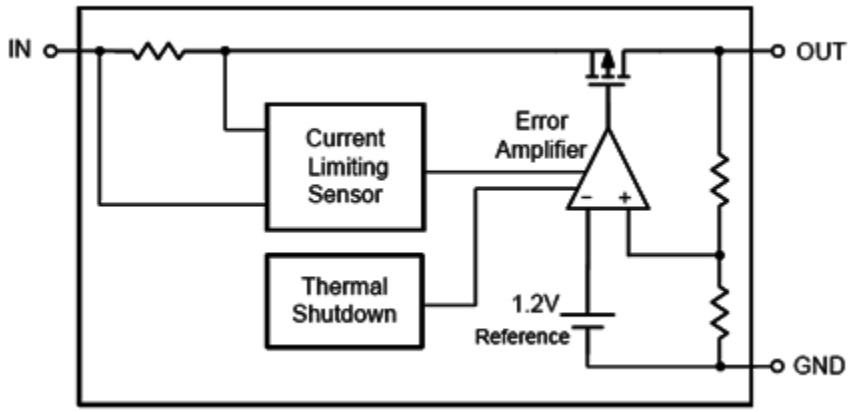
Pin Description

Pin	Name	Description
1	OUT	Output Pin.
2/4	GND	Ground.
3	IN	Power Input Pin

Marking Information

Device	Marking	Package	Shipping	Device	Marking	Package	Shipping
LP3993B-28X3F	LPS 3993B 28YW	SOT89-3	1K/REEL	LP3993B-33X3F	LPS 3993B 33YW	SOT89-3	1K/REEL
LP3993B-30X3F	LPS 3993B 30YW	SOT89-3	1K/REEL	LP3993B-36X3F	LPS 3993B 36YWX	SOT89-3	1K/REEL
LP3993B-50X3F	LPS 3993B 50YW	SOT89-3	1K/REEL				
Marking indication: Y:Production year W:Production week X: Series Number							

Function Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ---------- -0.3V to 32V
- ✧ Other pin to GND ---------- -0.3V to 8V
- ✧ Maximum Junction Temperature ---------- 150°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C
- ✧ Operating Junction Temperature Range (T_J) ---------- -40℃ to 150°C
- ✧ Storage Temperature ---------- -60℃ to 125°C

Power Dissipation, PD @ TA = 25°C

- ✧ SOT89-3 ---------- 700mW

Package Thermal Resistance

- ✧ SOT89-3, θ_{JA} ---------- 165°C/W

ESD Susceptibility

- ✧ HBM (Human Body Mode) ---------- 2kV
- ✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

- ✧ Supply Input Voltage ---------- V_{OUT}+1V to 28V

Electrical Characteristics

(C_{IN} = 10μF, C_{OUT} =10uF，V_{IN}=V_{OUT}+1V，Ta = 25° C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Units
Output Voltage Accuracy	ΔV_{OUT}	I_{OUT} = 1mA	−1	--	+1	%
Output Loading Current	I_{OUT}			200		mA
Current Limit	I_{LIM}	V_{OUT} = 0.9*$V_{OUT(nom)}$	250			
Quiescent Current	I_Q	No Load	2.5	4.5	6.5	μA
Dropout Voltage	V_{DROP}	I_{OUT} = 100mA, V_{OUT} =3.3V	—	300	500	mV
Linear Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{IN} = (V_{OUT} + 1V) to 12V, I_{OUT} = 1mA.	—	0.2	0.4	%
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	1mA < I_{OUT} < 150mA			2	%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			25		°C

Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3993B must be carefully selected for regulator stability and performance. Using a capacitor whose value is ≥ 10μF on the LP3993B input. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDO's application. The LP3993B is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 10μF with ESR is > 25mΩ on the LP3993B output ensures stability. The LP3993B still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the LP3993B and returned to a clean analog ground.

Thermal Considerations

Thermal protection limits power dissipation in LP3993B. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C.

The power dissipation definition in device is:

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction and ambient.

The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3993B, the junction to ambient thermal resistance (θ_{JA} is layout dependent) for LP3993B showed below.

SOT89-3 : 165℃/W

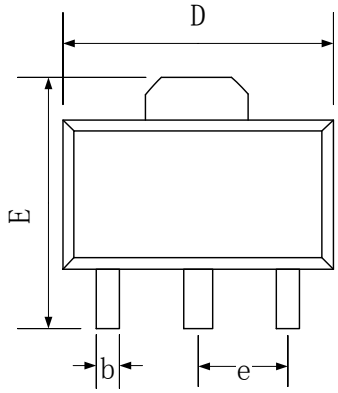
And ,

P_D=(125°C−25°C)/165℃/W= 600mW (SOT89-3)

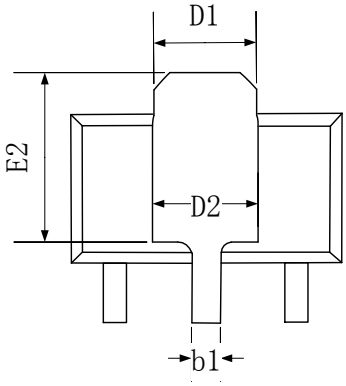
The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}.

Packaging Information

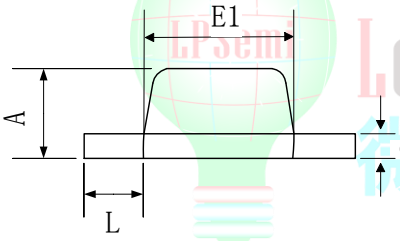
SOT-89



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.40	1.50	1.60
b	0.32	0.42	0.52
b1	0.36	0.48	0.56
c	0.35	-	0.44
D	4.39	4.50	4.60
D1	1.55 REF		
D2	1.63 REF		
E	3.9	4.20	4.40
E1	2.30	2.45	2.60
E2	2.75 REF		
e	1.50 BSC		
L	0.78	1.00	1.20

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