300mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3990A is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3990A performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. The LP3990A also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3990A consumes less than 1μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 1mm×1mm TDFN-4 packages.

Features

- Ultra-thin Package
- 2.5V- 5.5V Input Voltage Range
- Low Dropout : 240mV @ 300mA
- 1.2V, 1.5V, 1.8V, 2.5V, 2.8V,3.0V,3.3V and 5V Fixed
- 300mA Output Current, 450mA Peak Current
- High PSRR:-75dB at 1KHz
- 1uA Standby Current When Shutdown
- Available in 1mm×1mm TDFN-4 Package
- TTL-Logic-Controlled Shutdown Input
- Ultra-Fast Response in Line/Load transient
- Current Limiting and Thermal Shutdown Protection
- Quick start-up (typically 50uS)

Order Information

LP3990A □□ □□ □

F: Pb-Free

Package Type

QV: TDFN-4(1*1)

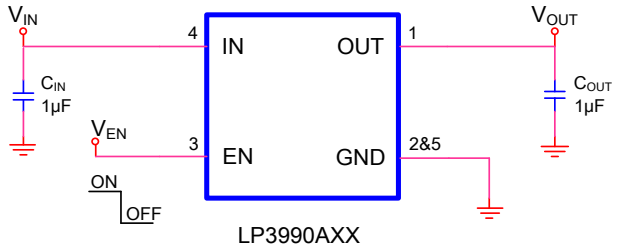
Output Voltage Type

12 : 1.2V
15 : 1.5V
18 : 1.8V
25 : 2.5V
28 : 2.8V
30 : 3.0V
33 : 3.3V
50 : 5.0V

Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Typical Application Circuit

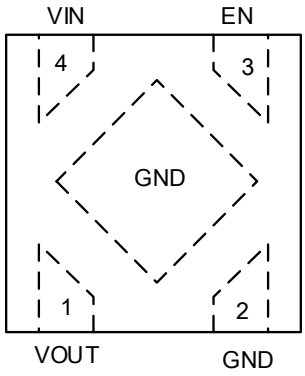


Marking Information

Device	Marking	Package	Shipping
LP3990A-18QVF	CWX	TDFN-4	12K/REEL
LP3990A-28QVF	HWX	TDFN-4	

Device	Marking	Package	Shipping
LP3990A-33QVF	EWX	TDFN-4	12K/REEL
W: W is week code. X: X is series number.			

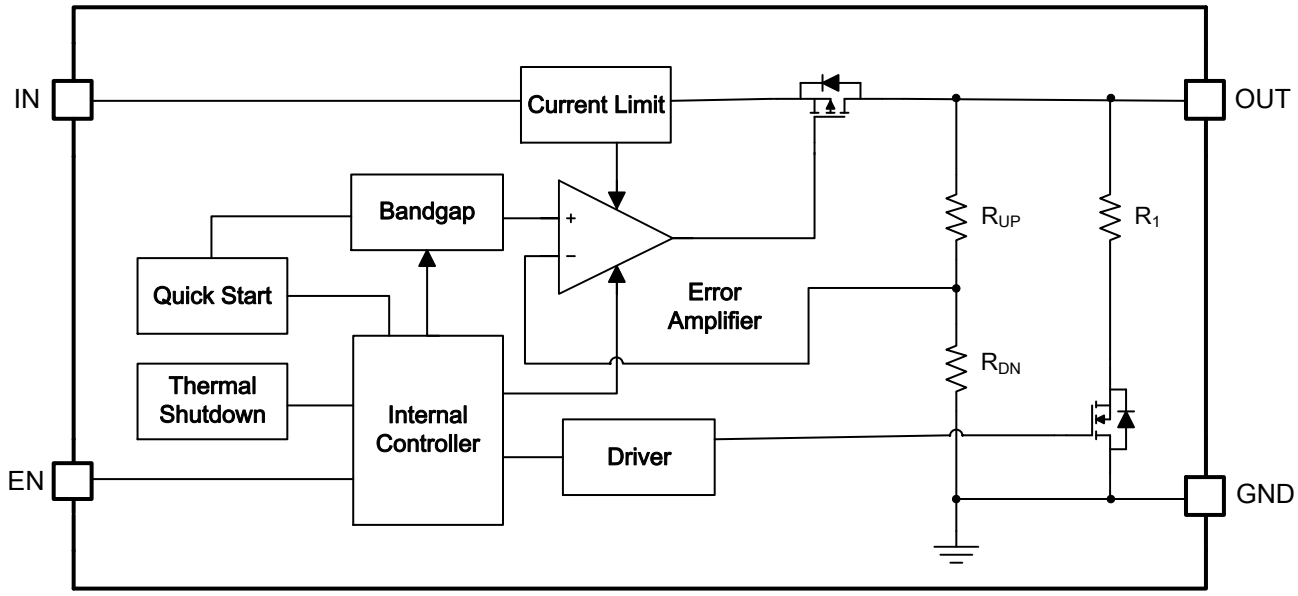
Functional Pin Description

Package Type	Pin Configurations
1mm×1mm TDFN-4	

Pin Description

Pin	Name	Description
1	VOUT	Output Voltage.
2	GND	Ground.
3	EN	Chip Enable (Active High). Note that this pin is high impedance.
4	VIN	Power Input Voltage.

Function Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ---------- -0.3V to 6V
- ✧ EN Pin Voltage ---------- -0.3V to Vin+0.3V

Power Dissipation, PD @ TA = 25° C

- ✧ TDFN-4 ---------- 390mW

Package Thermal Resistance

- ✧ TDFN-4, θJA ---------- 256°C/W
- ✧ Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ✧ Storage Temperature Range ---------- −60°C to 125°C

ESD Susceptibility

- ✧ HBM (Human Body Mode) ---------- 2kV
- ✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

- ✧ Supply Input Voltage ---------- 2.5V to 5.5V
- ✧ EN Input Voltage ---------- 0V to 5.5V
- ✧ Operation Junction Temperature Range ---------- −20°C to 125°C
- ✧ Operation Ambient Temperature Range ---------- −20°C to 85°C

Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1μF, TA = 25° C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Units
Output Voltage Accuracy		ΔVOUT	IOUT = 1mA	−3	--	+3	%
Output Loading Current		I_{LOAD}	VEN=VIN,VIN>2.5V		300		mA
Current Limit		ILIM	RLOAD = 1Ω	350	450		mA
Quiescent Current		IQ	VEN ≥ 1.4V, IOUT = 0mA		50		μA
Dropout Voltage		VDROP	IOUT = 200mA, VOUT > 2.8V		160	200	mV
			IOUT = 300mA, VOUT > 2.8V		240	300	
Line Regulation		ΔVLINE	VIN = (VOUT + 1V) to 5.5V, IOUT = 1mA			0.2	%
Load Regulation		ΔLOAD	1mA < IOUT < 200mA			2	%
Standby Current		ISTBY	VEN = GND, Shutdown		1		μA
EN Input Bias Current		IIBSD	VEN = GND or VIN		2		μA
EN Threshold	Logic-Low Voltage	VIL	VIN = 3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	VIH	VIN = 3V to 5.5V, Start-Up	1.4			
Output Noise Voltage			10Hz to 100kHz, IOUT = 200mA, COUT = 1μF		100		uVRMS
Power Supply Rejection Rate	f = 1kHz	PSRR	C_{OUT} = 1μF, I_{OUT} = 10mA		-75		dB
	f = 10kHz				−68		
Thermal Shutdown Temperature		TSD			150		°C

Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3990A must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LP3990A input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3990A is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LP3990A output ensures stability. The LP3990A still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP3990A and returned to a clean analog ground.

Start-up Function Enable Function

The LP3990A features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the LP3990A have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in LP3990A. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C.

The power dissipation definition in device is:

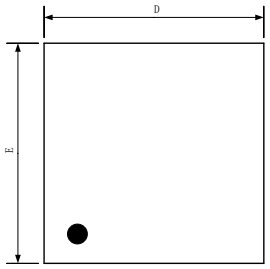
$$PD = (VIN-VOUT) \times IOUT + VIN \times IQ$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

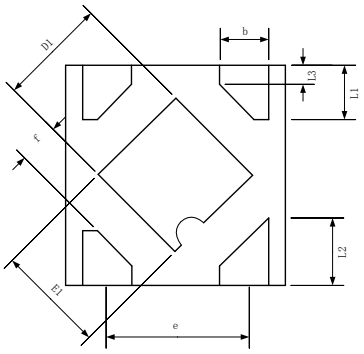
The maximum power dissipation can be calculated by following formula:

$$PD(MAX) = (TJ(MAX) - TA) / \theta JA$$

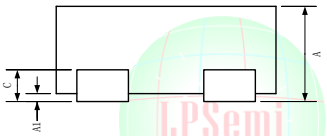
Packaging Information



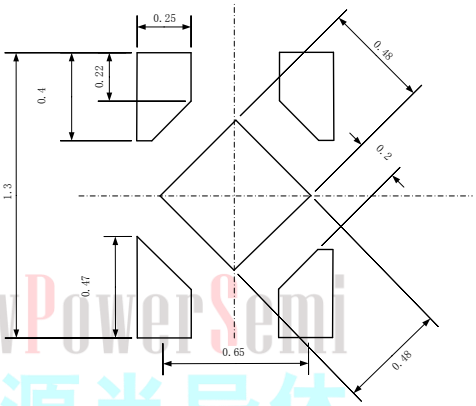
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.07	0.12	0.17
D	0.95	1.00	1.05
D1	0.43	0.48	0.55
E	0.95	1.00	1.05
E1	0.43	0.48	0.55
e	0.65BSC		
L1	0.2	0.25	0.30
L2	0.27	0.32	0.37
L3	0.09REF		
f	0.18REF		