1A Single Chip Li-Ion and Li-Polymer Charger

General Description

The LP4069PT is a complete constant-current/ constant voltage linear charger for single cell lithium-ion battery. No external sense resistor is needed, and no blocking diode is required due to the internal MOSFET architecture. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature. The charge voltage is fixed at V_{FLOAT}, and the charge current can be programmed externally by ISET pin with a single resistor.

The LP4069PT automatically terminates the charge cycle when the charge current drops to 1/10 setting current value after the final float voltage is reached.

Other features include charge current monitor, under voltage lockout, automatic recharge, status pins.

Order Information

LP4069PT □□ □-□□

- Battery Voltage
  Default: 4.2V
  44: 4.4V
- F: Pb-Free
- Package Type
  QV: TDFN-8

Features

- Input Over Voltage Protection：6.3V
- Short-circuit protection
- Programmable Charge Current up to 1A
- 1μA Battery Reverse Current
- Protection of Reverse Connection of Battery
- No MOSFET, Sense Resistor or Blocking Diode Required
- Constant-Current/Constant-Voltage Operation with Thermal Regulation
- TDFN-8 Package
- RoHS Compliant and 100% Lead (Pb)-Free

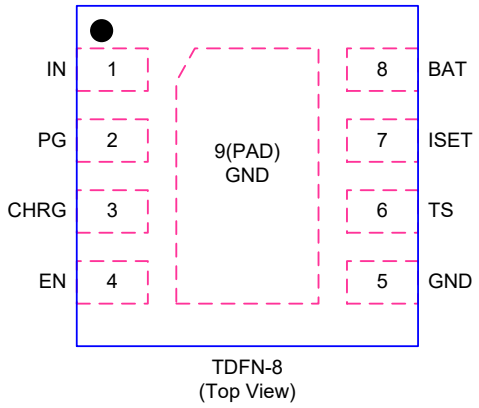
Applications

- Portable Media Players/Game
- Power Bank
- Bluetooth Applications
- PDA/MID

Marking Information

Device	Marking	Package	Shipping
LP4069PTQVF	LP4069 PTYWX	TDFN-8	4K/REEL
LP4069PTQVF-44	LP4069 PT44YW	TDFN-8	4K/REEL
Marking indication: Y:Production year W:Production week			

Functional Pin Description

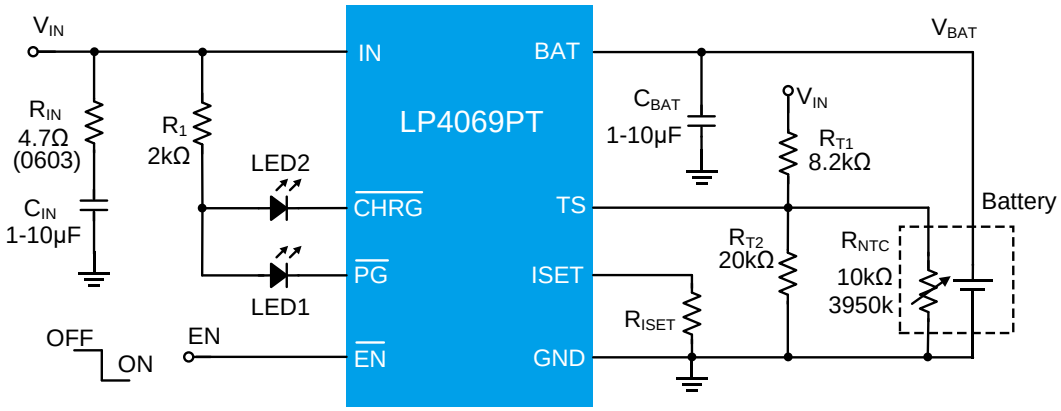
Package Type	Pin Configurations
TDFN-8	

TDFN-8
(Top View)

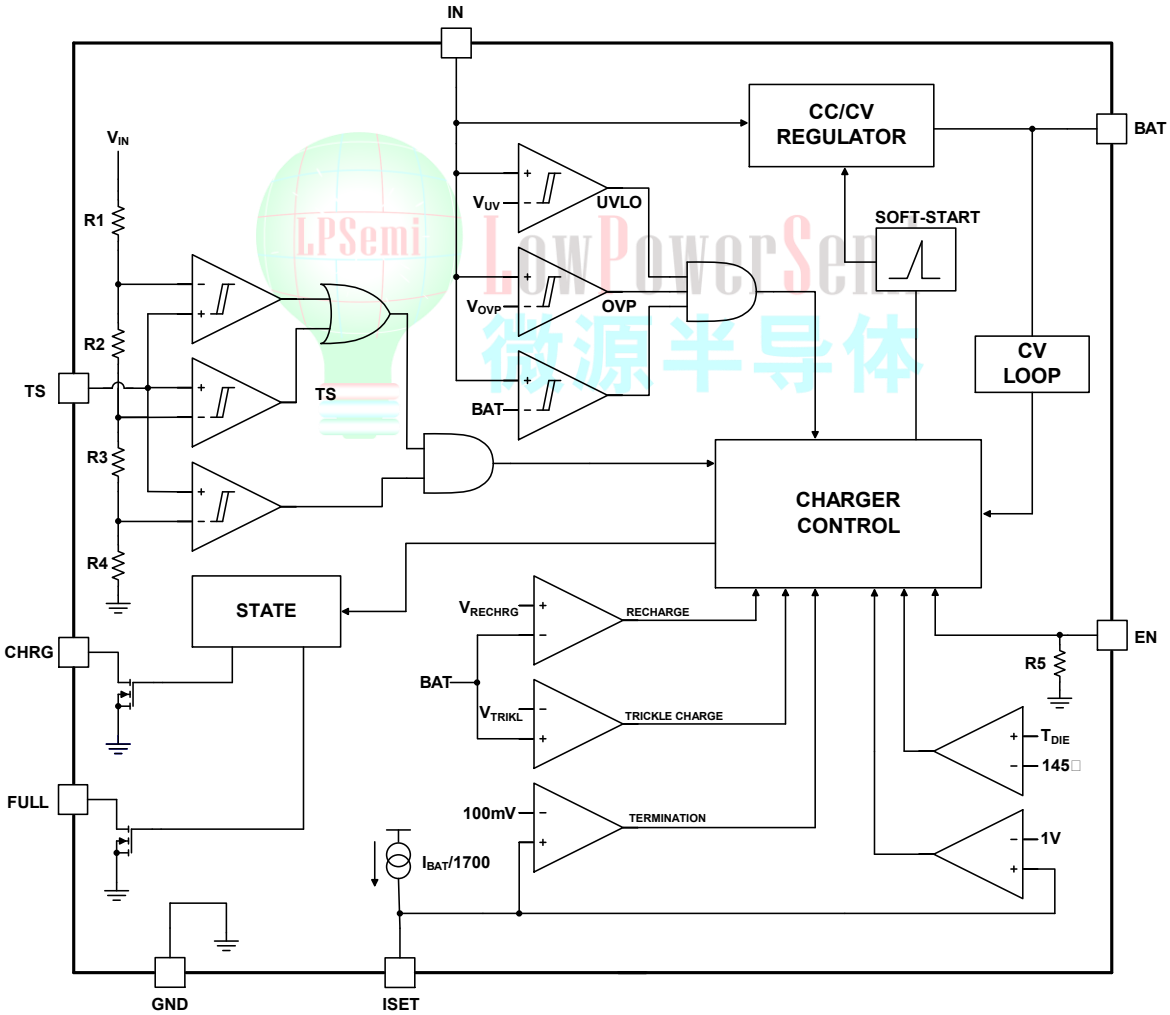
Pin Description

No.	NAME	DESCRIPTION
1	IN	IN is the input power source. Connect to a wall adapter.
2	PG	Open-Drain Status Output. Low indicates the input voltage is above the input UVLO voltage and the OUT (battery)+150mV voltage, and lower than OVP threshold.
3	CHRG	Open-Drain Charge Status Output. When the battery is charging, the CHRG pin is pulled low by an internal N-MOS. When the charge cycle is completed, the pin could be pulled High by an external pull high resistor.
4	EN	Charge Enable Input (active low).
5	GND	GND is the connection to system ground.
6	TS	Temperature Senses Voltage Input. This pin senses the temperature of the battery pack and stops the charger when the temperature is out of range. Connect to GND for disabling this function.
7	ISET	Charge Current Program. The charge current is programmed by connecting a 1% resistor(R_{ISET}) to ground. $$I_{BAT} = \frac{1700 \times V_{ISET}}{R_{ISET}}$$
8	BAT	BAT is the connection to the battery. Typically a 10μF Tantalum capacitor is needed for stability when there is no battery attached.
9	PAD	Exposed Pad,use to strengthen dissipation of heat.It usually connect to GND.

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings Note 1

- ✧ Input Voltage to GND ---------- -0.3V to 28V
- ✧ BAT Voltage GND ---------- - 5V to 15V
- ✧ Other pin to GND ---------- -0.3V to 6.5V
- ✧ Maximum Junction Temperature(T_J) ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
- ✧ Operating Junction Temperature Range ---------- -20℃ to 85℃
- ✧ Storage Temperature ---------- -60℃ to 125℃

Thermal Information

- ✧ Maximum Power Dissipation (P_D,T_A=25°C) ---------- 1.2W
- ✧ Thermal Resistance (θ_{JA}) ---------- 95℃/W

ESD Susceptibility

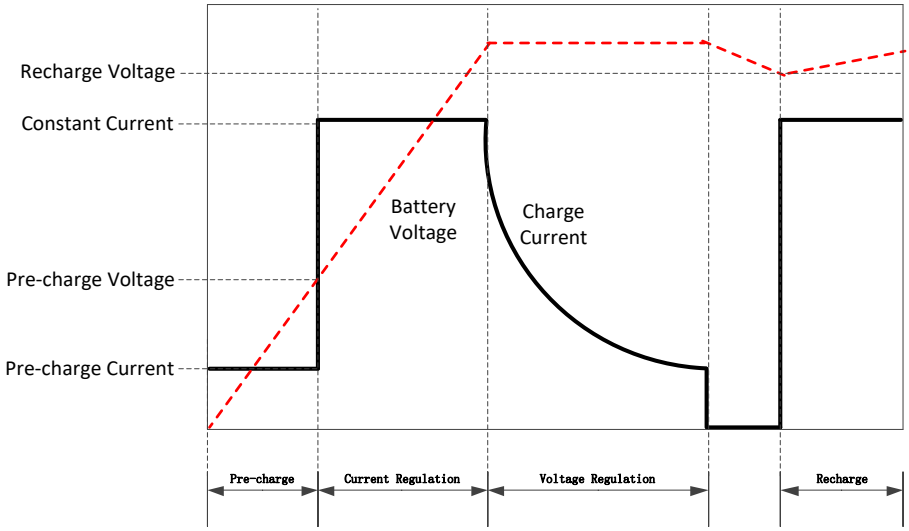
- ✧ HBM(Human Body Model) ---------- 2KV
- ✧ MM(Machine Model) ---------- 200V

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (T_A=25°C, V_{IN} =5V, unless otherwise noted.)

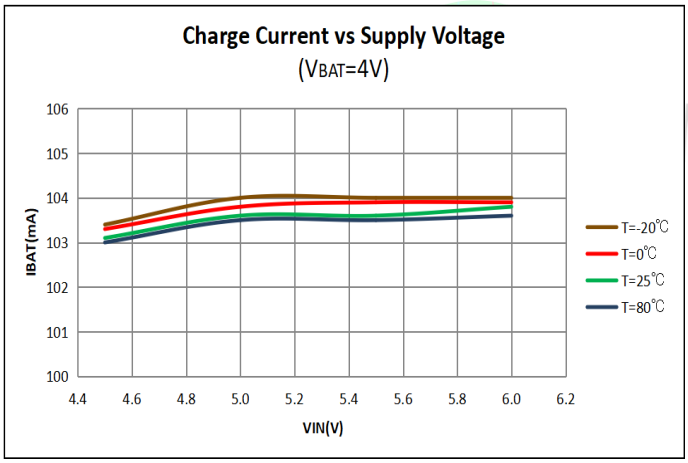
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
V_{IN}	Input Voltage		4.5	5	5.5	V
I_{IN}	Input Supply Current	R_{ISET}=17K,Charge Mode		300		uA
		V_{BAT}=4.4V, Charge Terminated		160		uA
		R_{ISET}=NC,Shutdown Mode		200		uA
V_{FLOAT}	Regulated Output (Float) Voltage	I_{BAT}=40mA	4.158	4.2	4.242	V
			4.356	4.4	4.444	V
V_{UV}	VIN Under Voltage Lockout Threshold	V_{IN} Rising		3.5		V
V_{UV_HYS}	Under Voltage Lockout Hysteresis			140		mV
V_{OVP}	Input Voltage OVP	V_{IN} Rising	6	6.3	7.5	V
V_{OVP_HYS}	OVP Hysteresis			150		mV
I_{BAT}	BAT Pin Current	R_{ISET}=3.4k, Current Mode	450	500	550	mA
		R_{ISET}=17k, Current Mode	90	100	110	mA
		V_{BAT}=4.2V（V_{IN}=Float or 0V）		-1		uA
I_{TRIKL}	Trickle Charge Current	V_{BAT}<V_{TRIKL}, R_{ISET}=10k, Charge Mode		40		%I_{BAT}
V_{TRIKL}	Trickle Charge Threshold Voltage	V_{BAT} Rising		2.6		V
$V_{TRIKL-HYS}$	Trickle Charge Hysteresis Voltage			150		mV
I_{TERM}	Termination Current Threshold			10		%I_{BAT}
V_{ISET}	ISET Pin Voltage	R_{ISET}=10k, Current Mode	0.9	1	1.1	V
I_{STAT}	CHRG Pin Sink Current	V_{CHRG}=5V			5	uA
V_{STAT}	CHRG Pin Output Low Voltage	I_{CHRG}=5mA			0.5	V
I_{PG}	PG Pin Sink Current	V_{CHRG}=5V			5	uA
V_{PG}	PG Pin Output Low Voltage	I_{CHRG}=5mA			0.5	V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT}-V_{RECHRG}		150		mV
V_{ASD}	V_{IN} - V_{BAT} Lockout Threshold Voltage	V_{BAT}=3.5V,V_{IN} Rising		150		mV
V_{EN_ON}	EN Logic-Low Voltage Threshold				0.4	V
V_{EN_OFF}	EN Logic-High Voltage Threshold		1.4			V
V_{TS_H}	TS high temperature threshold			30		%V_{IN}
V_{TS_L}	TS low temperature threshold			60		%V_{IN}
V_{TS_HYS}	TS Hysteresis Voltage			90		mV
V_{TS_DIS}	TS disable Threshold				0.2	V
T_{LIM}	Junction Temperature in Constant Temperature Mode			145		°C

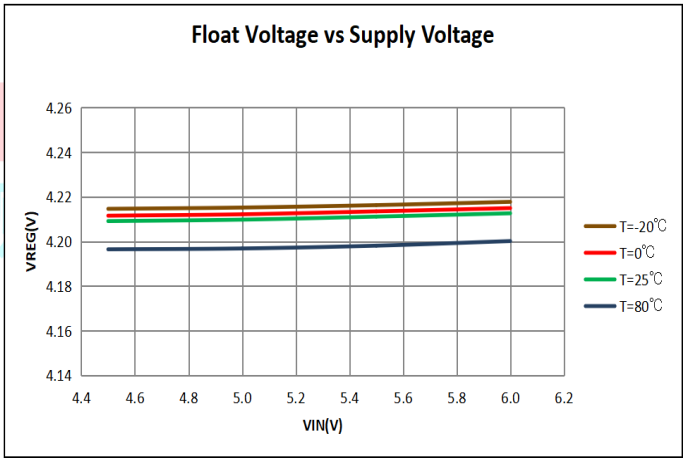
Typical Charging Profile

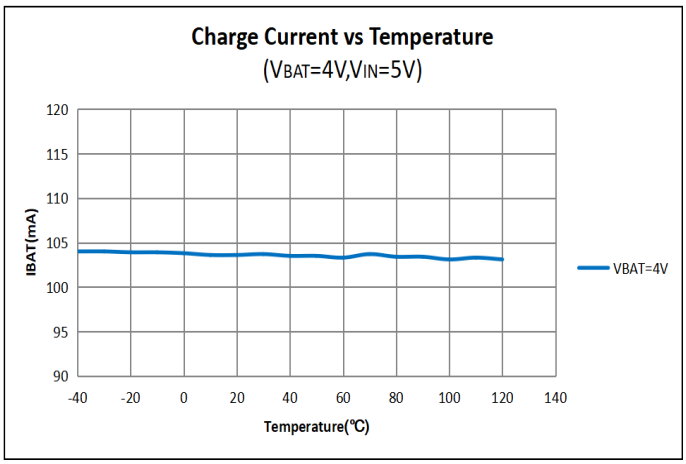


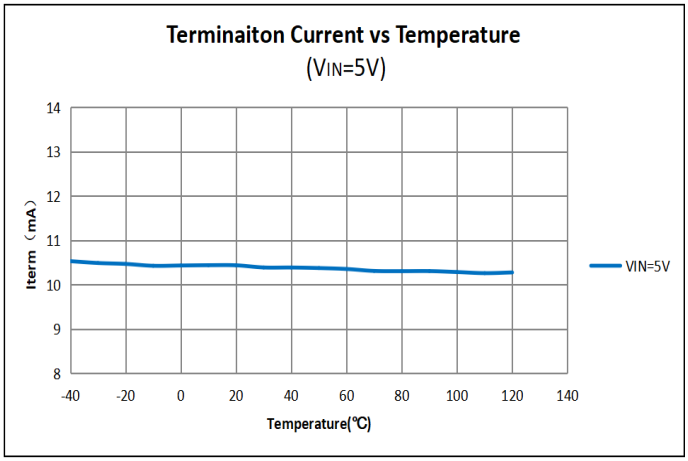
Typical Performance Characteristics

(CIN=COUT=10uF,RISET=16.5K, unless otherwise noted)









Application Information

The LP4069PT has built-in input voltage surge protection as high as +28V. The charger IC will be automatically disabled when the input voltage is higher than 7V. A charge cycle begins when EN is high, the voltage at the IN pin rises above the UVLO threshold level and a program resistor is connected from the ISET pin to ground. If the BAT pin is less than 2.6V, the charger enters trickle charge mode. In this mode, the LP4069PT supplies approximately 4/10 the ISET programmed charge current to bring the battery voltage up to a safe level for full current charging. When the BAT pin voltage rises above 2.6V, the charger enters constant-current mode(CC), where the ISET programmed charge current is supplied to the battery. When the Battery Voltage approaches the final float voltage, It enters constant-voltage mode(CV) and the charge current begins to decrease, and the battery full indication is set when the charge current in the CV mode is reduced to the programmed full battery current (1/10).

Charge Termination

A charge cycle is terminated when the charge current falls to 1/10th the ISET programmed value after the final float voltage is reached. This condition is detected by using an internal, filtered comparator to monitor the ISET pin. When the ISET pin voltage falls below 100mV for longer than t_{TERM} (typically 1ms), charging is terminated.

Charge Current Program

The charge current (I_{BAT}) is set by a resistor (R_{ISET}) connecting from the ISET pin to GND. The relationship of the charge current and the programming resistance is established by the following equations（V_{ISET}=1V）.

$$I_{BAT} = \frac{1700 \times V_{ISET}}{R_{ISET}}$$

Automatic Recharge

Once the charge cycle is terminated, the LP4069PT continuously monitors the voltage on the BAT pin. A charge cycle restarts when the battery voltage falls below 4.05V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at or near a fully charged condition and eliminates the need for periodic charge cycle initiations.

Charge Status Indicator (CHRG/PG)

When the input voltage is above the UVLO and above the battery voltage +150mV（VIN>VBAT+150mV），and lower than OVP (VIN<VOVP)，the PG internal NMOS turns on and provides a low impedance path to ground.

Function	PG
$V_{IN}<V_{UVLO}$	Hi-Z
$V_{UVLO}<V_{IN}<V_{OVP}$	Low
$V_{OVP}<V_{IN}$	Hi-Z

CHRG has two different states: pull-down ~5mA maximum sink current) to GND and high impedance. The pull-down state indicates that the LP4069PT is in a charge cycle. when the charge current decreases to the battery termination charge current threshold (IBF) ,the CHRG pin will become high impedance. After application of a 5V source, the input

Function	CHRG	FULL
Charging	Low	Hi-Z
Charge Finish	Hi-Z	Low

Thermal Limit

An internal thermal feedback loop reduces charge current if junction temperature attempts to rise above a preset value of approximately 145°C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.

Battery Temperature Detection

An internal resistor divider sets the low temperature threshold (V_{TS_L}) and high temperature threshold (V_{TS_H}) at 60% of V_{IN} and 30% of V_{IN}, respectively. For a given TS thermistor, select an appropriate R_{T1} and R_{T2} to set the TS window with following equation:

$$\frac{V_{TS\_L}}{V_{IN}} = \frac{R_{T2} \parallel R_{TS\_COLD}}{R_{T1} + R_{T2} \parallel R_{TS\_COLD}} = T_L = 60\%$$

$$\frac{V_{TS\_H}}{V_{IN}} = \frac{R_{T2} \parallel R_{TS\_HOT}}{R_{T1} + R_{T2} \parallel R_{TS\_HOT}} = T_H = 30\%$$

Where R_{TS_HOT} is the value of the TS resistor at the upper bound of its operating temperature range, and R_{TS_COLD} is its lower bound. The two resistors R_{T1} and R_{T2} determine the upper and lower temperature limits independently. This flexibility allows the IC to operate with most TS resistors for different temperature range requirements. Calculate R_{T1} and R_{T2} with following equation:

$$R_{T1} = \frac{R_{TS\_HOT} \times R_{TS\_COLD} \times (T_L - T_H)}{T_H \times T_L \times (R_{TS\_COLD} - R_{TS\_HOT})}$$

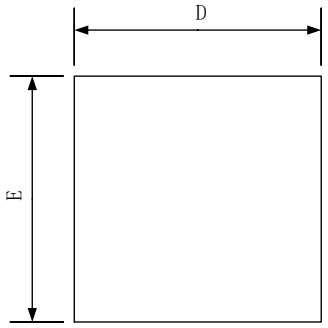
$$R_{T2} = \frac{R_{TS\_HOT} \times R_{TS\_COLD} \times (T_L - T_H)}{(1 - T_L) \times T_H \times R_{TS\_COLD} - (1 - T_H) \times T_L \times R_{TS\_HOT}}$$

Connect this pin to GND or set the voltage of pin under V_{TS_DIS}, can disable TS function

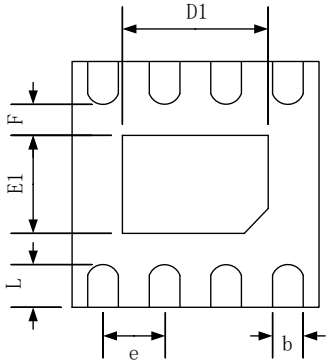
LPSemi LowPowerSemi 微源半导体

Packaging Information

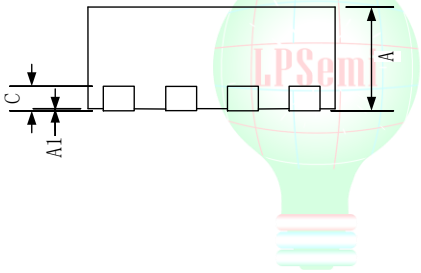
TDFN-8



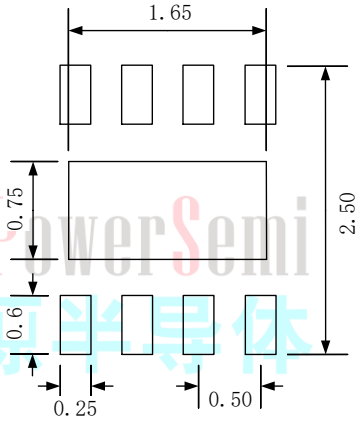
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c		0.20 REF	
D	1.90	2.00	2.10
D1	1.10	1.30	1.65
E	1.90	2.00	2.10
E1	0.60	0.75	0.85
e		0.50 BSC	
L	0.25	0.35	0.40
F	0.25	0.30	0.35