300mA Standalone Linear Li-Ion Battery Charger

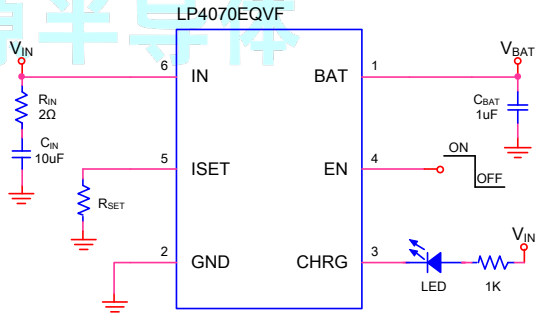
General Description

The LP4070E is a complete constant-current/constant-voltage linear charger for single cell lithium-ion batteries. Its TDFN-6 package and low external component count make the LP4070E ideally suited for portable applications. Furthermore, the device operates from either a USB port or AC adapter. Due to the internal MOSFET architecture,No external sense resistor is needed and no blocking diode is required.Thermal feedback prevents overheating by regulating the charge current to limit the die temperature during high power operation or high ambient temperature conditions.The charge voltage is preset at 4.2V/4.35V and the charge current can be programmed up to 300mA externally with a single resistor. The LP4070E automatically terminates the charge cycle when the charge current drops to 10% programmed value after the final float voltage is reached. When the input supply (wall adapter or USB supply) is removed, the LP4070E automatically enters a low current state, dropping the battery drain current to less than 1μA. Other features include charge current monitor, automatic recharge and charge status indications.

Features

- Operating input voltage from 3.9 V to 6 V
- Programmable Charge Current Up to 300mA
- No MOSFET, Sense Resistor or Blocking Diode Required
- Constant-Current/Constant-Voltage Operation with Thermal Regulation to Maximize Charge Rate Without Risk of Overheating
- Preset 4.2V/4.35V Charge Voltage with ±1% Accuracy
- Reverse Leakage Protection Prevents Battery Drainage
- Low Battery Leakage Current (less than 1 μA)
- 2.9V Trickle Charge Threshold
- Automatic Recharge
- C/10 Charge Termination
- Output OCP
- Available in a Low Profile TDFN-6 (1*1mm) Package

Typical Application Circuit



Order Information

LP4070E □□ □ □□

- Battery Voltage
  - Default: 4.2V
  - 435: 4.35V
- F: Pb-Free
- Package Type
  - QV: TDFN-6

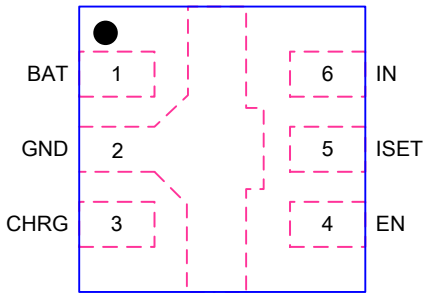
Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- PDA/DSC
- Bluetooth Applications

Marking Information

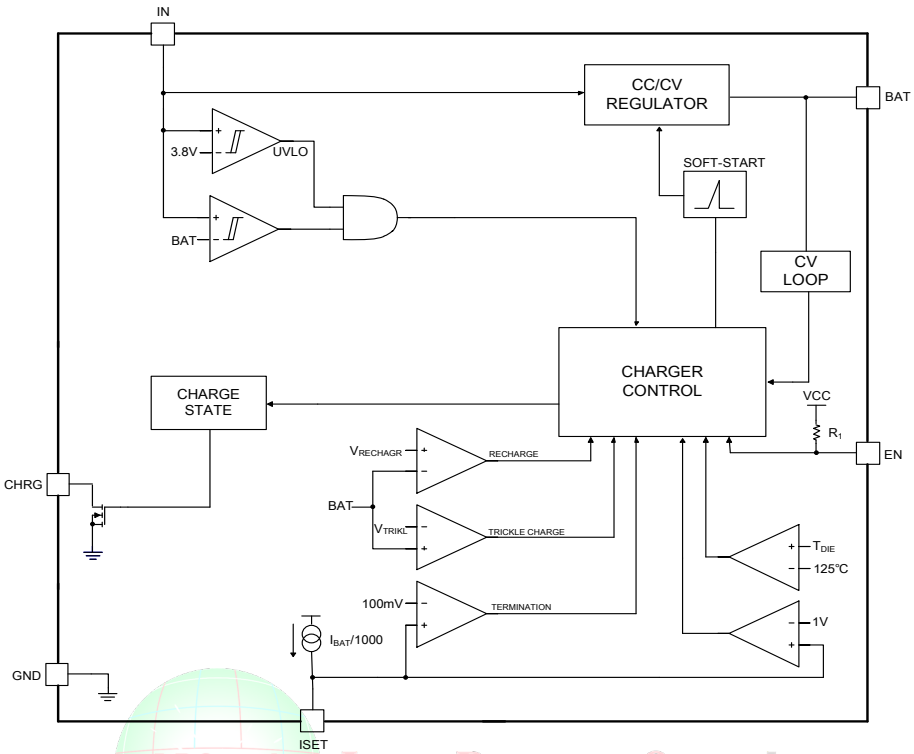
Device	Marking	Package	Shipping
LP4070EQVF	BVX	TDFN-6	12K/REEL
Marking indication: X:Production batch.			

Functional Pin Description

Package Type	Pin Configuration
TDFN-6 (1*1mm)	Top View  DFN-6 (Top View)

Pin	Name	Description
1	BAT	Charge Current Output. Provides charge current to the battery and regulates the final float voltage to 4.2V/4.35V. An internal precision resistor divider from this pin sets the float voltage.
2	GND	Ground.
3	CHRG	Open-Drain Charge Status Output. When the battery is charging, the CHRG pin is pulled low by an internal N-channel MOSFET. When the LP4070E detects an under voltage lockout condition or charge complete, CHRG is forced high impedance.
4	EN	Chip Enable Pin. Charging when the pin is floating or connected to a high voltage. Discharge when the pin pull low.
5	ISET	Charge Current Program and Charge Current Monitor Pin. The charge current is programmed by connecting a 1% resistor, R_{ISET}, to ground. When charging in constant-current mode, this pin servos to 1V. In all modes, the voltage on this pin can be used to measure the charge current using the following formula: IBAT=1000/R_{ISET}
6	IN	Positive Input Supply Voltage.

Functional Block Diagram



Absolute Maximum Ratings Note1

- ✧ Input to GND(IN) ---------- -0.3V to 8V
- ✧ BAT to GND(BAT) ---------- -5V to 8V
- ✧ Other Pin to GND ---------- -0.3V to 6V
- ✧ BAT Short-circuit Duration ---------- Continuous
- ✧ Maximum Junction Temperature (T_J) ---------- 125℃
- ✧ Operating Junction Temperature Range ---------- -20℃ to 85℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
- ✧ Storage Temperature Range ---------- -60℃ to 125℃

Note1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (P_D,T_A=25°C) ---------- 0.39W
- ✧ Thermal Resistance (TDFN-6, θ_{JA}) ---------- 256℃/W

ESD Susceptibility

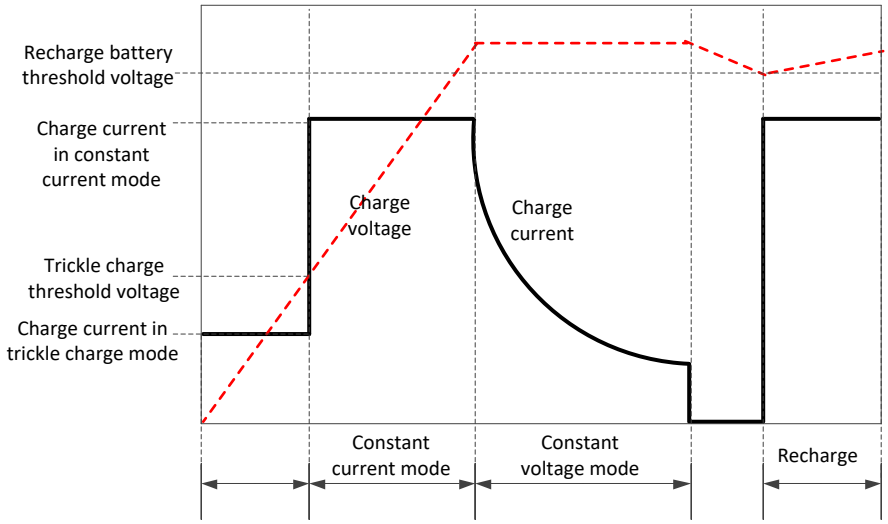
- ✧ HBM(Human Body Model) ---------- 2KV
- ✧ MM(Machine Model) ---------- 200V

Electrical Characteristics

(T_A = 25℃. V_{IN} = 5V, unless otherwise noted.)

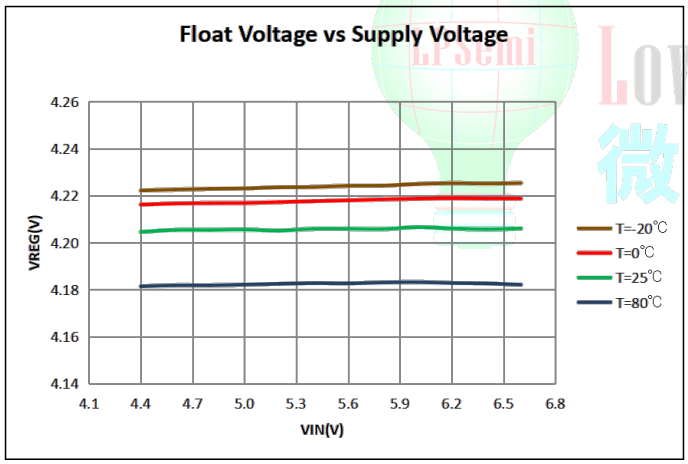
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
V_{IN}	Adapter/USB Voltage Range		3.9	5	6	V
I_{IN}	Input Supply Current	Charge Mode, R_{ISET}= 10K		200	1000	uA
		Standby Mode (Charge Terminated)		50		
V_{FLOAT}	Regulated Output (Float) Voltage	LP4070EQVF, I_{BAT} = 40mA	4.158	4.2	4.242	V
		LP4070EQVF435, I_{BAT} = 40mA	4.307	4.35	4.394	V
I_{BAT}	BAT Pin Current	R_{ISET} = 10K，Current Mode	85	100	115	mA
		R_{ISET} = 3.3K，Current Mode	255	300	345	
		Standby Mode, V_{BAT} = 4.2V Sleep Mode, V_{IN} = 0V	0	0.1	±1	uA
V_{TRIKL}	Trickle Charge Threshold Voltage	R_{ISET} = 10k, V_{BAT} Rising		2.9		V
V_{TRHYS}	Trickle Charge Hysteresis Voltage	R_{ISET} = 10K		100		mV
I_{TRIKL}	Trickle charge current	V_{BAT} < V_{TRIKL}, R_{ISET} =10K		80		mA
		V_{BAT} < V_{TRIKL}, R_{ISET}=3.3K		200		
V_{UV}	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising	3.7	3.8	3.9	V
V_{UVHYS}	V_{IN} Undervoltage Lockout Hysteresis		150	200	300	mV
V_{ASD}	V_{IN}–V_{BAT} Lockout Threshold Voltage			150		mV
V_{ISET}	ISET Pin Voltage	R_{ISET} = 10K,Charge Mode		1		V
V_{EN-ON}	EN Logic-High Voltage Threshold		1.4			V
V_{EN-OFF}	EN Logic-Low Voltage Threshold				0.4	V
V_{CHRG}	CHRG Pin Output Low Voltage	I_{CHRG} = 5mA			0.5	V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT} - V_{RECHRG}	100	150	200	mV

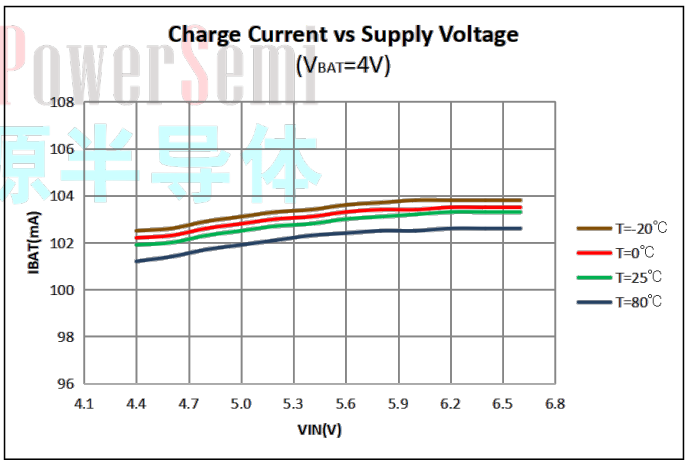
Typical Charging Profile

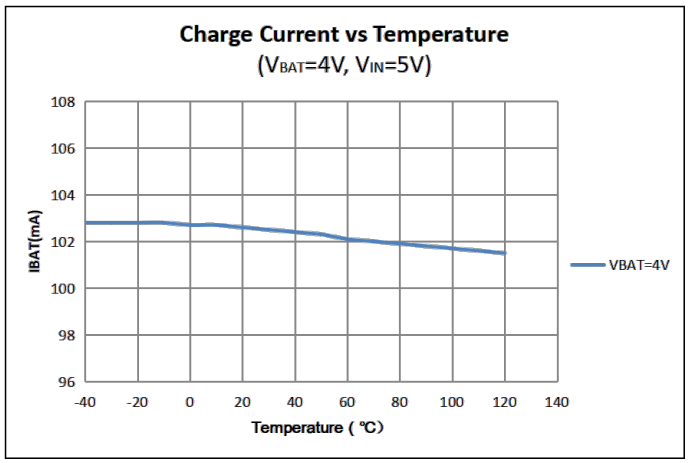


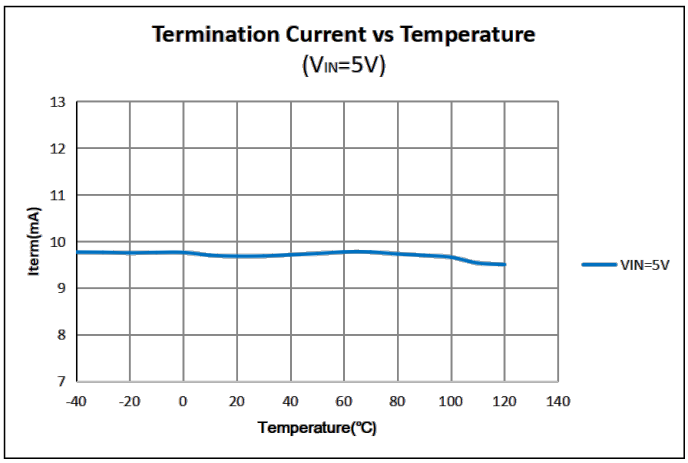
Typical Performance Characteristics

(C_{IN}=C_{BAT}=10uF)









Applications Information

The LP4070E is a highly integrated Li-Ion and Li-Pol linear charger device targeted at space-limited portable applications. The device operates from either a USB port or AC adapter. The charge voltage is preset at 4.2V/4.35V with ± 1% Accuracy and the charge current can be programmed up to 300mA externally with a single resistor. The LP4070E includes an internal P-channel power MOSFET and thermal regulation circuitry. No blocking diode or external current sense resistor is required; thus, the basic charger circuit requires only three external components.

Normal Charge Cycle

A charge cycle begins when the supply voltage at the VIN pin rises above the UVLO threshold level and the 1% program resistor is connected from the ISET pin to ground. If the battery voltage is below the trickle threshold, the battery is considered discharged and a trickle cycle begins. The amount of the current goes into the battery during this phase is called pre-charge current. It is fixed to 10% of the constant current. Once the battery voltage has charged to the trickle threshold, The fast charge current is applied. The constant current is programmed using the ISET terminal. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination current is set to 10% of the fast charge current.

Charge Current Program

The charge current is programmed using a single resistor from the ISET pin to ground. The battery charge current is 1000 times the current out of the ISET pin. The program resistor and the charge current are calculated using the following equations:

$$R_{ISET}=1000\div I_{BAT}$$

$$I_{BAT}=1000\div R_{ISET}$$

The charge current out of the BAT pin can be determined at any time by monitoring the ISET pin voltage using the following equation:

$$I_{BAT}=V_{ISET}\div R_{ISET}\times 1000$$

Charge Status Indicator (CHRG)

The charge status output has two different states: strong pull-down (~10mA) and high impedance. The strong pull-down state indicates that the LP4070E is in a charge cycle. High impedance indicates that the charge cycle complete or the LP4070E is in under voltage lockout mode: either V_{IN} is less than 100mV above the BAT pin voltage or insufficient voltage is applied to the VIN pin. A microprocessor can be used to distinguish between these two states.

Charge Stage	CHRG Pin Status
Charging	Low
Charge Complete	Hi-Z

Charge Termination

Once the BAT voltage reaches voltage regulation and the current tapers down to thetermination threshold (10% of the fast charge current), the CHRG terminal goes high impedance and a charge cycle is terminated This condition is detected by using an internal, filtered comparator to monitor the ISET pin. When the ISET pin voltage falls below 100mV for longer than T_{TERM} (typically 1ms), charging is terminated. The charge current is latched off and the LP4070E enters standby mode, where the input supply current drops to 200μA. When charging, transient loads on the BAT pin can cause the ISET pin to fall below 100mV for short periods of time before the DC charge current has dropped to the 10% programmed value. The 1ms filter time (T_{TERM}) on the termination comparator ensures that transient loads of this nature do not result in premature charge cycle termination. Once the average charge current drops below 10% programmed value, the LP4070E terminates the charge cycle and ceases to provide any current through the BAT pin. In this state, all loads on the BAT pin must be supplied by the battery. The LP4070E constantly monitors the BAT pin voltage in standby mode. If this voltage drops below the 4.05V recharge threshold (V_{RECHRG}), another charge cycle begins and current is once again supplied to the battery. To manually restart a charge cycle when in standby mode, the input voltage must be removed and reapplied.

Thermal Limit

An internal thermal feedback loop reduces the charge current if the die temperature attempts to rise above a preset value of approximately 125℃. This feature protects the LP4070E from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LP4070E. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.

Under voltage Lockout (UVLO)

An internal under voltage lockout circuit monitors the input voltage and keeps the charger in shutdown mode until V_{IN} rises above the under voltage lockout threshold .The UVLO circuit has a built-in hysteresis of 200mV. Furthermore, to protect against reverse current in the power MOSFET, the UVLO circuit keeps the charger in shutdown mode if V_{IN} falls to within 150mV of the battery voltage. If the UVLO comparator is tripped, the charger will not come out of shutdown mode until V_{IN} raises 150mV above the battery voltage.

Automatic Recharge

Once the charge cycle is terminated, the LP4070E continuously monitors the voltage on the BAT pin using a comparator with a 2ms filter time ($T_{RECHARGE}$). A charge cycle restarts when the battery voltage falls below 4.05V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at or near a fully charged condition and eliminates the need for periodic charge cycle initiations. CHRG output enters a strong pull-down state during recharge cycles.

Power Dissipation

The conditions that cause the LP4070E to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Nearly all of this power dissipation is generated by the internal MOSFET—this is calculated to be approximately:

$$PD=(V_{IN} - V_{BAT}) \times I_{BAT}$$

Where PD is the power dissipated, V_{IN} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A=125℃-PD\theta_{JA}$$

$$T_A=125℃-(V_{IN}-V_{BAT})\times I_{BAT}\times\theta_{JA}$$

Example: An LP4070E operating from a 5V USB supply is programmed to supply 300mA full-scale current to a discharged Li-Ion battery with a voltage of 3.75V. Assuming θ_{JA} is 256 ℃/W (see Board Layout Considerations), the ambient temperature at which the LP4070E will begin to reduce the charge current is approximately:

$$T_A=125℃-(5V-3.75V)\times(300mA)\times256℃/W$$

$$T_A=125℃-0.375W\times256℃/W=29℃$$

Moreover, when thermal feedback reduces the charge current, the voltage at the ISET pin is also reduced proportionally as discussed in the Operation section. It is important to remember that LP4070E applications do not need to be designed for worst-case thermal conditions since the IC will automatically reduce power dissipation when the junction temperature reaches approximately 125℃.

IN Bypass Capacitor

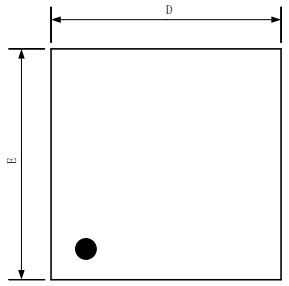
Many types of capacitors can be used for input bypassing; however, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a live power source. Adding a 1.5Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

Layout Considerations

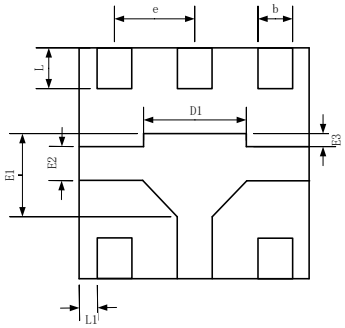
- For the main current paths as indicated in bold lines, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information

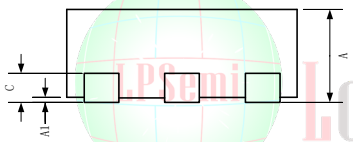
TDFN-6



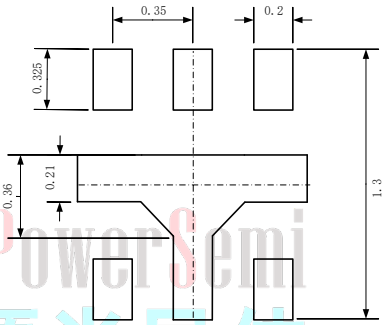
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.36	0.38	0.40
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
c		0.127REF	
D	0.95	1.00	1.05
D1	0.40	0.45	0.50
E	0.95	1.00	1.05
E1	0.31	0.36	0.41
E2	0.10	0.15	0.20
E3	0.005	0.055	0.105
e		0.35BSC	
L	0.125	0.175	0.225
L1		0.075REF	