Multi-Channel DC-DC Converter for LCD Panel

General Description

The LP6285 includes a high-efficiency boost regulator, a VCOM buffer, and dual charge pump controller for active matrix TFT LCDs.

The converter is a high switching frequency current-mode regulator with an integrated N-Channel 200mΩ MOSFET that allows the use of small inductors and ceramic capacitors.

The Unity-Gain buffer can drive the VCOM voltage, that features high short-circuit current, fast slew rate and rail-to-rail inputs and outputs.

The positive/negative charge pump controller provides regulated Gate-On voltage. The regulation of the charge pump is generated by the internal comparator that senses the output voltage and compares it with an internal reference.

Other features include under-voltage protection, short circuit protection, thermal shutdown protection and under-voltage lockout (UVLO). The LP6285 is available in a space saving QFN-16 (0.5mm pitch) package.

Order Information

LP6285 □□ □

F: Pb-Free

Package Type

QVF: QFN-16

Features

- Wide V_{IN} Range: 2.5V to 5.5V
- 1.2MHz Current-Mode Boost Regulator
  - Adjustable Output Voltage (±1%)
  - Built-In 2.5A, 200mΩ N-MOSFET
  - Internal Soft-Start
- Operation Amplifier for VCOM Buffer
  - Adjustable Detecting Voltage
  - Open-Drain Reset Output
- VGH and VGL Charge Pump
- Under-Voltage Protection
- Over-Temperature Protection
- Available in QFN-16 (3mm×3mm)
- RoHS Compliant
- Pb-Free Package

Applications

- Photo Frame
- GPS

Marking Information

Device	Marking	Package	Shipping
LP6285	LPS LP6285 YWX	QFN-16	3K/REEL
Y: Y is year code. W: W is week code. X: X is series number.			

Typical Application Circuit

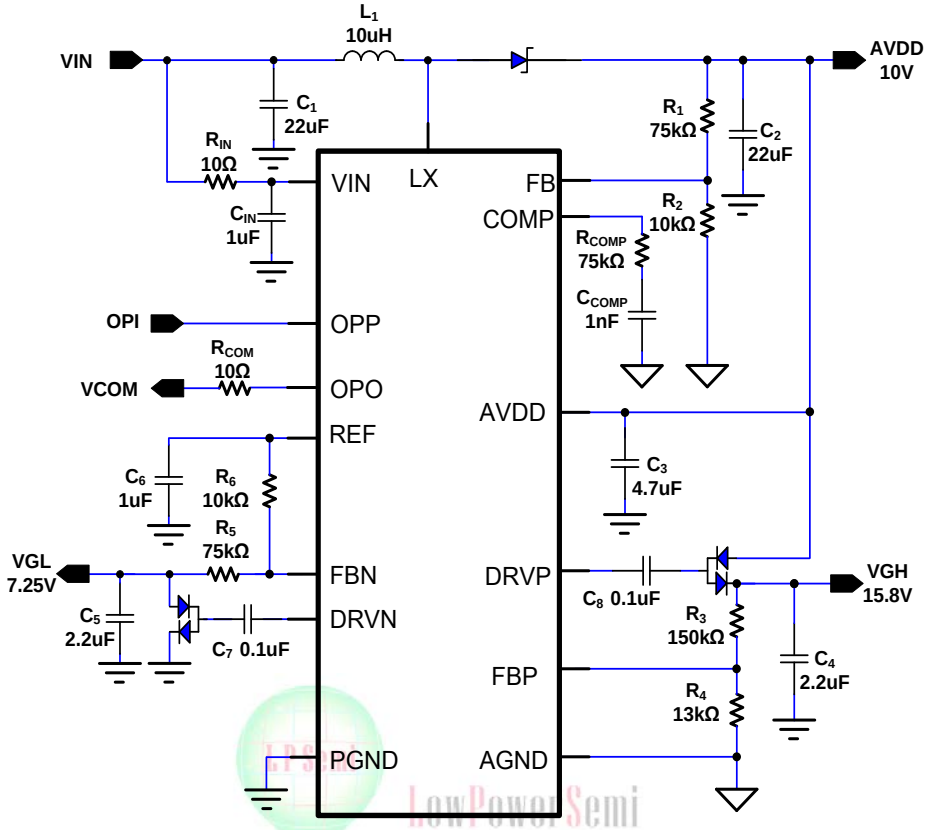


Figure 1. Typical Application Circuit of LP6285

Pin Configuration

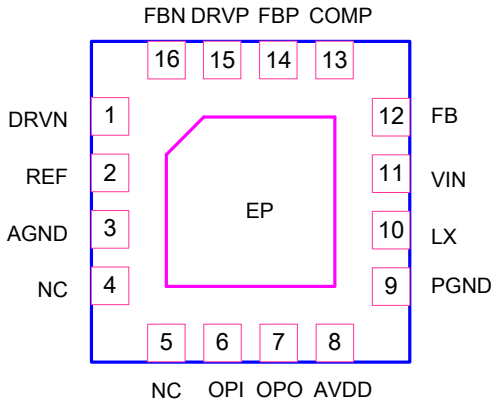


Figure 2. QFN-16 Package (3mm x 3mm) Top View

Function Block Diagram

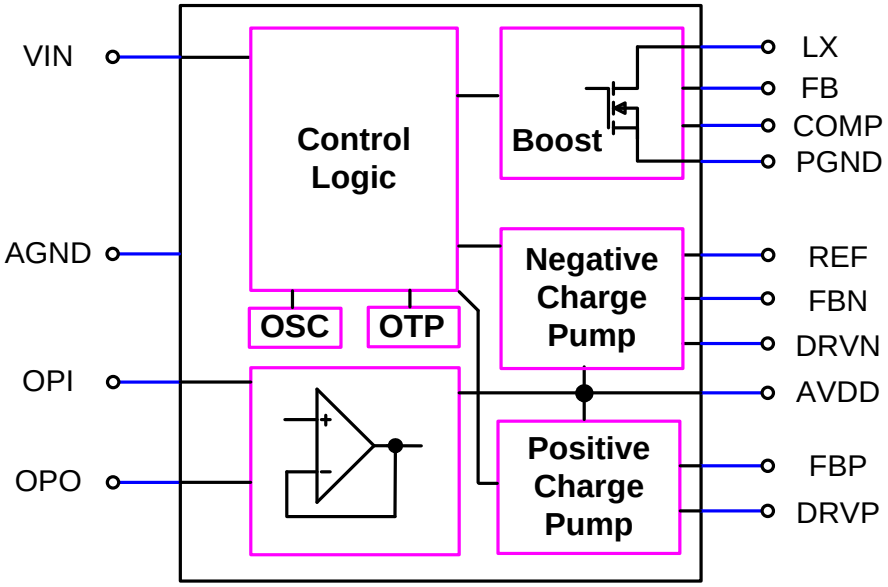


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	DRVN	VGL Charge-Pump Regulator Driver Output.
2	REF	Reference Voltage Output. Connect a ceramic capacitor between REF and GND.
3	AGND	Analog GND.
4, 5	NC	No connection.
6	OPI	Unity-Gain OP Input pin.
7	OPO	Unity-Gain OP Output pin.
8	AVDD	VDD for Source Driver Power. This also supplies the Charge-Pump/OPA power source.
9	PGND	Power Ground.
10	LX	Boost Regulator Switching Node. Connect the inductor and the schottky diode to LX.
11	VIN	Supply Input. The input voltage range is between 2.5V to 5.5V. Connect a ceramic capacitor between VIN and GND.
12	FB	Boost Regulator Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage.
13	COMP	Boost Regulator Error Amplifier Compensation Pin.
14	FBP	VGH Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGH to GND to set the output voltage.
15	DRVP	VGH Charge-Pump Regulator Driver Output.
16	FBN	VGL Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGL to REF to set the output voltage.
EP		Exposed pad. Connect this pin to other gnd pin.

Absolute Maximum Ratings Note 1

- ✧ VIN to GND ---------- −0.3V to +7V
- ✧ AVDD, LX to GND ---------- −0.3V to +20V
- ✧ FB, FBP, FBN, COMP, REF to GND ---------- −0.3V to (VIN + 0.3V)
- ✧ OPI, OPO, DRVP, DRVN to GND ---------- −0.3V to (AVDD + 0.3V)
- ✧ PGND to GND ---------- −0.3V to +0.3V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40°C to +150°C
- ✧ Operation Ambient Temperature Range ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} =3.3V, V_{AVDD} =10V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
V_{IN} Input Supply Voltage	V_{IN}		2.5		5.5	V
AVDD	AVDD		6		18	V
AVDD Over Voltage Protect	V_{OVP}			18	20	V
Boost Switching Frequency	F_{LX}		1	1.2	1.4	MHz
Charge Pump Frequency	F_{CP}		500	600	700	kHz
V_{IN} Supply Current	I_Q	VFB=1.3V, LX no Switching		0.3	0.6	mA
		VFB=1.1V, LX Switching		0.8	2	mA
AVDD Operation Current	I_{AVDD}			0.6	0.9	mA
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{IN} Rising	1.8	2	2.2	V
UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$	Falling Hysteresis		100		mV
Reference Voltage	V_{REF}		1.176	1.2	1.224	V
Thermal Shutdown Threshold	T_{SD}			150		°C
Thermal Shutdown Hysteresis				30		°C
Boost Regulator						
Maximum Duty-Cycle	D_{MAX}		86	90	94	%
Feedback Voltage	V_{FB}		1.188	1.2	1.212	V
Transcocnductance	Gm	ΔI=5uA		70		uA/V
Voltage Gain	A_V			700		V/V
Switch-ON Resistance	$R_{DS(ON)}$			200	500	mΩ
Current Limit	I_{Limit}			2.5		A
LX Leak Current	I_{Leak}	LX Off.		0.01	1	uA
Internal Soft Start Time	T_{SS}			10		ms
UVP Fault Protection Voltage	V_{UVP}	V_{FB} Falling		0.95		V
UVP Fault Delay	T_{UVP}			100		ms
Short Circuit Protection Voltage	V_{SCP}			100		mV

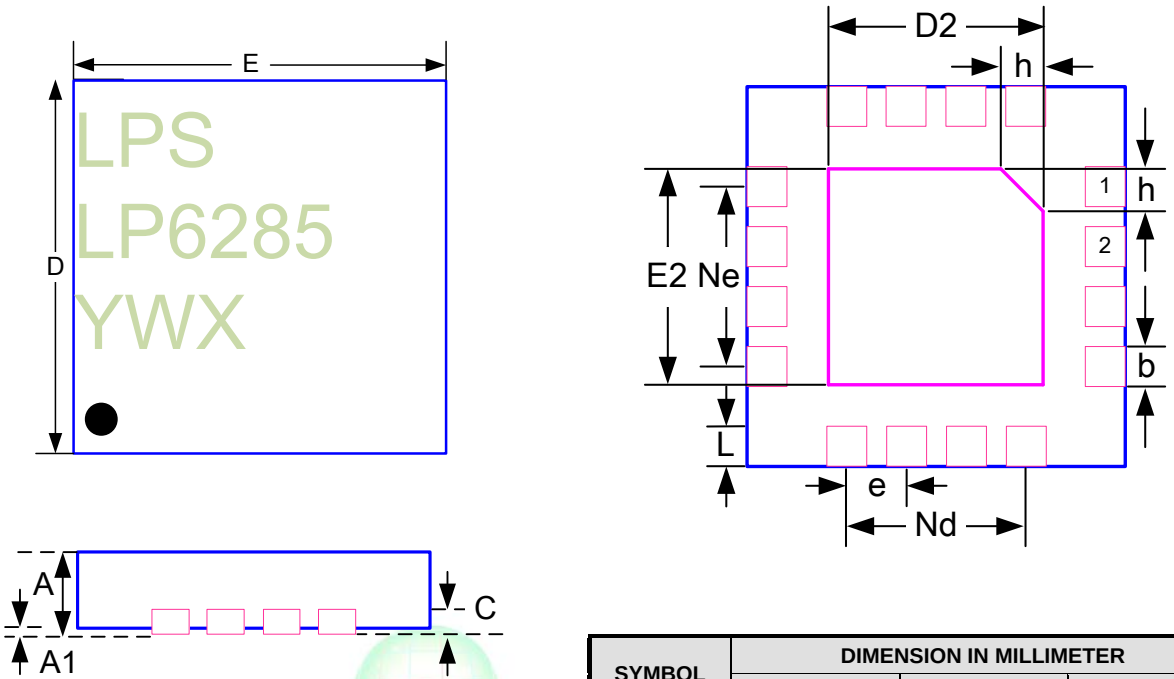
Electrical Characteristics (Continued)

(V_{IN} =3.3V, V_{AVDD} =10V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Charge Pump						
Charge Pump Soft Start Time	T_{SS_CP}			3.4		ms
Positive Feedback Voltage	V_{FBP}		1.176	1.2	1.224	V
DRVP Switch ON Resistance	R_{DS_DRVP1}	AVDD=10V, I_{DRVP}=20mA		3	20	Ω
	R_{DS_DRVP2}			3	20	Ω
Negative Feedback Voltage	V_{FBN}		210	240	270	mV
DRVN Switch ON Resistance	R_{DS_DRVN1}			3	20	Ω
	R_{DS_DRVN2}			3	20	Ω
Operation Amplifier						
Input Offset Voltage	V_{OS}	V_{OPO}=V_{AVDD}/2		2	15	mV
Output Voltage Swing High	V_{OH}	I_{Load} = 500uA	AVDD - 20	AVDD - 5		mV
		I_{Load} = 5mA	AVDD - 200	AVDD - 50		
Output Voltage Swing Low	V_{OL}	I_{Load} = -500uA		5	20	
		I_{Load} = -5mA		150	200	
Short Circuit Current	V_{OP_Short}	V_{OPO}=V_{AVDD}/2		±100		mA
Slew Rate	SR		8	12		V/us

Outline Information

QFN-16 Package (3x3) pitch 0.5 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.180	0.250	0.300
C	0.180	0.200	0.250
D	2.900	3.000	3.100
D2	1.550	1.650	1.750
E	2.900	3.000	3.100
E2	1.550	1.650	1.750
e	0.500 BSC		
Nd	1.500 BSC		
Ne	1.500 BSC		
L	0.350	0.400	0.450
h	0.200	0.250	0.300