



LPM2301 -20V/-2.6A

P-Channel Enhancement Mode Field Effect Transistor

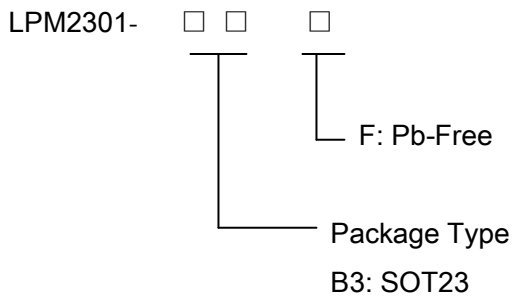
General Description

The LPM2301 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Ordering Information



Features

- -20V/-2.6A, $R_{DS(ON)}=150m\Omega(\text{typ.})@V_{GS}=-2.5V$
- -20V/-2.6A, $R_{DS(ON)}=120m\Omega(\text{typ.})@V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOT23 Package

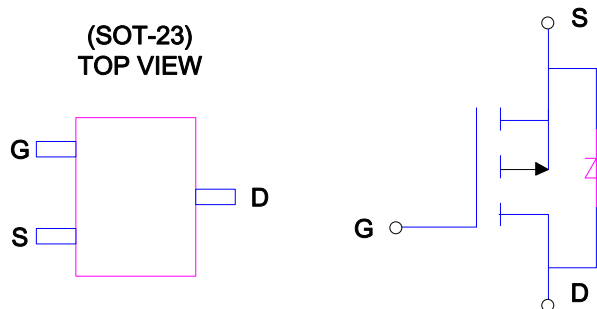
Applications

- ◇ Portable Media Players
- ◇ Cellular and Smart mobile phone
- ◇ LCD
- ◇ DSC Sensor
- ◇ Wireless Card

Marking Information

Device	Marking	Package	Shipping
LPM2301B3F	A1SHB	SOT23	3K/REEL

Pin Configurations





Absolute Maximum Ratings

$T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current A	I_D	$T_A=25^{\circ}\text{C}$	A
Current A		$T_A=70^{\circ}\text{C}$	
Pulsed Drain Current B	I_{DM}	-8	
Power Dissipation A	P_D	$T_A=25^{\circ}\text{C}$	W
		$T_A=70^{\circ}\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ.	Units
Maximum Junction-to-Ambient	$R_{\theta JA}$	$t \leq 10\text{s}$	$^{\circ}\text{C/W}$
Maximum Junction-to-Ambient		Steady-State	$^{\circ}\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	Steady-State	$^{\circ}\text{C/W}$

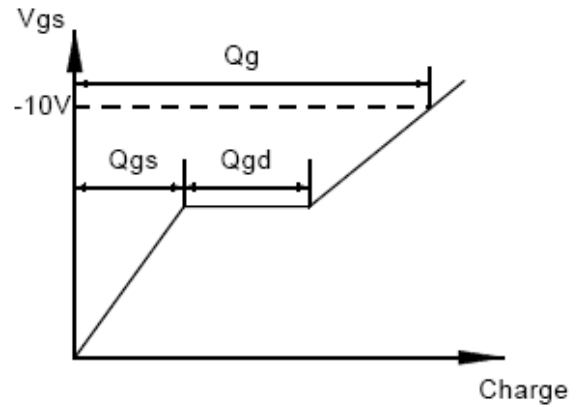
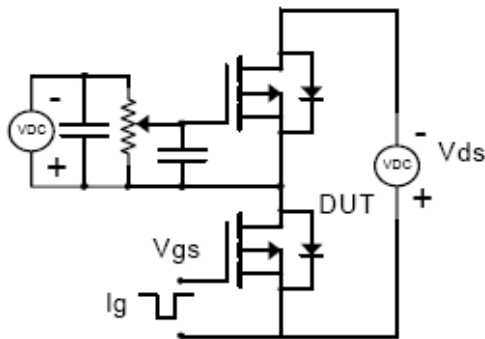


Functional Pin Description

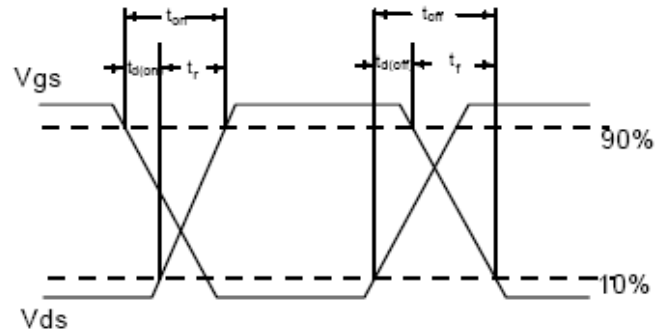
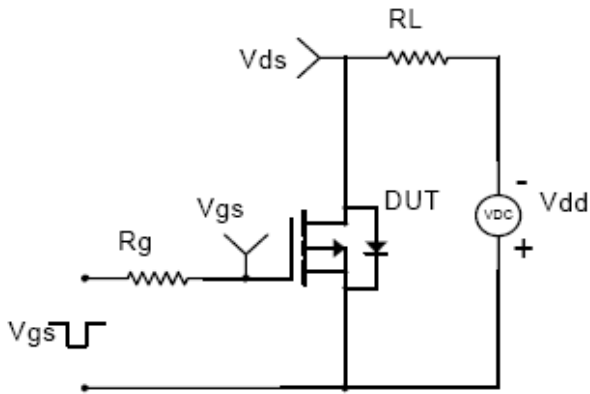
Symbol	Parameter	Condition	Min	Typ.	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu A, V_{GS}=0V$	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-1 -10	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0V, V_{GS}=\pm 12V$			± 1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4		-1	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-2.6A$		120		$m\Omega$
		$V_{GS}=-2.5V, I_D=-2.6A$		150		$m\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$		10		S
V_{SD}	Diode Forward Voltage	$I_S=-1A, V_{GS}=0V$		-0.7	-1	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=-15V,$ $f=1MHz$		400		pF
C_{oss}	Output Capacitance			220		pF
C_{riss}	Reverse Transfer Capacitance			80		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS}=-10V, V_{DS}=-15V,$ $I_D=-2A$		7		nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1.8		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10V, V_{DS}=-15V,$ $R_L=3.6\Omega,$ $R_{GEN}=6\Omega$		15		nS
t_r	Turn-On Rise Time			36		
$t_{D(off)}$	Turn-Off DelayTime			42		
t_f	Turn-Off Fall Time			34		



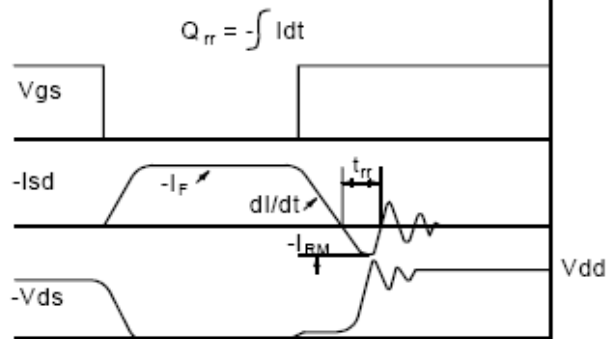
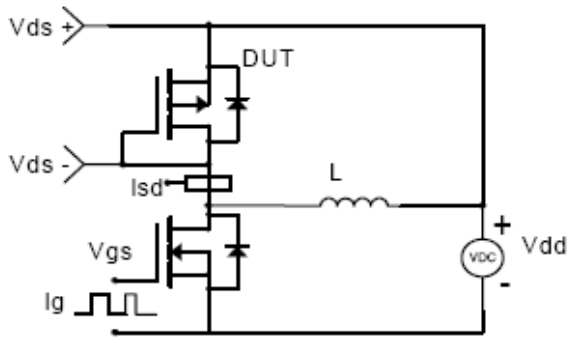
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



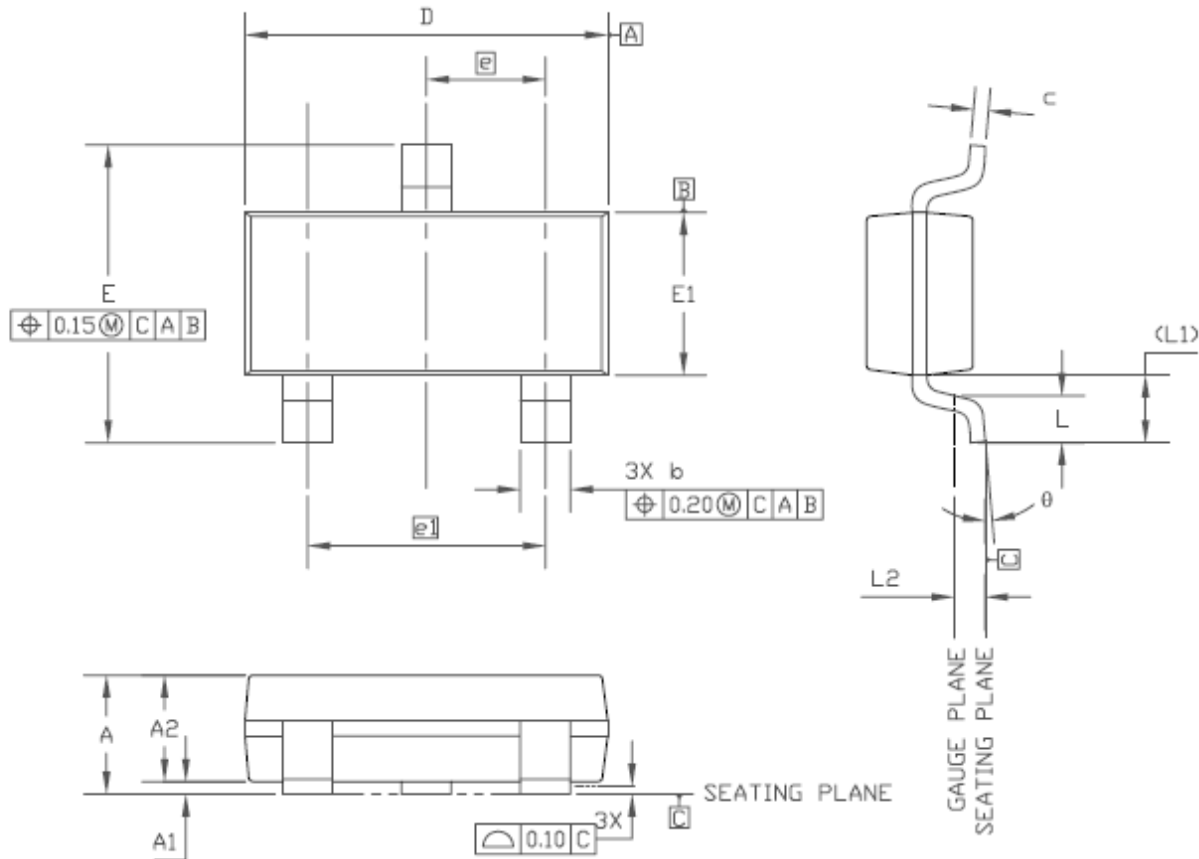
Diode Recovery Test Circuit & Waveforms



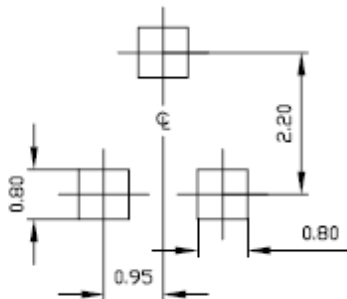


Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
theta	0°	—	8°	0°	—	8°