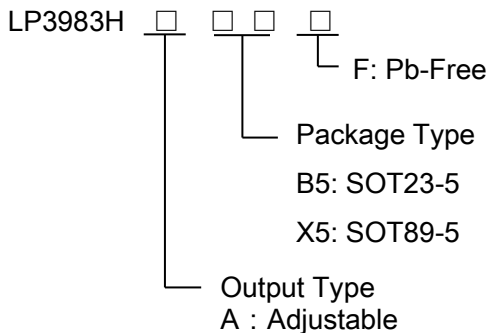


## 600mA, Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

### General Description

The LP3983H is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3983H performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3983H also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3983H consumes less than 0.1 $\mu$ A in shutdown mode and has fast turn-on time less than 50 $\mu$ s. The other features include ultra low dropout voltage, high feedback accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 5-lead of SOT23-5 and SOT89-5 packages.

### Order Information



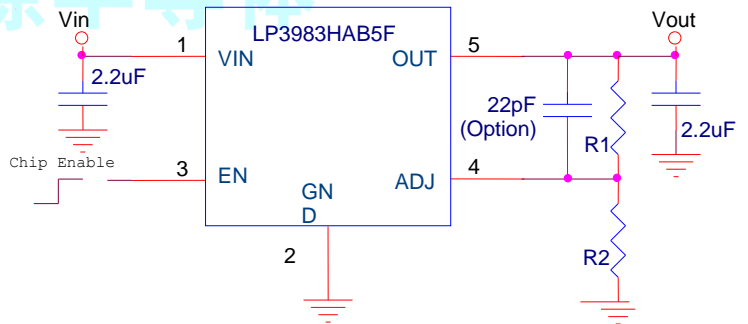
### Features

- ◆ Ultra-Low-Noise for RF Application
- ◆ 2.2V- 6V Input Voltage Range
- ◆ Low Dropout : 420mV @ 600mA
- ◆ 600mA Output Current, 750mA Peak Current
- ◆ High PSRR: -70dB at 217Hz
- ◆ < 1uA Standby Current When Shutdown
- ◆ Ultra-Fast Response in Line/Load transient
- ◆ Current Limiting and Thermal Shutdown Protection

### Applications

- ◇ Portable Media Players/MP3 players
- ◇ Cellular and Smart mobile phone
- ◇ LCD/ DSC Sensor
- ◇ Wireless Card

### Typical Application Circuit



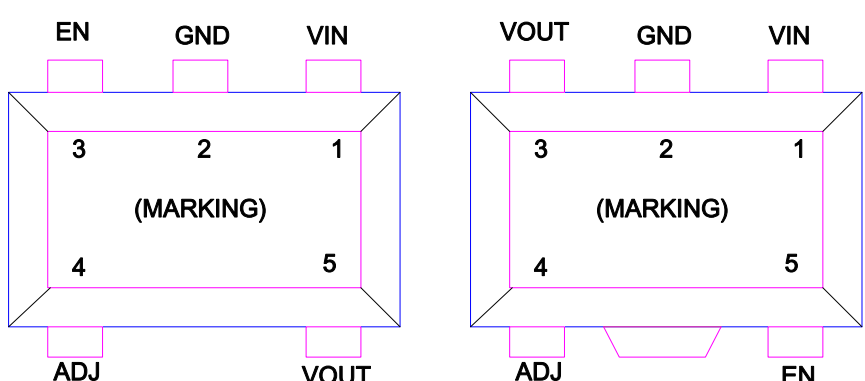
### Marking Information

Device	Marking	Package	Shipping
LP3983HAB5F	LPS 1FYWX	SOT23-5	3K/REEL
LP3983HAX5F	LPS 3983X YWX	SOT89-5	1K/REEL

Marking indication:

Y:Year code .W: W is week code. X: X is series number.

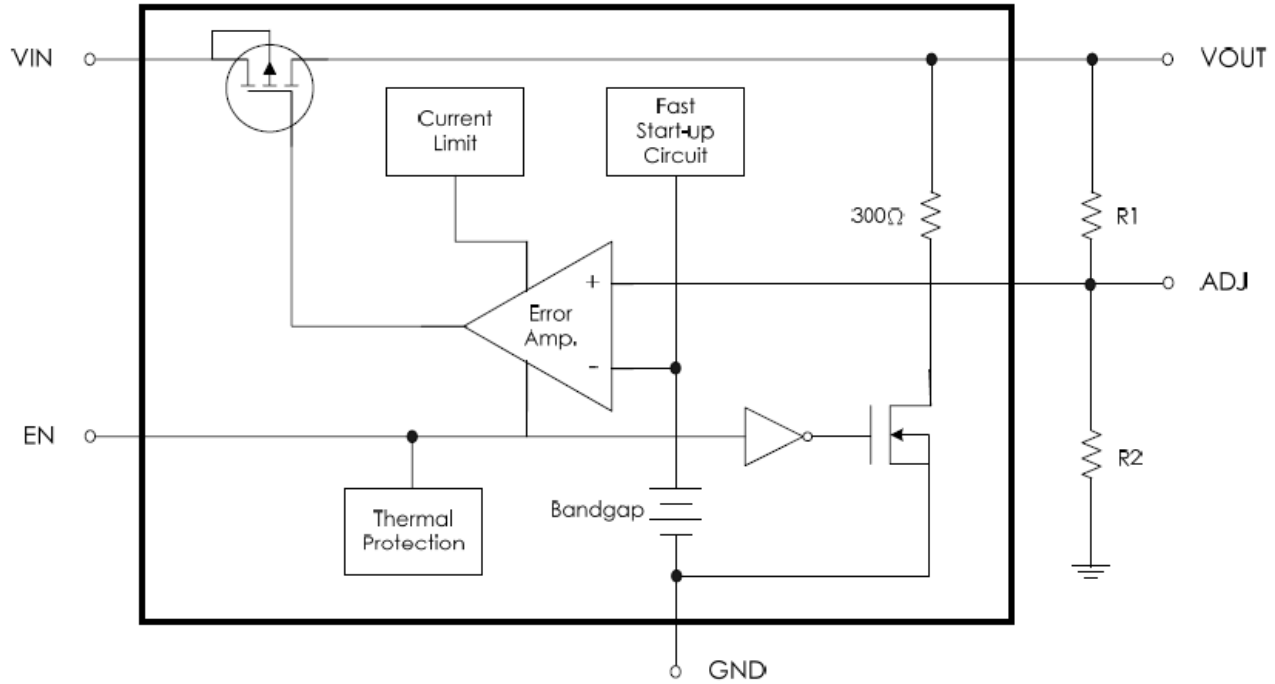
## Functional Pin Description

Package Type	Pin Configurations
SOT23-5 / SOT89-5	 <p style="text-align: center;">SOT23-5                      SOT89-5</p>

## Pin Description

Pin		Name	Description
SOT23-5	SOT89-5		
1	1	VIN	Power Input Voltage.
2	2	GND	Ground.
3	5	EN	Chip Enable (Active High). There is an integrated pull low 1MΩ resistor connected to GND when the EN pin is floating.
4	4	BP	Feedback pin. The reference voltage is 0.8V.
5	3	VOUT	Output Voltage. $V_{out} = V_{FB} \times (1 + R1/R2)$ , which $V_{FB} = 0.8V$

## Function Diagram



## Absolute Maximum Ratings

- ◇ Supply Input Voltage ----- -0.3V to 6.5V
- ◇ EN Pin Voltage ----- -0.3V to  $V_{in}+0.3V$

Power Dissipation, PD @  $T_A = 25^{\circ}C$

- ◇ SOT23-5 ----- 500mW
- ◇ SOT89-5 ----- 700mW

Package Thermal Resistance

- ◇ SOT23-5,  $\theta_{JA}$  -----  $195^{\circ}C/W$
- ◇ SOT89-5,  $\theta_{JA}$  -----  $165^{\circ}C/W$
- ◇ Lead Temperature (Soldering, 10 sec.) -----  $260^{\circ}C$
- ◇ Storage Temperature Range -----  $-60^{\circ}C$  to  $125^{\circ}C$

ESD Susceptibility

- ◇ HBM (Human Body Mode) ----- 2kV
- ◇ MM(Machine-Mode) ----- 200V

Recommended Operating Conditions

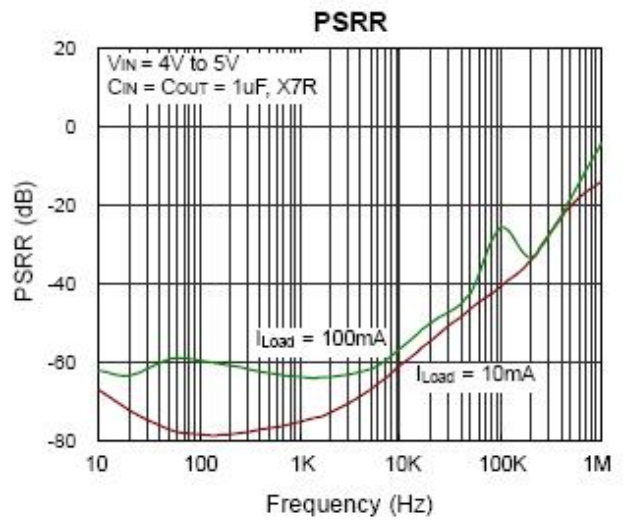
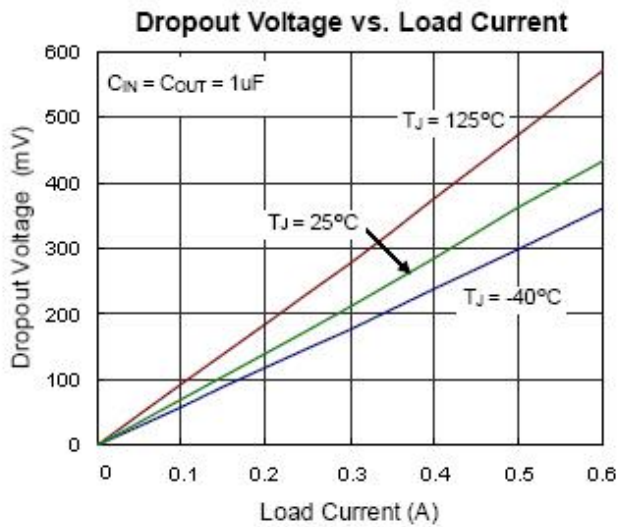
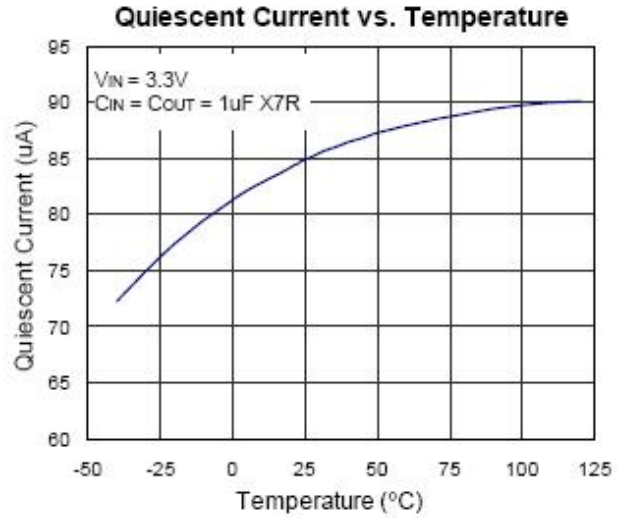
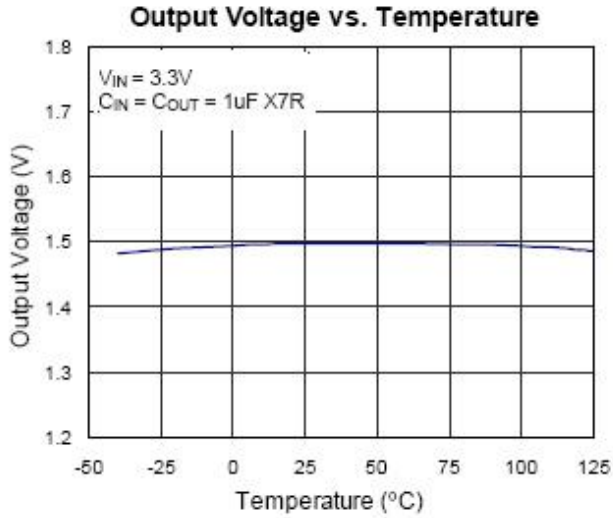
- ◇ Supply Input Voltage ----- 2.2V to 6V
- ◇ Operation Ambient Temperature Range -----  $-40^{\circ}C$  to  $85^{\circ}C$

## Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1μF, , TA = 25° C, unless otherwise specified)

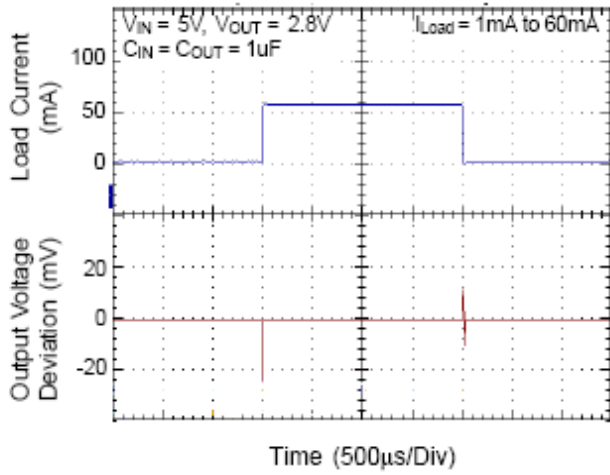
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Loading Current		I <sub>LOAD</sub>	V <sub>EN</sub> =V <sub>IN</sub> , V <sub>IN</sub> >2.5V		600		mA
Current Limit		I <sub>LIM</sub>	R <sub>LOAD</sub> = 1Ω		750		mA
Adjustable voltage reference		V <sub>FB</sub>	I <sub>OUT</sub> =1mA	0.784	0.8	0.816	V
Quiescent Current		I <sub>Q</sub>	V <sub>EN</sub> ≥ 1.2V, I <sub>OUT</sub> = 0mA		75	130	μA
Dropout Voltage		V <sub>DROP</sub>	I <sub>OUT</sub> = 400mA, V <sub>OUT</sub> >2.8V		280	320	mV
			I <sub>OUT</sub> = 600mA, V <sub>OUT</sub> >2.8V		420	480	mV
			I <sub>OUT</sub> = 400mA, V <sub>OUT</sub> =1.8V		520	600	mV
			I <sub>OUT</sub> = 600mA, V <sub>OUT</sub> =1.8V		740	800	mV
			I <sub>OUT</sub> = 400mA, V <sub>OUT</sub> =1.2V		1000	1200	mV
			I <sub>OUT</sub> = 600mA, V <sub>OUT</sub> =1.2V		1140	1300	mV
Line Regulation		ΔV <sub>LINE</sub>	V <sub>IN</sub> = (V <sub>OUT</sub> + 1V) to 5.5V, I <sub>OUT</sub> = 1mA			0.2	%
Load Regulation		ΔV <sub>LOAD</sub>	1mA < I <sub>OUT</sub> < 300mA			2	%
Standby Current		I <sub>STBY</sub>	V <sub>EN</sub> = GND, Shutdown		0.1	1	μA
EN Input Bias Current		I <sub>IBSD</sub>	V <sub>EN</sub> = 5V		5		nA
EN Threshold	Logic-Low Voltage	V <sub>IL</sub>	V <sub>IN</sub> =3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V <sub>IH</sub>	V <sub>IN</sub> =3V to 5.5V, Start-Up	1.4		V <sub>IN</sub> +0.3	V
Output Noise Voltage			10Hz to 100kHz, I <sub>OUT</sub> =200mA		100		μVRMS
Power Supply Rejection Rate	f = 217Hz	PSRR	C <sub>OUT</sub> =1μF, I <sub>OUT</sub> =10mA		-70		dB
	f = 1kHz				-58		dB
Thermal Shutdown Temperature		T <sub>SD</sub>			150		°C

## Typical Operating Characteristics

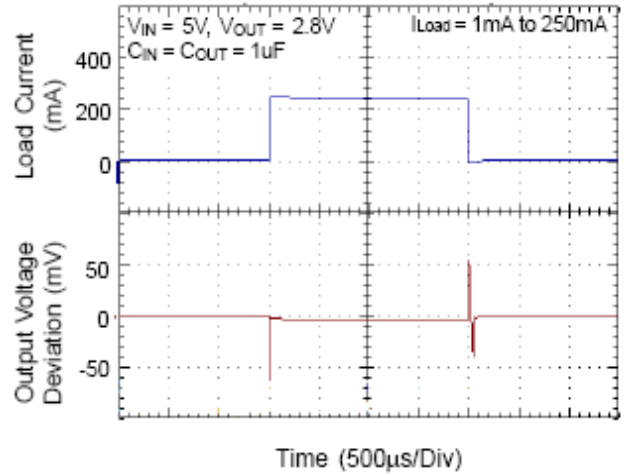




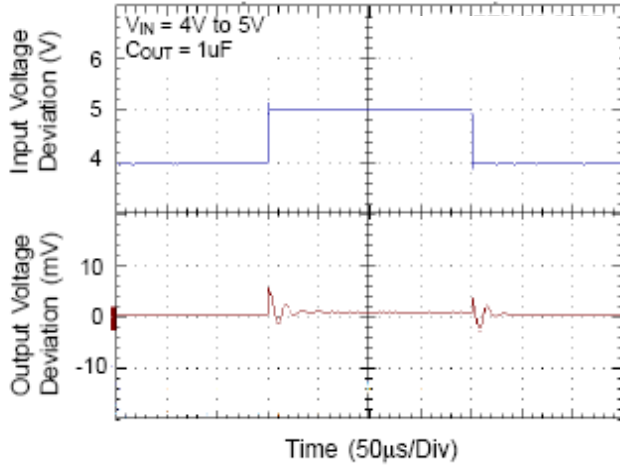
Load Transient Response



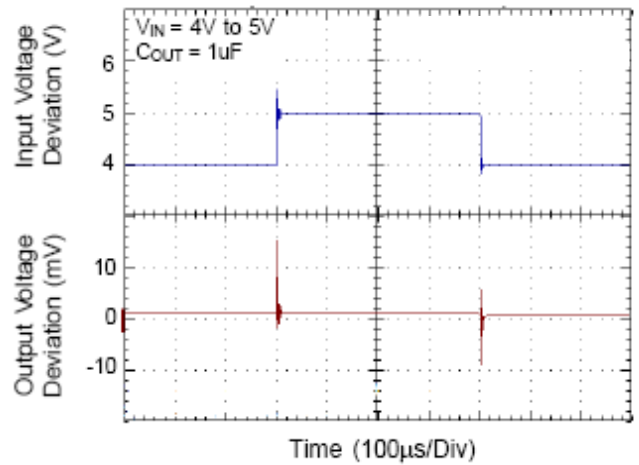
Load Transient Response



Line Transient Response

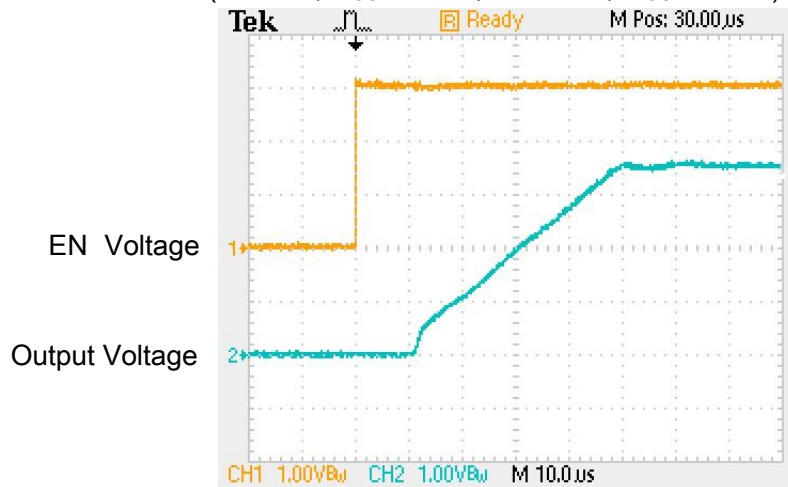


Line Transient Response



EN Soft Start Function

( $V_{IN}=5V$  ,  $V_{OUT}=3.3V$  ,  $C_{IN}=1uF$  ,  $C_{OUT}=4.7uF$ )



## Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3983H must be carefully selected for regulator stability and performance. Using a capacitor whose value is  $> 1\mu\text{F}$  on the LP3983H input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. There is a special attention which is the input capacitance should not be less than output capacitance. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3983H is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least  $1\mu\text{F}$  with ESR is  $> 25\text{m}\Omega$  on the LP3983H output ensures stability. The LP3983H still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the  $V_{\text{OUT}}$  pin of the LP3983H and returned to a clean analog ground.

### Enable Function

The LP3983H features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts but not above  $V_{\text{IN}}+0.3\text{V}$ . The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For protecting the system, the LP3983H have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to  $V_{\text{IN}}$  to keep the LDO regulator in a continuously on state.

### Feedback Capacitor and Voltage

For adjustable version, connecting a 22pF between output pin and FB pin significantly reduces output voltage ripple, it is critical that the capacitor connection should be direct and PCB traces should be as short as possible. The output voltage of LDO could be set by the formula below:

$$V_{\text{out}}=V_{\text{FB}} \times ( 1+R1/R2 )$$

which  $V_{\text{FB}} = 0.8\text{V}$

$V_{\text{OUT}}(\text{V})$	$R2(\text{K}\Omega)$	$R1(\text{K}\Omega)$
1.2	51	25.5
1.5	51	44.6
1.8	51	63.8
2	47	70.5
2.5	47	99.9
2.8	47	117.5
3	33	90.8
3.3	33	103.1
3.5	33	111.4
4	33	132.0
4.2	33	140.3
4.5	33	152.6

Considering the practical application, we may add a small capacitor with R1 in parallel which could be 22pF or 47pF.



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### Thermal Considerations(for SOT23-5)

Thermal protection limits power dissipation in LP3983H. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C. For continue operation, do not exceed absolute maximum operation junction temperature 150°C.

The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction and ambient.

The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 150°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3983H, where

$T_{J(MAX)}$  is the maximum junction temperature of the die (150°C) and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance ( $\theta_{JA}$  is layout dependent) for SOT23-5 package is 195°C/W.

$$P_D = (150^\circ\text{C} - 25^\circ\text{C}) / 195 = 641\text{mW (SOT23-5)}$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . Considering the PCB thermal feather, the  $P_{D(MAX)}$  may be higher than 500mW.

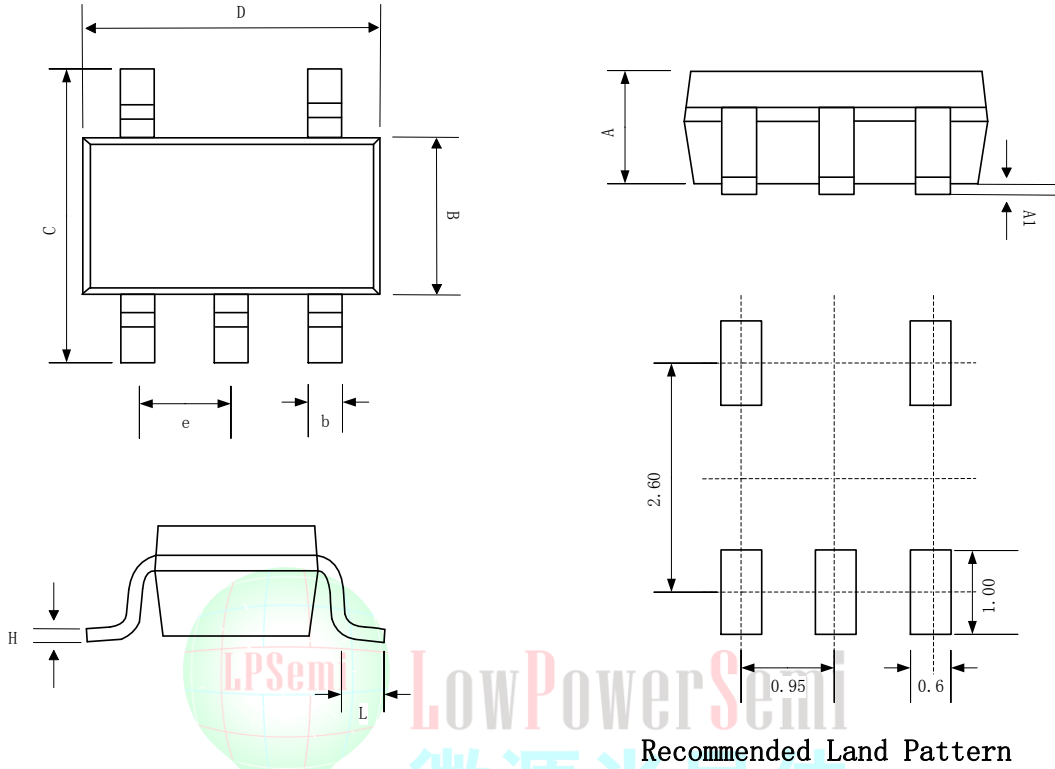


LOW POWER SEMI  
微源半导体



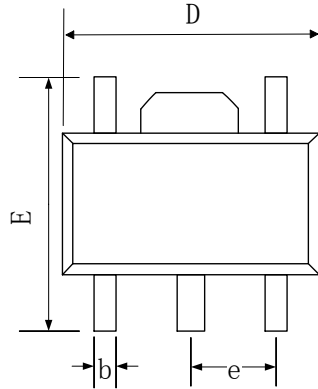
# Packaging Information

## SOT23-5

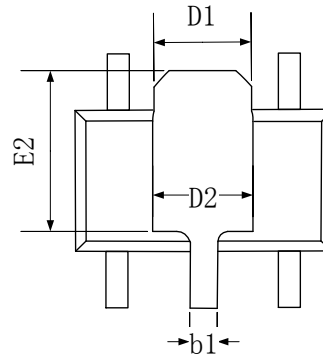


SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

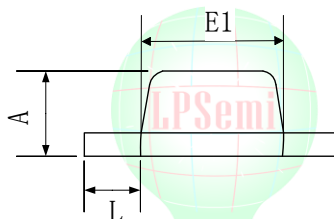
## SOT89-5



TOP VIEW



BOTTOM VIEW



SIDE VIEW

LP Semi Low Power Semi  
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SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.40	1.50	1.60
b	0.32	0.42	0.52
b1	0.36	0.48	0.56
c	0.35	-	0.44
D	4.40	4.50	4.60
D1	1.70 REF		
D2	1.75 REF		
E	4.00	4.20	4.40
E1	2.30	2.45	2.60
E2	2.84 REF		
e	1.50 BSC		
L	0.80	1.00	1.20