Features

- Input over-voltage protected up to 16V
- Charge Management
  - Programmable charge current up to 1A
  - Programmable floating voltage with 0.3% accuracy
  - Programmable trickle charge and termination current
- Charge and discharge current monitor
- Automatic re-charge and thermal foldback
- I2C bus to SoC with an interrupt pin
- Low drop-out fast charge function
- Power Path Management
- Charge safety timer and watchdog
- NTC management
- Rich protections: UVLO, OVP, SCP
- 0.6-μA ultra-low iq in standby mode
- 0.4-μA ultra-low iq in ship mode
- 3mm X 3mm DFN-10 package
- RoHS Compliant and 100% Lead (Pb) Free
-

Applications

- Wearable
- Fitness Application
- Smart Watch

General Description

The LP4081H is an ultra-low power linear charger targeting at wearable applications protected up to 16V input voltage. It contains a linear charger to charge the Li-ion battery. An I2C interface is offered for programmability and flexibility of the device. The charger has an ideal-diode mode for high efficiency and low heat operation. The LP4081H integrates the power path management function to support SoC powerup even with a deeply-discharged battery. The LP4081H features 150mΩ low $R_{ds,on}$ of the BAT_FET from the battery to the system to achieve high discharge efficiency and low heat.

The LP4081H provides rich protections, including the input Under-volage lockout protection (UVLO), input over-voltage protection (OVP) and system short circuit protection (SCP).

The typical quiescent current of LP4081H is 0.6-μA and the battery current is reduced to 0.4-uA in ship mode.

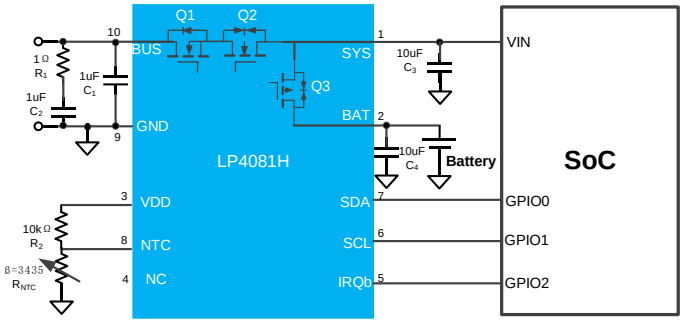
The whole system is in a 10-pin 3 X 3 DFN package.

Order Information

LP4081H □□ □

- F: Green/Pb-Free
- Package Type
  - QV : DFN

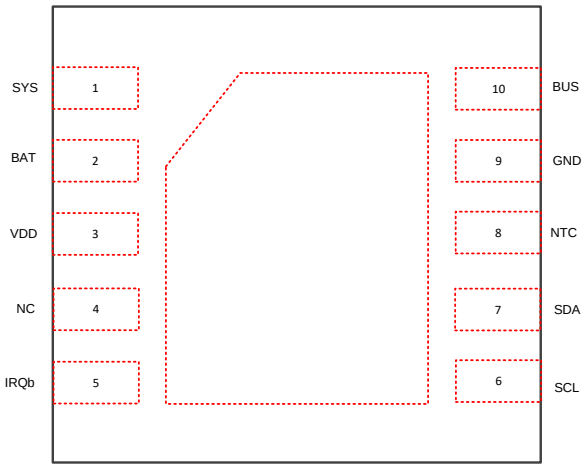
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping
LP4081HQVF	LPS LP4081H YWX	10-pin 3 X 3 DFN	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.			

Pin Diagram



LP4081H Pinout

Pin Description

Pin #	Name	Description
1	SYS	power output for the system. A 4.7uF decoupling capacitor is recommended.
2	BAT	Battery pin of the linear charger. A 4.7uF decoupling capacitor is recommended.
3	VDD	NTC bias voltage output
4	NC	No connection. Left this pin float.
5	IRQb	interrupt output. Ship mode detection. This pin open-drain output.
6	SCL	Clock line of the I2C bus. This pin open-drain output.
7	SDA	Data line of the I2C bus. This pin open-drain output.
8	NTC	NTC detection pin. Connect the resistor divider between this pin, VDD and GND pin
9	BUS	Input power supply. A 4.7uF decoupling capacitor is recommended.
10	GND	Power Ground.
		Thermal PAD, reuse as the GND pin. Connect to power ground.

Absolute Maximum Ratings (Note)

BUS to GND ---------- -0.3V to 16V

All other pins to GND ---------- -0.3V to 6.5V

Maximum Junction Temperature (TJ) ---------- 150°C

Operating Ambient Temperature Range (TA) ----------40℃ to 85℃

Maximum Soldering Temperature (at leads, 10 sec) ----------260℃

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV

CDM (Charged Device Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ----------65℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{bus}	Input voltage	3		5.6	V
I_{bus}	Input current			1.5	A
T_A	Ambient temperature range	-40		85	°C
C_{bus}	Input decoupling capacitor	0.1			μF
C_{sys}	System capacitor	1			μF
C_{bat}	Battery capacitor	1			μF

Electrical Characteristics

(The specifications are measured under conditions V_{bus} = 5V, T_J = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_bus}	BUS UVLO	BUS falling, no deglitch		3.0		V
V_{ULVO_H}	BUS UVLO hysteresis	BUS rising		100		mV
V_{OVP_bus}	BUS OVP BUS	BUS rising, no deglitch	5.6	5.7	5.8	V
V_{OVP_H}	BUS OVP BUS hysteresis	BUS falling		100		mV
I_{q_bus}	BUS Input quiescent current	BUS=5.0V，BAT=4.3V，EN_CHG=1,		100	130	uA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ds,on_bus}	Q1+Q2, NMOS on- resistance			0.3	0.4	Ω
I_{IN_LIM}	Input current limit	IIN_LIM=0	0.5	0.65		A
	Hiccup wait time			60		ms
BATTERY SECTION						
V_{BAT_POR}	BAT Power-on-reset	battery voltage rising	1.6		2.4	V
$V_{BAT\_POR\_hys}$	BAT POR hysteresis			100		mV
I_{BAT_Dis}	Quiescent current from BAT	Discharge mode，BUS=0V, BAT=3.8V, SYS=Float DIS[1:0]=10, EN_WTD=1		16		uA
I_{BAT_CHG}		Charge mode ，BUS=5V, BAT=4.5V, EN_Term=1		2	3	uA
I_{BAT_STD}		Standby mode ，BUS=0V, BAT=3.8V, DIS[1:0]=00, EN_WTD=0 , EN_NTC=0		0.6	1	uA
I_{BAT}		Ship mode，BUS=0V, BAT=3.8V		0.4		uA
Charge Management						
V_{TRK}	Trickle charge voltage threshold	BAT rising edge, Vtri=3.0V	2.95	3.0	3.05	V
V_{TRK_hys}	Trickle charge voltage hysteresis			100		mV
I_{TRK}	Trickle charge current	Iterm[2:0]=001, 3mA	2.7	3	3.3	mA
I_{CC}	CC current	25ºC	28.5	30	31.5	mA
V_{CV}	CV voltage	25ºC	-0.3		0.3	%
		From -10ºC to 85ºC	-0.5		0.5	%
V_{RECHG}	Re-charge threshold	BAT falling edge, Reference to CV voltage		-150		mV
t_{drechg}	Recharge deglitch time [1]			200		ms
I_{term}	Charge termination current	Iterm[2:0]=001, 3mA	2.7	3	3.3	mA
t_{dterm}	termination deglitch time[1]			30		ms

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SYS_DPM}	SYS Dynamic Power Management	DPM[2:0]= 011, 3.6V	3.55	3.6	3.65	V
T_{therm}	Thermal foldback threshold		100	120	140	ºC
t_{Tri_safe}	Trickle charge safety timer			0.75		hr
t_{Fast_safe}	Fast charge safety timer	From exit Trickle to charge terminate		3.75		hr
Power Path Management						
R_{ds,on_bat}	BAT_FET on resistance	BAT=3.8V		0.15	0.2	Ω
I_{DIS_LIM}	Discharge SCP limit	IDIS_LIM[1:0]=00,		0.44		A
t_{denter_ship}	Enter shipping mode delay time[1]			1		s
t_{dexit_ship}	Exiting shipping mode by pulling IRQb pin delay time[1]			2		s
V_{UV_BAT}	Battery UVLO	BAT falling edge		3.0		V
		hysteresis		0.2		V
t_{d_BATUV}	BAT_UV deglitch			40		ms
NTC Management						
T_0	0ºC threshold	V_{NTC} rising edge threshold	72.4	73.3	74.2	%
		Hysteresis		1.5		%
T_{10}	10ºC threshold	V_{NTC} rising edge threshold	63.3	64.3	65.3	%
		Hysteresis		1.5		%
T_{45}	45ºC threshold	V_{NTC} falling edge threshold	32.1	32.9	33.7	%
		Hysteresis		2		%
I2C and IRQb						
V_H	Logic High		1.2			V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_L	Logic Low				0.4	V
I_{sink}	SDA, SCL, IRQb sink current capability	BAT=3.8V， VIRQb=0.4V	0.5			mA
t_{irqb}	IRQb low pulse width			256		us

[1]: Not production tested. Guaranteed by design

Typical Characteristics

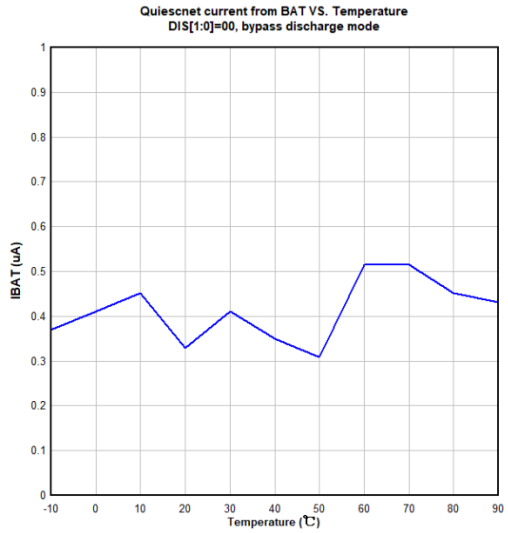


Figure 1. Battery Quiescent Current VS. Junction Temperature, BAT=3.6V

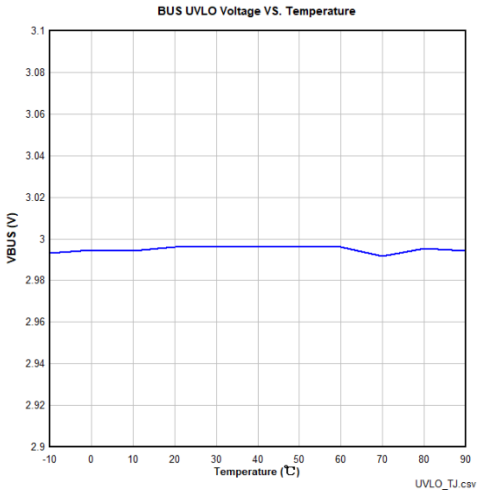


Figure 2. BUS UVLO Threshold VS. Junction Temperature

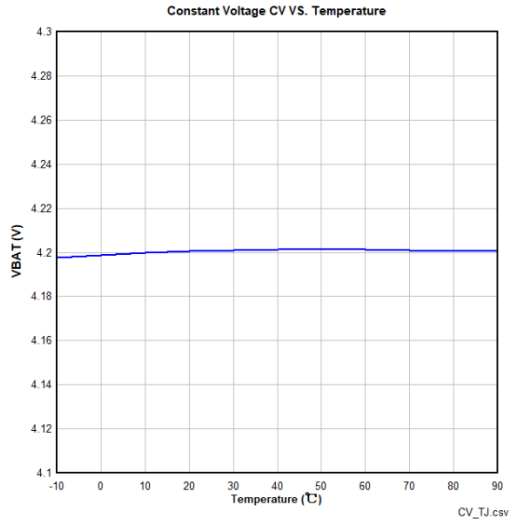


Figure 3. Battery Floating Voltage VS. Junction Temperature

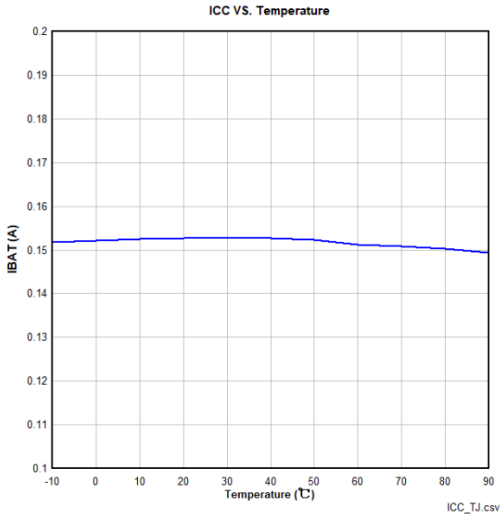
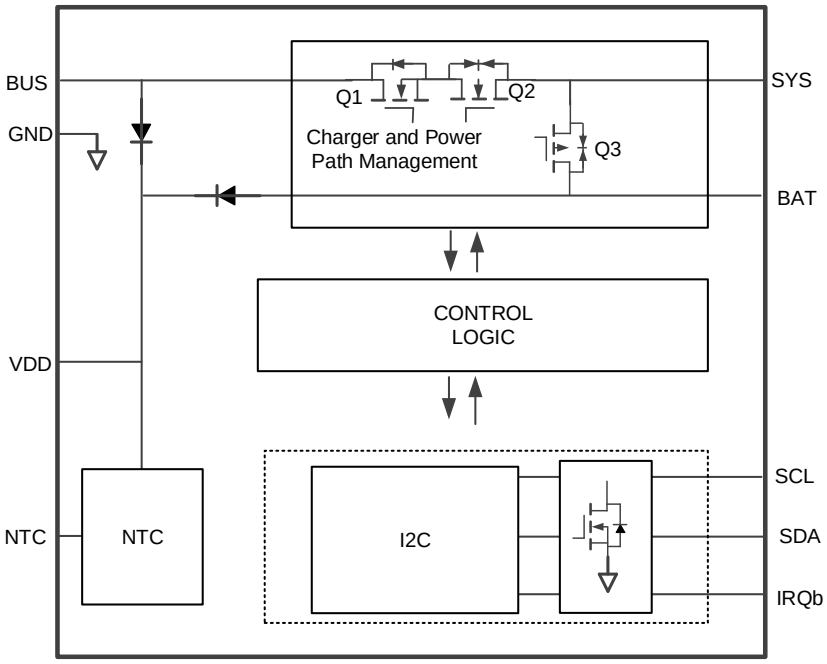


Figure 4. Battery Constant Current VS. Junction Temperature

Functional Block Diagram



Detailed Description

Overview

The LP4081H is a fully integrated linear charger solution with power management function targeting at wearable applications. It contains a standard linear charger to charge the Li-ion battery with an I2C interface and an IRQb interrupt indication. The charger has an ideal-diode mode to achieve high efficiency and low heat performance when fast charge is needed. The power path management function allows the system to be powered from the input voltage even with a dead battery.

When the linear charger is not in operation, the BAT leaks 0.6-μA current.

Input Section

When one of the events below occurs, the LP4081H will perform a power-on reset. All registers will be set to the default values.

- Battery insertion without input voltage
- The input voltage is present without battery

The SoC or MCU can access all the registers after POR.

Under-voltage lockout (UVLO) and over-voltage protection (OVP)

The input block monitors the BUS pin voltage to determine when to turn on the input FETs.

The LP4081H detects an over voltage (OV) event when the Input voltage is higher than OVP threshold. The LP4081H turns off the input FETs immediately.

The LP4081H detects an under voltage (UV) event when the Input voltage is lower than BUS_UVLO threshold. The LP4081H turns off the input FETs as well after a typical 100-us deglitch time.

BUS Powerup

When the input voltage is higher than the UVLO threshold but lower than the OVP threshold, the PGD bit is set and the SYS voltage ramps up after a 1-ms deglitch time. Otherwise, the input FETs remains open until the Input voltage falls to the PGD range.

The input voltage is connected to the SYS after PGD is set. But the charger function is still OFF unless the EN_CHG bit is set by I2C interface.

Reverse-current Protection (RCP) and Forward Regulation

The input FETs integrates a 50mV forward regulation amplifier, when the Input voltage drops to only 50mV higher than the SYS voltage, the input FETs increase the R_{ds,on_bus} to limit the current to SYS. When the Input voltage drops to only 25mV above the SYS voltage, the input FETs turn off to prevent the reverse current from the SYS capacitor.

Current Limit and Short Circuit Protection (SCP)

The input FETs integrate a typical 0.65A current limit function. The LP4081H monitors the input current when the BUS is present. When the SYS is short to GND, the LP4081H enters hiccup mode.

Charge Management

The charger is a typical linear charger with three charging modes, i.e., trickle, constant current (CC), and constant voltage (CV) modes. The EN_CHG bit can enable the charger. The default value at power-on reset is low, which disables the charger.

1. The linear charger starts charging when all the conditions below are valid:

- BUS power up (PGD=1)
- EN_CHG is set by I2C

all the charge related timers are reset when a new charge cycle starts.

2. **Trickle charge:** The trickle-charge voltage threshold is programmable via Vtri bit with 3.0V default value. The LP4081H starts trickle charging when the battery voltage is below the trickle threshold. The trickle-charge current is programmable in the ITERM[2:0] register. If the Vtri is not reached before the trickle charger safety timer(0.75Hr), the charging cycle is terminated forcedly and the TRI_TE status register is set. A low-level pulse is sent out at IRQb pin at the same time.

3. **CC charge:** The LP4081H starts CC charging when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The charging current is determined by ICC[5:0] registers and the ICC_EXT bit register via I2C bus. The CC current is programmable from 10~470mA when ICC_EXT is set to 0 and the range is extended to 25~1175mA when the ICC_EXT bit is set to 1. The default charging current is 800mA and ICC_EXT bit is 1.

   The fast charge safety timer is 3.75Hrs. The TERM_TE bit is set when the CC charging time expires. The charge progress is terminated and the IRQb pin outputs a low-level pulse as well when EN_Term is set to 1.

4. **Power path management**: The minimum system voltage is set by DPM[2:0] register. When the SYS voltage is below DPM[2:0], the charging current reduces until a new balance is reached. Even with a dead battery, the system voltage is regulated above the minimum system voltage.

5. **CV charge:** The LP4081H starts CV charging when the battery voltage rises above the CV threshold. The charging decreases gradually until the charging termination is triggered in this phase. The CV voltage is programmable via the BAT_CV[4:0] register. The default value is 4.2V.

6. **Termination:** When the BAT voltage is higher than the recharge voltage and charge current drops to the termination current, the low-level pulse is sent out from IRQb pin. The charge cycle is terminated immediately when EN_term bit is set to 1, otherwise, the charging continues until fast charge safety timer time expire.

7. **Recharge:** A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage while the BUS is still available. The charging cycle starts again and the safety timer re-counting.

8. **Charge current foldback** : When the die temperature reaches 120 °C, the charger current decreases until a new temperature balance is reached.

9. **NTC management:** An NTC resistor with 1% accuracy and with a beta of 3435 is recommended for LP4081H. The VDD and internal NTC detection circuits are disabled when EN_NTC is set to 0 to reduce the quiescent current. Three thresholds are achieved: 0 °C, 10 °C, and 45 °C temperature threshold detection. The NTC interrupt pulse will be sent when the temperature is crossing these thresholds for SoC to take actions according to the temperature.

   The NTC [2:0] bits are used to indicate the temperature range in the status register. The SoC can change the charging parameters or disable the charging operations by using the control registers.

   The charging function and charger safety timers are forced to be turned off when the temperature is outside the range of 0 °C to 45 °C. The charging function recovers when temperature returns inside the range of 0 °C to 45 °C. The trickle/fast charge safety timers are reset and starts counting again. The NTC[2:0] will be set to 011 when EN_NTC=0.

10. **EN_CHG**: When EN_CHG is set to 0, the charging process is terminated immediately and safety timer counting is reset. When EN_CHG is set to 1 from 0. The charging cycle starts again and the safety timer re-counting.

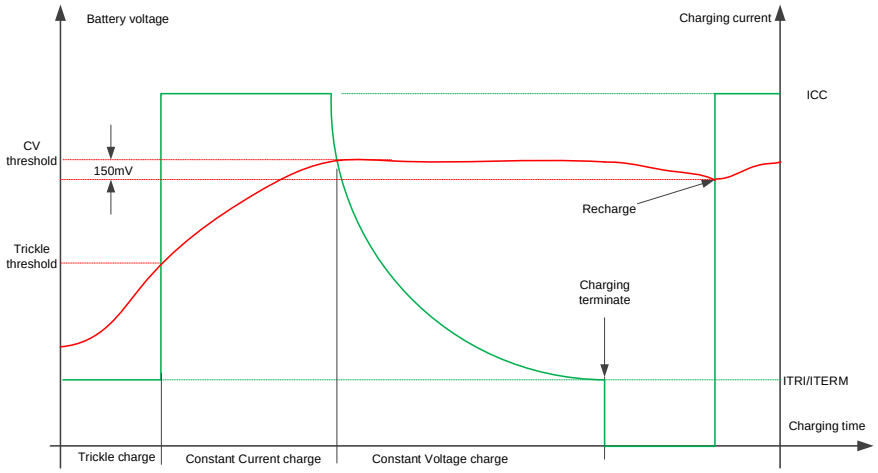


Figure 5. Charging profile

Discharge Management

The LP4081H integrates the power path management function. The SYS is always powered either from the input voltage or the battery. The system voltage drops when the input power source is removed.

BAT_FET control

The LP4081H supports two discharge modes when the input voltage is not present. The BAT_FET can be set to bypass, power down reset and auto mode by configure the DIS[1:0] register. When DIS[1:0] is set to 00, the BATFET is turned on forcedly and works in bypass mode but without current limit function. When DIS[1:0] is set to 01, the BAT_FET is turned OFF for 8s and the SoC can reset itself. When DIS[1:0] is set to 10, the BAT_FET is in auto mode with current limit function.

The BAT_FET can be set to bypass, power down reset and auto mode by one-wire bus as well.

Discharge current limit

The LP4081H supports system current limit function even without the BUS voltage. The maximum current through the BAT_FET is limited. This function is only valid when the DIS[1:0] register is set to 10. The default current limited is 0.44A when the SYS is short to ground. Just the same as the SCP in charge mode, the LP4081H functions a hiccup operation. The current limit is programmable via the register IDIS_LIM[1:0].

Attention should be paid here, the discharge current limit function is disabled when DIS[1:0] is set to 00.

Battery UVLO

When the battery voltage is lower than 3.0V, the discharge function is disabled immediately and the BAT_UV is set. IRQb low pulse is sent.

System reset

The LP4081H integrates two different methods to reset the SoC system.

- Watchdog time out. The LP4081H integrates a typical 40-s watchdog. The LP4081H turns off the input FETs and the BAT_FET for 8s. (Details in WATCHDOG section). All the registers reset to default values after 8s time over.
- Set DIS[1:0] register to 01. The LP4081H turns off the input FETs and the BAT_FET for 8s as well when DIS[1:0] is set to 01 by I2C. All the registers reset to default values after 8s time over.

Standby state

The LP4081H enters standby state with the condition described below is met:

1. The BAT_FET discharge function is configured as bypass mode.

2. EN_WTD is set to 0
3. No input voltage

The LP4081H only consumes 0.6-uA quiescent current in standby state from the battery. Only one wire and I2C registers are active in standby state.

The LP4081H exits standby state immediately with each of the following conditions are met:

1. The battery POR event occurs.
2. The input voltage is present
3. One-wire communication is active.

Shipping mode

The LP4081H supporting shipping mode by setting the SHIP bit (DIS[1:0] =11) by I2C or one-wire communication interface. The DIS[1:0] bits should be set to 10 before entering shipping mode. The LP4081H turns off all the active circuits after a typical 1s deglitch time. The LP4081H only consumes 400nA in shipping mode and a valid 5V BUS exiting the shipping mode.

All the registers are set to the default values after LP4081H enters shipping mode.

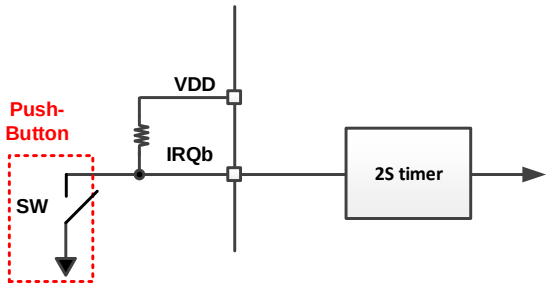


Figure 6. Exit ship mode by IRQb pin

Watchdog

A 40s typical wait time watchdog is integrated. The Bluetooth SoC should write the WTD bit to 1 before time expires.

When the watchdog timer expiration, all the power FETs are forced to be turned off 8s. In this way, the SoC can reset itself. All the registers recover to the default values after watchdog expires.

Once be enabled, the watchdog is always active, either the input voltage or the battery is present. The watchdog can be turned off to save quiescent current by setting EN_WTD bit to 0.

Thermal Shutdown

When the internal junction temperature of LP4081H exceeds the thermal shutdown threshold of 150° C, the LP4081H disables all the power paths. The LP4081H recovers to the default setting after the junction temperature falls to the 130 ° C .

I2C Bus and Interrupt

The LP4081H has an I2C bus with an interrupt IRQb pin and the internal registers. The LP4081H operates as a slave device and the I2C slave address is 6BH (7bit, 1101011), a 1 or 0 should be placed at the end of the address which represents read or write operation. The interrupt pin IRQb is an open-drain output that pulls to low for 256us when an interruptible event happens in the chip. These events are included:

- Input power is present or removed.
- SYS pin short circuit happens
- Trickle charge timer expires

- Fast charge timer expires
- Watchdog timer expires
- charge status changes
- Battery is fully charged
- Battery voltage is UVLO
- NTC cross range

All of the SDA, SCL and IRQb are open-drain outputs. SoC can pull up these pins to the digital IO power rail internally.

DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

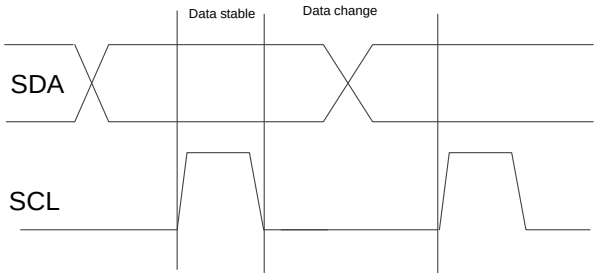


Figure 7. I2C Data validity

Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the SDA line while the SCL is high means a data transfer starts. A rising edge on the SDA line while the SCL is at high means a data transfer stops.

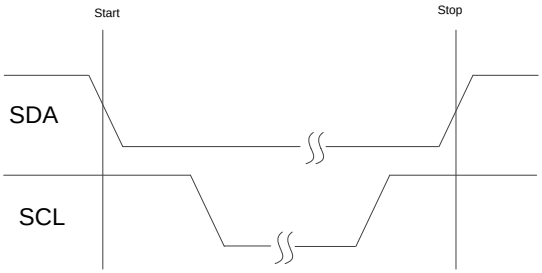


Figure 8. I2C Start and Stop Conditions

Byte format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

Single Byte Read and Write

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 9. Single byte write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK
							8 bit	1bit	1bit
							Data from Address	NACK	STOP

Figure 10. Single byte read

Multi-Read and Multi-Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit							
START	Slave address	0	ACK	Register address	ACK	START							
							8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit
							Data to Address	ACK	Data to Address	ACK	.....	Data to Address	ACK	stop

Figure 11. Multi-byte write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit					
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1					
									8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit
									Data from Address	ACK	Data from Address	ACK	.....	Data from Address	NACK	stop

Figure 12. Multi-byte read

Register Maps

Table 1. Device Registers

Reg Name	Addr		7	6	5	4	3	2	1	0	Def
Status register 0	00H	RO	TRI_TE	TERM_TE	WTD_TE	BAT_UV	SCP	CHG	CHG	PGD	00
Status register 1	01H	RO						NTC	NTC	NTC	00
Mask register 0	02H	RW		mBAT_UV	mEOC	mSCP	mCHG	mPGD	mTimer	mNTC	00
Control register 0	03H	RW			ICC_EXT	IDSI_LIM	IDIS_LIM	IIN_LIM	DIS	DIS	3E
Control register 1	04H	RW	ITERM	ITERM	ITERM	BAT_CV	BAT_CV	BAT_CV	BAT_CV	BAT_CV	E4
Control register 2	05H	RW	EN_CHG	VTRI	ICC	ICC	ICC	ICC	ICC	ICC	F0
Control register 3	06H	RW	WTD	EN_WTD	EN_NTC	EN_Tri_Timer	EN_Term	DPM	DPM	DPM	2B

Note:**RO**: read only; **RC**: read and clear; **RW**: read and write

Status Register 0 /Address: 00H (default: 0x00)

Table 2. Status register 0

Bit	Symbol	Description	Read/Write	Default
7	Trickle_TE	=1 Trickle charge timer expiration	r	0
6	Term_TE	=1 Fast charge timer expiration	r	0
5	WTD_TE	=1 Watchdog timer expiration	r	0
4	BAT_UV	=1 battery UVLO	r	0
3	SCP	=1 SYS is short circuit	r	0
2	CHG	00: not in charging mode, 01: trickle	r	0
1	CHG	10: CC/CV 11: EOC	r	0
0	PGD	=1 when input is between UVLO and OVP.	r	0

Status Register 1 /Address: 01H (default: 0x03)

Table 3. Status register 1

Bit	Symbol	Description	Read/Write	Default
2	NTC	000: not valid, 001: <0 °C		0
1	NTC	010:0-10 °C, 011: 10~45 °C		1
0	NTC	100: >45 °C, 101/ 110/111: not valid		1

Interrupt Mask Register/Address: 02H (default: 0x00)

Table 4. Interrupt mask register

Bit	Symbol	Description	Read/Write	Default
7		reserve	r/w	0
6	mbat_uv	Mask interrupt	r/w	0
5	meoc		r/w	0
4	mscp		r/w	0
3	mCHG		r/w	0
2	mPGD		r/w	0
1	mTimer		r/w	0
0	mNTC		r/w	0

Control Register 0/Address: 03H (default: 0x3E)

Register 03H sets masks for interrupts described in the interrupt register above.

Table 5. Control Register0

Bit	Symbol	Description	Read/Write	Default
7		reserve		0
6		reserve		0
5	ICC_EXT	=1, All the charge related current extension by 2.5 times, including: trickle/CC/termination current =0, default setting, no extension function		1
4	IDIS_LIM	discharge current limit		1
3	IDIS_LIM	00: 440mA 01: 1A 10:2A 11: 3A		1
2	IIN_LIM	input current limit =1: 1.5A, =0: 650mA		1
1	DIS[1]	BAT_FET operation mode control:	r/w	1
0	DIS[0]	00: BAT_FET bypass mode, 01: SYS power down 8s, 10: auto mode, 11: ship mode	r/w	0

Control Register 1/Address: 04H (default: 0xE4)

Table 6. Register 3

Bit	Symbol	Description	R/W	Default
7	Iter[2]	Trickle and Termination current set:	r/w	37.5mA
6	Iter[1]	000:1mA, 001:3 mA, 010:5 mA, 011:7 mA, 100:9 mA	r/w	111
5	Iter[0]	101:11 mA, 110:13 mA, 111:15 mA All these current will be X 2.5 times when the ICC_EXT is set to 1	r/w	
4	BAT_CV[4]	Battery CV voltage set:	r/w	4.2V
3	BAT_CV[3]	00000:4.0V, 00001:4.05V, 00010:4.1V,00011:4.15V, 00100:4.2V,	r/w	00100
2	BAT_CV[2]	00101:4.22V,00110:4.24V,00111:4.26V, 01000:4.28V,01001:4.3V	r/w	

1	BAT_CV[1]	01010:4.32V,01011:4.34V,01100:4.35V,01101:4.36V, 01110:4.38V 01111:4.4V,10000:4.42V,10001:4.44V, 10010:4.46V,10011:4.48V, 10100:4.5V, 10101~1111: not valid	r/w	
0	BAT_CV[0]		r/w	

Control Register 2/Address: 05H (default: 0XF0)

Table 7. Register 4

Bit	Symbol	Description	R/W	Default
7	EN_CHG	=1: Charge enable. =0: Charge disable	r/w	1
6	VTRI	Trickle charge threshold set: =1: 3.0V =0:2.8V	r/w	1
5	ICC[5]	Constant current set: 000000:25 mA,000000~100010, 12.5mA/step, 25~450mA 100011:475mA, 10011~111111, 25mA/step, 425~1175mA All the current is reduced to 40% ICC if ICC_EXT bit is set to 0	r/w	800mA 110000
4	ICC[4]		r/w	
3	ICC[3]		r/w	
2	ICC[2]		r/w	
1	ICC[1]		r/w	
0	ICC[0]		r/w	

Control Register 3/Address: 06H (default: 0x2B)

Table 8. Register 5

Bit	Symbol	Description	R/W	Default
7	WTD	Write WTD 1 will reset watchdog timer SoC need write this bit to 1 before watchdog timer count out.	r/w	0
6	EN_WTD	=1 watchdog function is enabled =0 watchdog function is disbaled	r/w	0
5	EN_NTC	=1 NTC circuits are enabled =0 NTC circuits are disabled	r/w	1
4	EN_Tri_Timer	=1 enable 0.75Hr trickle charge safety timer =0 disable 0.75Hr trickle charge safety timer	r/w	0
3	EN_Term	=1 stop charging after EOC, =0 continue charging after EOC until 3.75Hr safety timer time expiration	r/w	1
2	DPM[2]	VSYS DPM threshold: 000:3.0V, 001:3.2V, 010:3.4V, 011:3.6V, 100:3.8V, 101:4.0V, 110:4.2V, 111:4.4V	r/w	011
1	DPM[1]		r/w	
0	DPM[0]		r/w	

Application Information

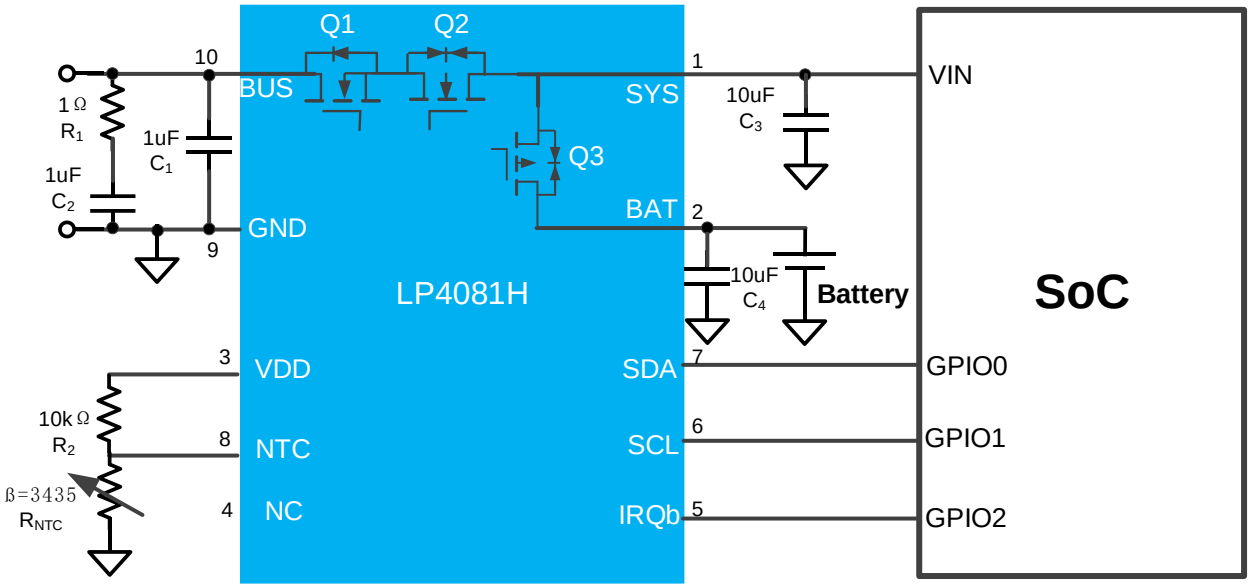


Figure 13. Typical Application Schematic

A typical application consists of the multi-function-in-one power management IC of LP4081H and a host SoC. When powering up in default mode, the battery CV voltage of LP4081H is 4.2V, the constant charging current is 800mA, the termination current and trickle charge current is 37.5mA. The minimum SYS voltage is 3.6V. The SoC can change all the default values by I2C interface.

Capacitor selection

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the BUS, BAT, and SYS pin to the GND pin. The BUS capacitor C_1 should be 25V rating with minimum 1uF capacitance. The BAT capacitor C_4 should be at least 6.3V rating with minimum 10uF capacitance. The SYS capacitor C_3 should be at least 6.3V rating with minimum 10uF capacitance.

NTC Design

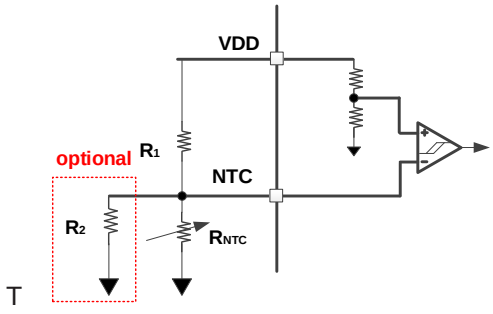


Figure 14. NTC circuit

As all the trigger point thresholds of the internal NTC comparators are well design with a certain type of NTC resistor, an 10-kΩ NTC resistor with 1% accuracy and with a beta of 3435 is recommended. The R1 should be set to 10-kΩ to cooperate with the 10-kΩ NTC resistor. All the thresholds can be found in the electrical characteristics table. An additional

resistor in parallel with the NTC resistor can help adjust the temperature trigger point. The following equations help adjusting the NTC thresholds.

$$R2 = \frac{0.404 * R_{NTC_{HOT}} * R_{NTC_{COLD}}}{0.0878 * R_{NTC_{COLD}} - 0.4918 * R_{NTC_{HOT}}}$$

$$R1 = 0.364 * (\frac{R2 * R_{NTC_{COLD}}}{R2 + R_{NTC_{COLD}}})$$

For example, when the charge function is needed in the 0C~60C temperature range, the RNTC_HOT is 3.02-kΩ while the RNTC_COLD is 27.5-kΩ. The calculated R2 is 35.8-kΩ and the R1 is 5.66-kΩ.

Application Waveforms

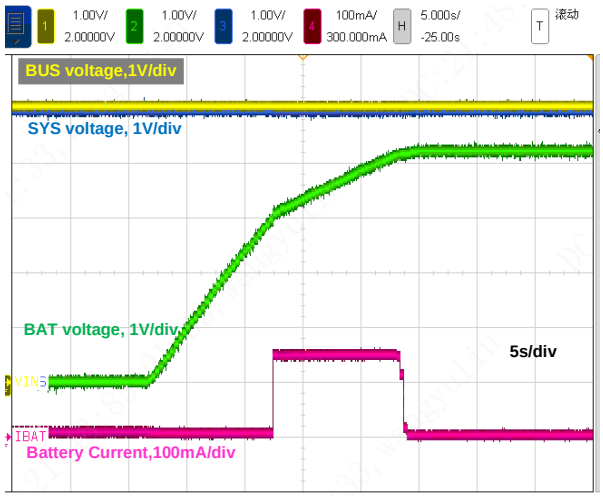


Figure 15. Battery Charging Curve

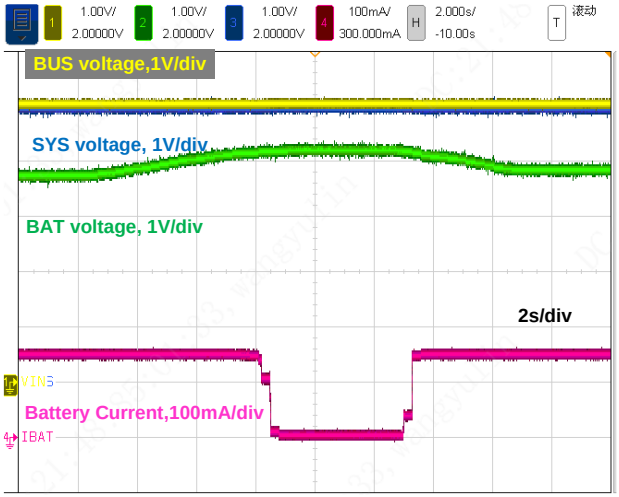


Figure 16. Auto-Recharge

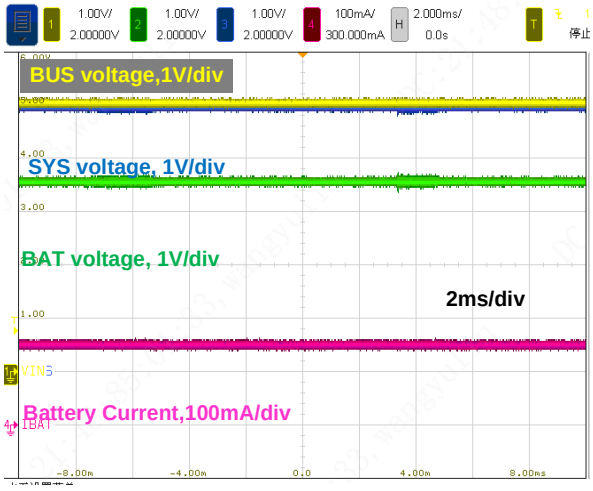


Figure 17. CC Steady State

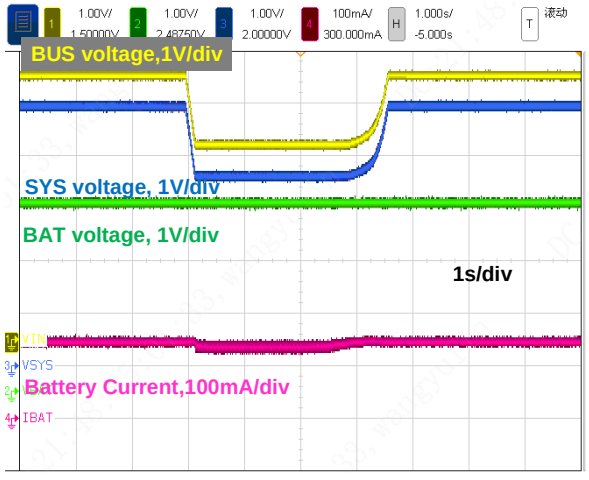


Figure 18. VIN Based PPM

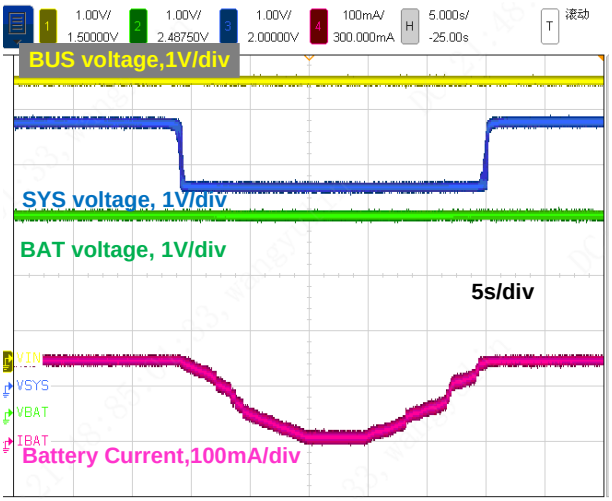


Figure 19. Input Current Limit Based PPM

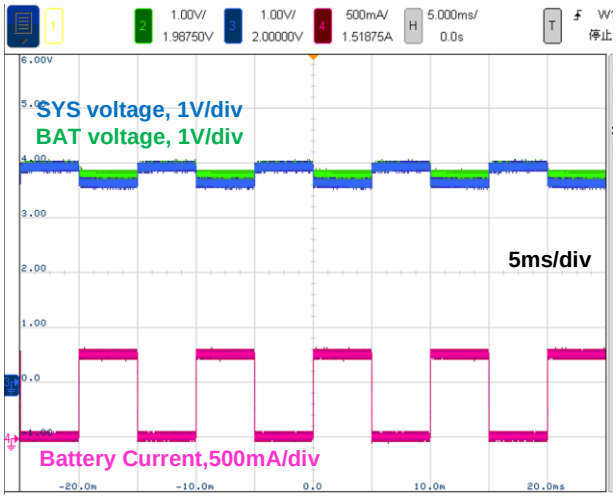


Figure 20. SYS Load Transient, 0A-0.8A-0A, BAT=4.0V, bypass mode

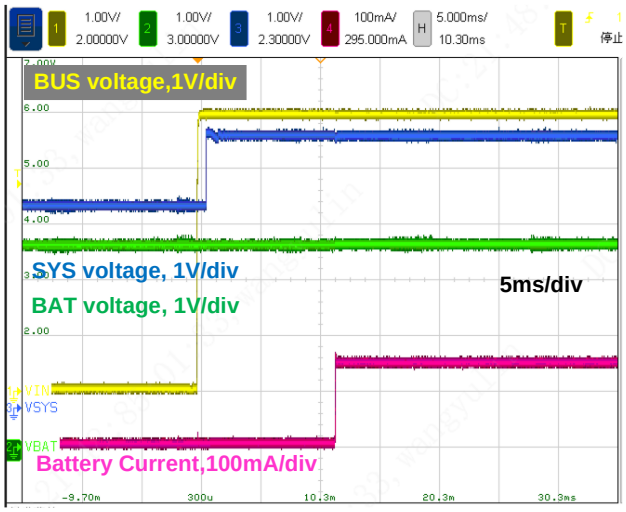


Figure 21. VIN Power Up

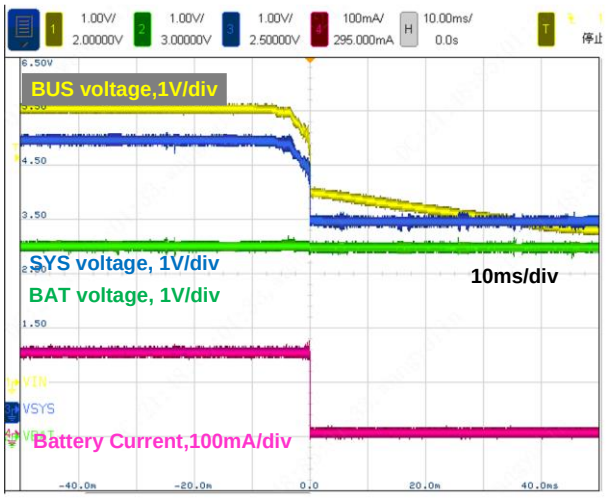


Figure 22. VIN Power Down

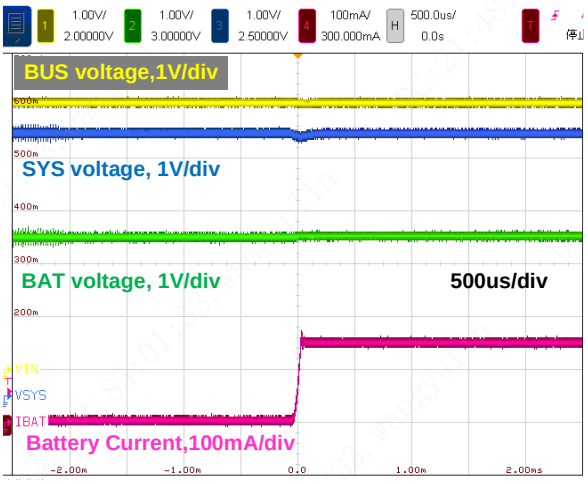


Figure 23. Charge Enable

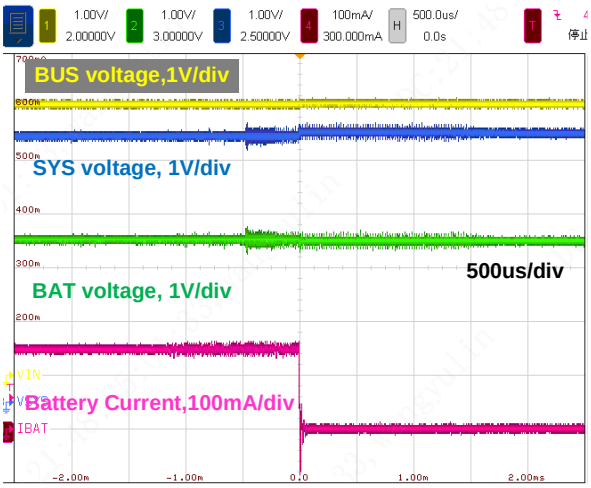


Figure 24. Charge Disable

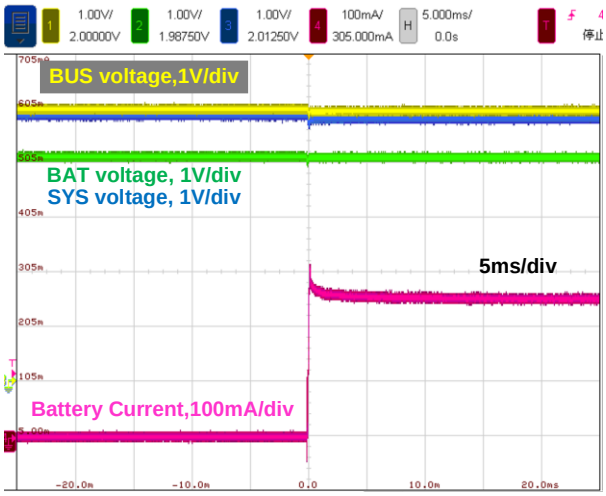


Figure 25. Battery Insert

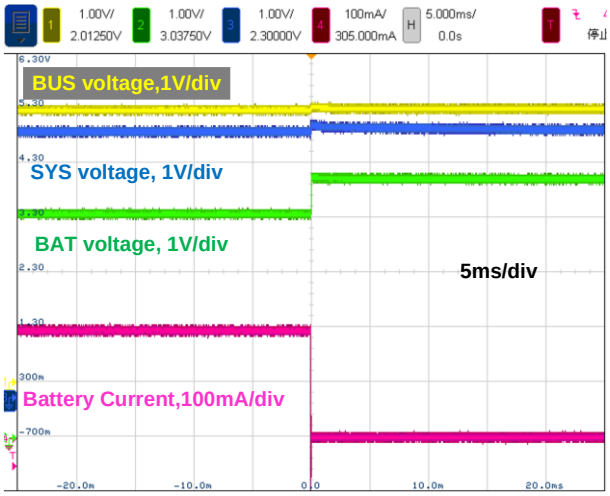


Figure 26. Battery Removal

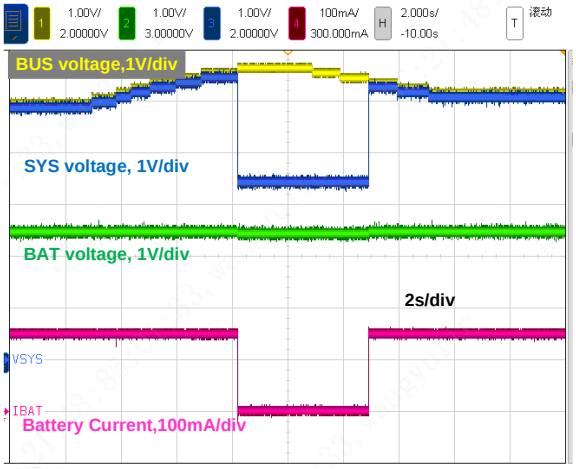


Figure 27. VIN OVP and recover

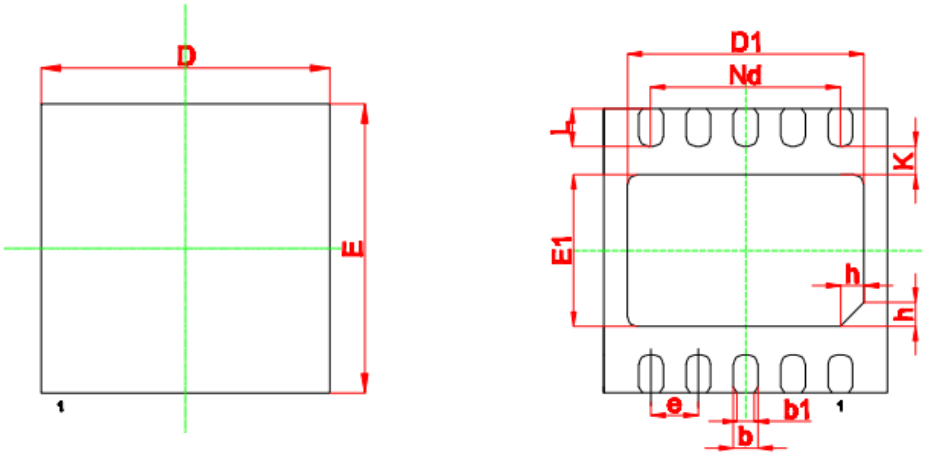
PCB Layout Guidelines

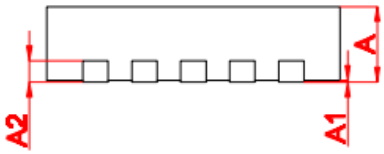
Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

Packaging Information

3x3 DFN package





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
* A1	0.00	0.02	0.05
* b	0.25	0.25	0.30
A2		0.203REF	
* D	2.90	3.00	3.10
* E	2.90	3.00	3.10
* D1	2.40	2.50	2.60
* E1	1.45	1.55	1.65
* e		0.50 BSC	
h	0.20	0.25	0.30
Nd		2.00 BSC	
b1	0.16	0.18	0.20
* k	0.20	0.30	0.35
* L	0.30	0.40	0.50

Revision History

Revision	Date	Change Description
Rev 1p0	10/5/2022	Release Version 1.0