15W Full Bridge With Dual Channel LDO

General Description

LP1140 is a highly integrated full bridge power IC optimized for wireless power transmitter solutions. The device integrates all critical functions such as high-efficiency power FETs, low EMI FET driver, bootstrap circuit, 3.3V and 5V LDO and lossless current measurement.

LP1140 also includes protection functions such as input under-voltage lockout, short-circuit protection, and thermal shutdown. These provisions further enhance the reliability of the total system solution.

The LP1140 are available in the industry standard QFN-20 packages.

Order Information

LP1140 □□ □

- □: F: Pb-Free
- □□: Package Type QV: QFN-20

Features

- Up to 24V DC VIN voltage
- 4.2V to 15V supply voltage(PVINX)
- Output Power: 15W
- Integrated High Efficiency Full Bridge FETs
- Integrated FET Driver Optimized for Low EMI
- Integrated 3.3V/5V LDO to Bias External Circuit
- Input Under-Voltage Lockout
- Short-Circuit Protection
- Thermal Shutdown
- Available in 4mm × 4mm QFN-20 Package

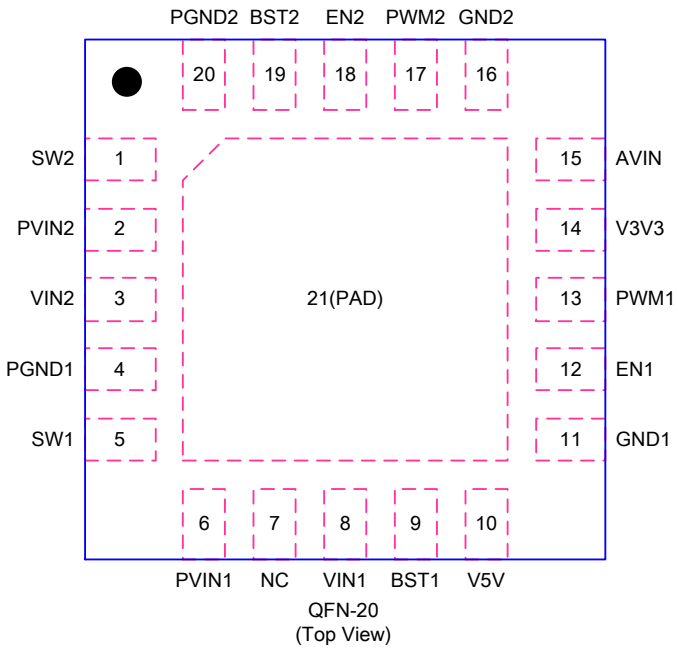
Marking Information

Device	Marking	Package	Shipping
LP1140QVF	LP1140 YWXXX	QFN-20	3K/REEL
Y:Production year W:Production period X:Production batch			

Applications

- ✧ Wireless Power Transmitter
- ✧ Motor Drivers

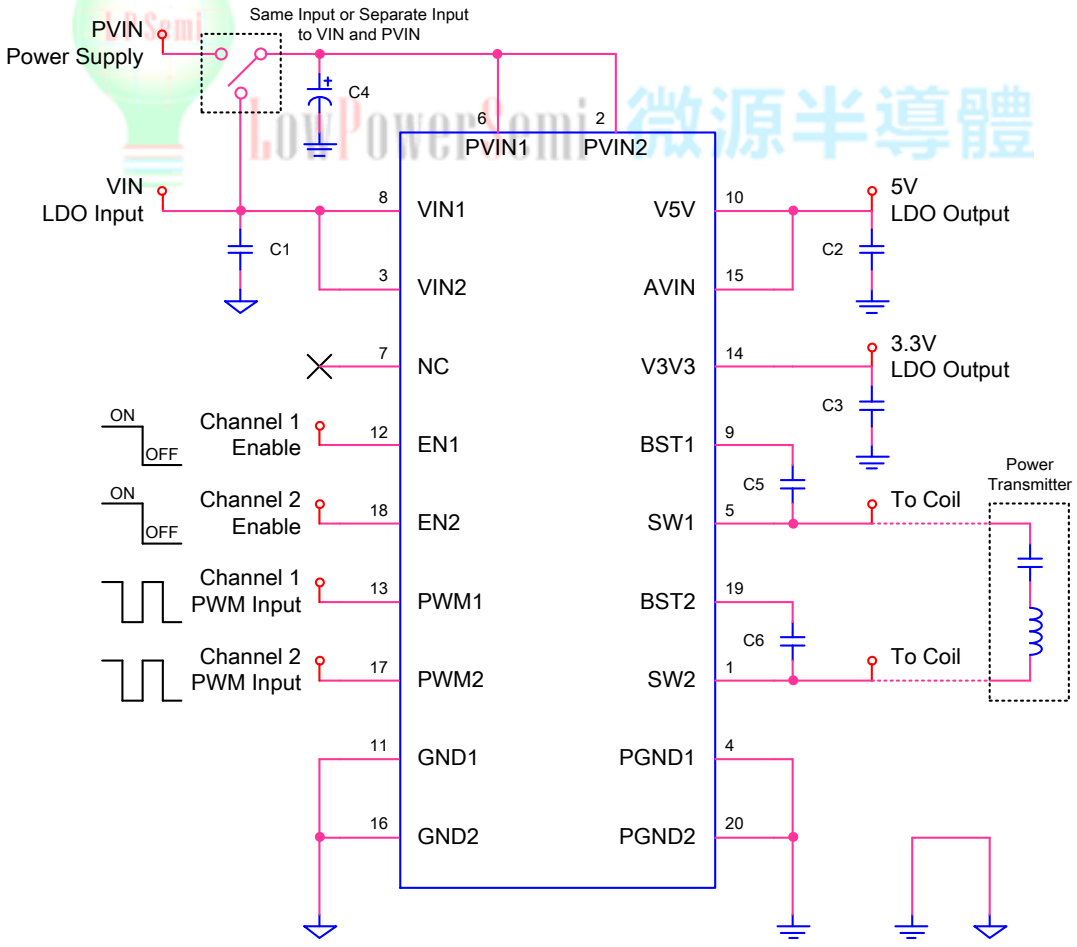
Functional Pin Description

Package Type	Pin Configurations
QFN-20	

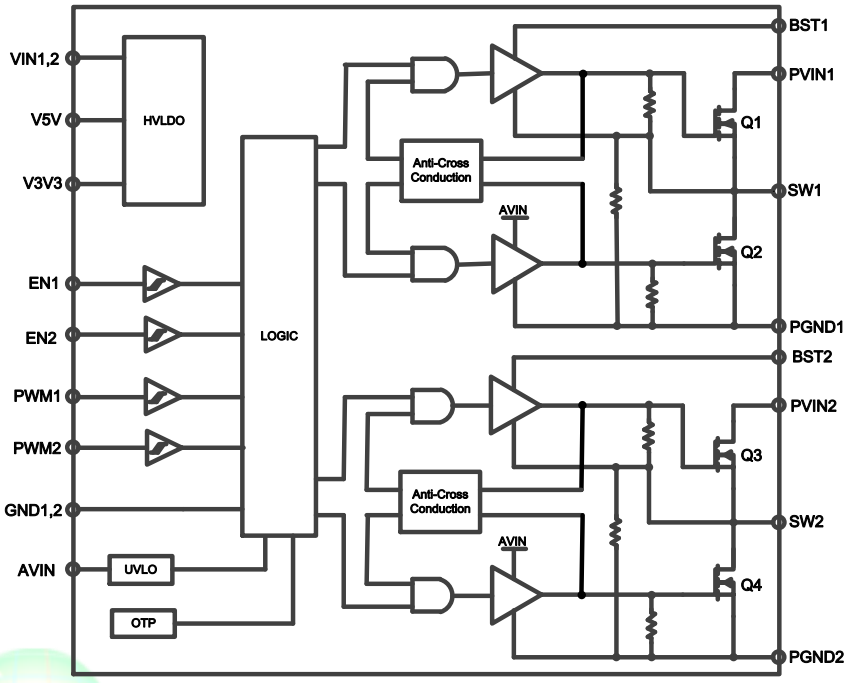
Pin	Name	Description
1	SW2	Switch node of half bridge 2. Connect the High Side and Low Side power NMOS inside the half bridge 2.
2	PVIN2	The power supply input pin of the half bridge 2. Power is supplied to the internal High Side power NMOS of the half bridge 2. Place the external capacitor as close as possible to the chip.
3	VIN2	Power supply input pin 2. Power is supplied to the 3.3V LDO. Place the external capacitor as close as possible to the chip.
4	PGND1	The power ground of the half bridge 1.
5	SW1	Switch node of half bridge 1. Connect the High Side and Low Side power NMOS inside the half bridge 1.
6	PVIN1	The power supply input pin of the half bridge 1. Power is supplied to the internal High Side power NMOS of the half bridge 1. Place the external capacitor as close as possible to the chip.
7	NC	No connection.
8	VIN1	Power supply input pin 1. Power is supplied to the 5V LDO and the half bridge 1 Gate Driver. powered by. Place the external capacitor as close as possible to the chip.
9	BST1	Bootstrap input pin for half bridge 1. A capacitor needs to be connected to the BST1 and SW1 pins. The recommended value for the capacitor is 0.1uF~1uF. Try to be close to the chip.
10	V5V	Output pin for internal 5V LDO. It is recommended to connect a 10uF ceramic capacitor to ground, placed close to the chip.
11	GND1	The signal ground of the half bridge 1.

12	EN1	The enable logic input pin of half bridge 1. The high level enables the chip, and the low level makes SW1 high impedance.
13	PWM1	Half bridge 1 PWM logic input. Controls the power output of the SW1 pin.
14	V3V3	Output pin for internal 3.3V LDO. It is recommended to connect a 10uF ceramic capacitor to ground, placed close to the chip.
15	AVIN	The power input pin of the internal gate driver of the half bridge. Place the external capacitor as close as possible to the chip.
16	GND2	The signal ground of the half bridge 2.
17	PWM2	Half bridge 2 PWM logic input. Controls the power output of the SW2 pin.
18	EN2	The enable logic input pin of half bridge 2. The high level enables the chip, and the low level makes SW1 high impedance.
19	BST2	Bootstrap input pin for half bridge 2. A capacitor needs to be connected to the BST2 and SW2 pins. The recommended value for the capacitor is 0.1uF~1uF. Try to be close to the chip.
20	PGND2	The power ground of the half bridge 2.

Typical Application Circuit



Function Diagram



Absolute Maximum Ratings

- ✧ VIN1,VIN2 to GND ---------- -0.3V to 30V
- ✧ AVIN to GND ---------- -0.3V to 7V
- ✧ PVIN1,PVIN2 to GND---------- -0.3V to 18V
- ✧ BST1, BST2 to SWN ---------- -0.3V to 7V
- ✧ SW1, SW2 to GND---------- -0.3V to 18V
- ✧ EN1, EN2 to GND ---------- -0.3V to 20V
- ✧ PWM1, PWM2 to GND ---------- -0.3V to 6.5V
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads,10 sec) ---------- 260℃
- ✧ Storage Temperature ---------- -55℃ to 150℃
- ✧ Operating Ambient Temperature Range ---------- -40℃ to 85℃

Note1: All voltages are with respect to PGND except where noted.

Note2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note3: This device is ESD sensitive. Use standard ESD precautions when handling.

Thermal Information

- ✧ Maximum Power Dissipation (P_D,T_A=25℃) ---------- 2W
- ✧ Junction to Ambient, θ_{JA}---------- 50℃/W

Note4: 2 layer board, 1 in2 Cu, 1 oz thickness.

Electrical Characteristics

(V_{IN}=12V T_A=25°C, V_{AVIN}=5V, unless otherwise noted. The electrical characteristics of the following table default to channel 1, and channel 2 is the same as channel 1)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply						
Supply Voltage Range	V_{IN}		4.2		24	V
Supply Current	I_{SYS}	V_{SW}=12V, V_{PWM}=0V, V_{EN}=3V		0.9		mA
		V_{SW}=12V,V_{PWM}=3V, V_{EN}=3V		1.4		mA
EN Input						
Input Voltage High	V_{EN_HI}		2.0			V
Input Voltage Low	V_{EN_LO}				0.8	V
Hysteresis	V_{EN-HYS}			400		mV
Input Current	I_{EN}			3		μA
EN pull-down resistor	R_{EN}			1.5		MΩ
PWM Input						
Input Voltage High	V_{PWM_HI}		2.0			V
Input Voltage Low	V_{PWM_LO}				0.8	V
Hysteresis	–			400		mV
Input Current	I_{PWM}	No internal pull-up or pull-down resistors	-1.0		1.0	μA
PWM pull-down resistor	R_{PWM}			260		KΩ
5V LDO Regulator						
Output Voltage		V_{IN}=6V, I_{V5V}=0mA		5		V
Dropout Voltage	$V_{DROP-V5V}$	I_{V5V}=100mA		240		mV
		I_{V5V}=200mA		500		mV
Current limit	V_{5V_ILM}			300		mA
Linear Regulation		V_{IN}=6V to 12V, I_{OUT}=1mA		0.3		%
Load Regulation		V_{IN}=12V, 1mA < I_{OUT}<200mA		2		%
3.3V LDO Regulator						
Output Voltage		V_{IN}=6V, I_{V3V3}=0mA		3.3		V
Dropout Voltage	$V_{DROP-V3V3}$	I_{V3V3}=100mA		240		mV
		I_{V3V3}=200mA		500		mV
Current limit	V_{3V3_ILM}			300		mA
Linear Regulation		V_{IN}=6V to 12V, I_{OUT}=1mA		0.5		%
Load Regulation		V_{IN}=12V, 1mA < I_{OUT}<200mA		2		%
Under Voltage Lockout						
UVLO Startup(AVIN)	V_{UV}			3.8		V
Hysteresis	V_{UV-HYS}			0.4		V
MOSFET STATIC Characteristics						
High-Side MOS Rdson	R_{DS_H}	I_{DS}=1A		65		mΩ
Low-Side MOS Rdson	R_{DS_L}	I_{DS}=1A		65		mΩ
Temperatrue protection						
Over Temperature Protection	T_{OTP}			150		℃
Over Temperature Protection Hysteresis	T_{OTP_HYS}			20		℃

Applications Information

The LP1140 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU. The LP1140 has 4 power input pins. VIN1 and VIN2 is connected to the power FETs of 5V and 3.3V LDOs. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN1, VIN2, PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VINX is from 4.2V to 24V. An Under-voltage Lockout(UVLO) circuit monitors the voltage of AVIN pin and disable the IC operation when AVIN voltage falls below the UVLO threshold of 3.8V typically.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the LP1140 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

Enable function

The EN1 and EN2 pins can control the enable and disable of half-bridge 1 and half-bridge 2, respectively. When EN1 is high, SW1 is enabled. When EN1 is low, SW1 is in a high impedance state. EN2 controls SW2 in the same way.

5V and 3.3V LDO

The LP1140 has 2 integrated low-dropout voltage regulators which powered from VIN and supply regulated 5V and 3.3V voltage, and the output of the 5V LDO can be used as AVIN input. The output current capability is 300mA. These LDO can be used to bias the supply voltage of external transmitter controller or MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the AVIN pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM control

The LP1140 integrate full bridge power stage with 65mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 400KHz for different applications which is completely compatible with WPC's frequency requirement from 100KHz to 205KHz.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q2's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by AVIN power supply rail.

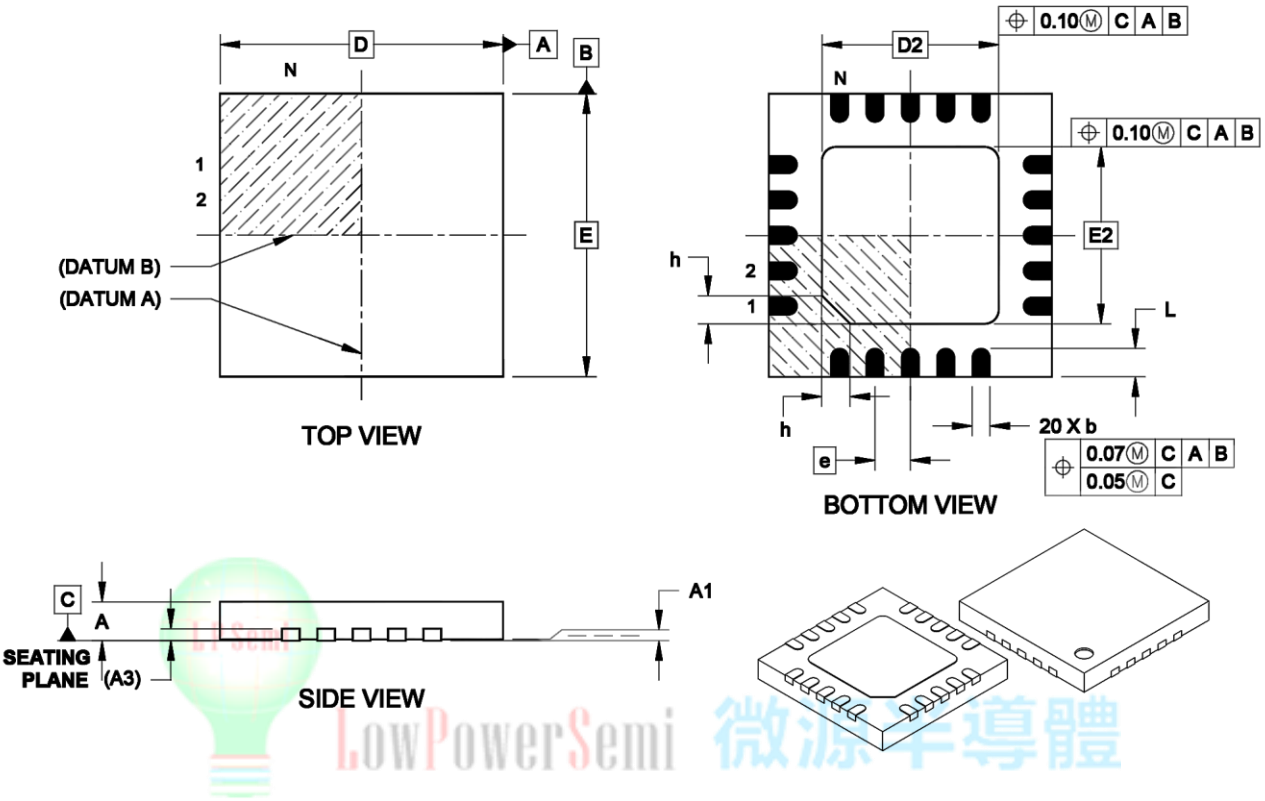
PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Thermal shutdown

The LP1140 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 150℃ the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 130 ℃ , then the device restarts.

Packaging Information

QFN-20(4*4)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 BSC	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	h	0.30	0.35	0.40