



LPM9017 30V/4A

P-Channel Enhancement Mode Field Effect Transistor

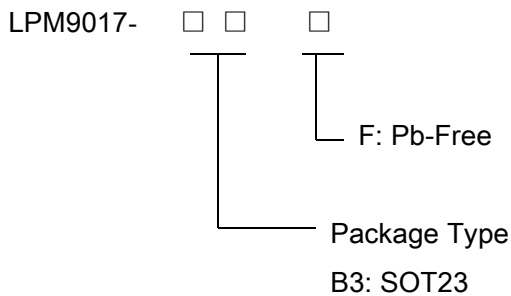
General Description

The LPM9017 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Ordering Information



Features

- -30V/-4.0A, $R_{DS(ON)} < 58m\Omega$ (typ.)@VGS=-10V
- -30V/-3.0A, $R_{DS(ON)} < 68m\Omega$ (typ.)@VGS=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOT23 Package

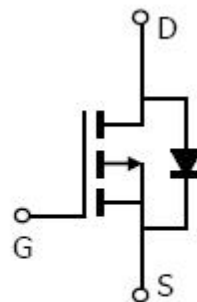
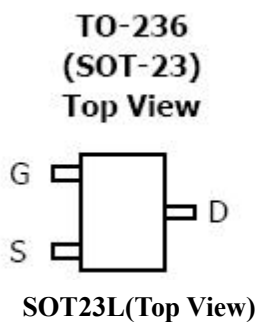
Applications

- ◇ Portable Media Players
- ◇ Cellular and Smart mobile phone
- ◇ LCD
- ◇ DSC Sensor
- ◇ Wireless Card

Marking Information

Device	Marking	Package	Shipping
LPM9017	A1XX	SOT23	3K/REEL

Pin Configurations





Absolute Maximum Ratings

$T_A=25^{\circ}\text{C}$ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current A	$T_A=25^{\circ}\text{C}$	I_D	-4	A
	$T_A=70^{\circ}\text{C}$		-3.5	
Pulsed Drain Current B		I_{DM}	-25	
Power Dissipation A	$T_A=25^{\circ}\text{C}$	P_D	1.4	W
	$T_A=70^{\circ}\text{C}$		0.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

Thermal Characteristics

Parameter		Symbol	Typ.	Max.	Units
Maximum Junction-to-Ambient A	$t \leq 10\text{s}$	$R_{\theta JA}$	70	90	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Ambient A	Steady-State		100	125	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Lead C	Steady-State	$R_{\theta JL}$	63	80	$^{\circ}\text{C}/\text{W}$



Functional Pin Description

Symbol	Parameter	Condition	Min	Typ.	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -250\mu A, V_{GS} = 0V$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$ $T_J = 55^\circ C$			-1 -10	μA
I_{GSS}	Gate-Body leakage current	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.6		-1.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10V, I_D = -4A$		55	58	m Ω
		$V_{GS} = -4.5V, I_D = -3A$		64	68	
		$V_{GS} = -2.5V, I_D = -2A$		85	95	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5V, I_D = -4A$		10		S
V_{SD}	Diode Forward Voltage	$I_S = -1A, V_{GS} = 0V$		-0.7	-1	V
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -15V,$ $f = 1MHz$		680		pF
C_{oss}	Output Capacitance			320		pF
C_{rss}	Reverse Transfer Capacitance			65		pF
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	$V_{GS} = -10V, V_{DS} = -15V,$ $I_D = -4A$		7		nC
Q_{gs}	Gate Source Charge			13		nC
Q_{gd}	Gate Drain Charge			1.8		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS} = -10V, V_{DS} = -15V,$ $R_L = 3.6\Omega,$ $R_{GEN} = 6\Omega$		12	18	nS
t_r	Turn-On Rise Time			3	7	
$t_{D(off)}$	Turn-Off DelayTime			34	42	
t_f	Turn-Off Fall Time			3	7	



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

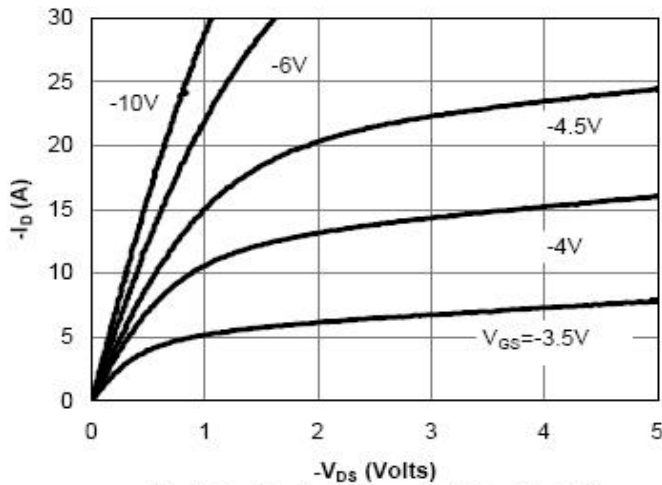


Fig 1: On-Region Characteristics (Note E)

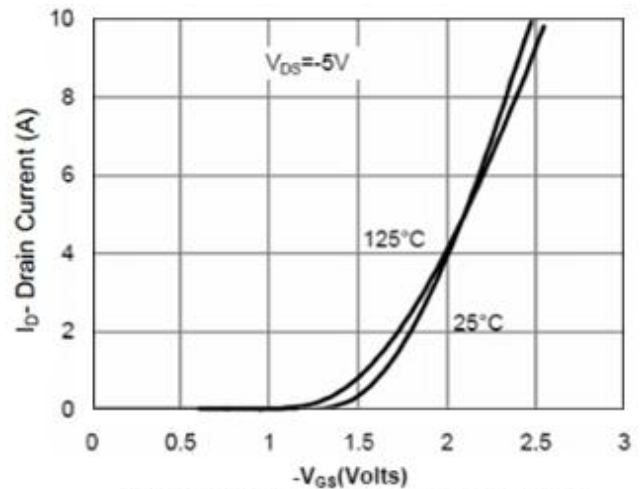


Figure 2: Transfer Characteristics (Note E)

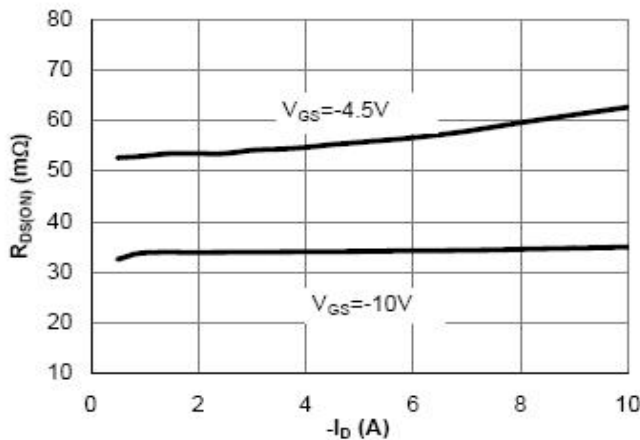


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

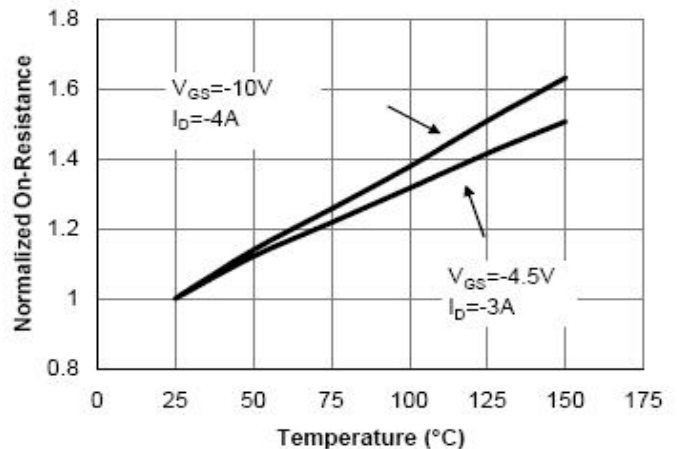


Figure 4: On-Resistance vs. Junction Temperature (Note E)

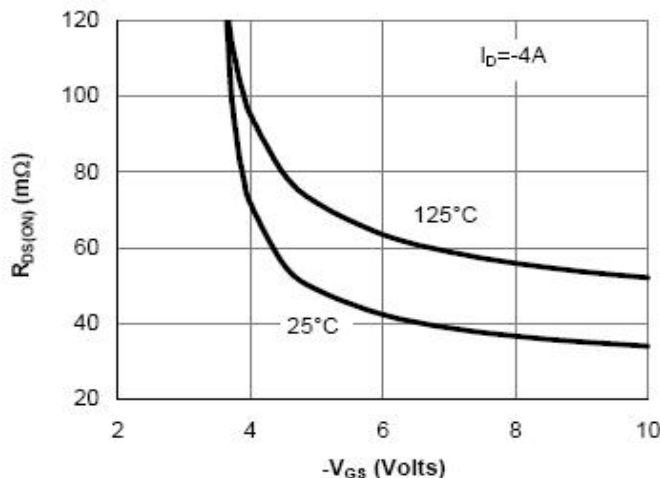


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

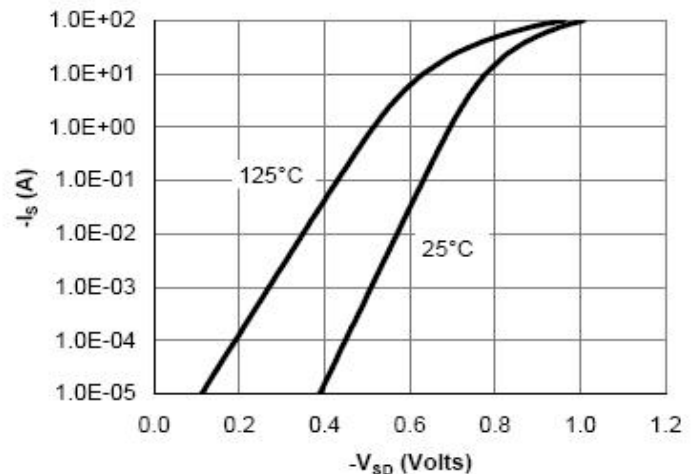


Figure 6: Body-Diode Characteristics (Note E)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

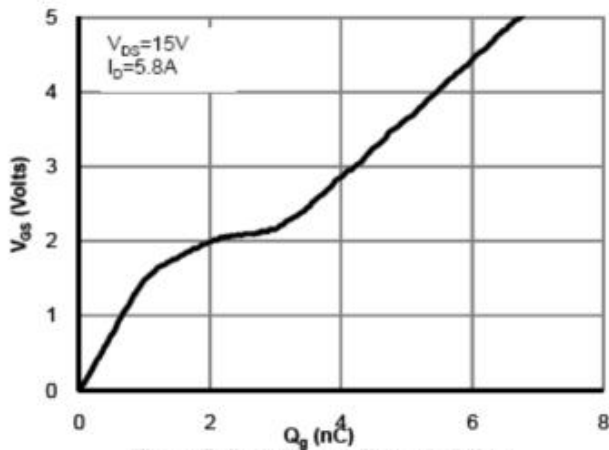


Figure 7: Gate-Charge Characteristics

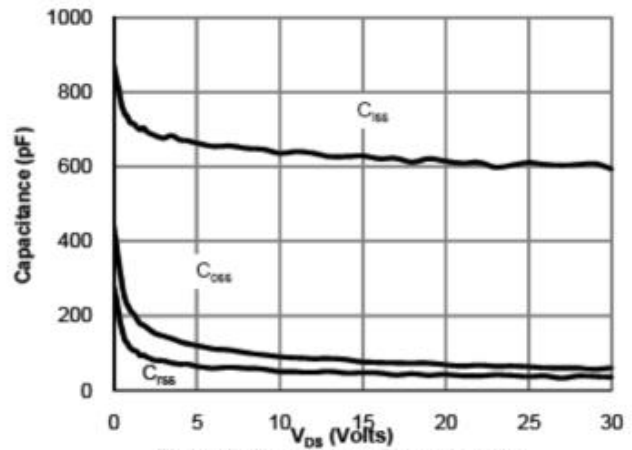


Figure 8: Capacitance Characteristics

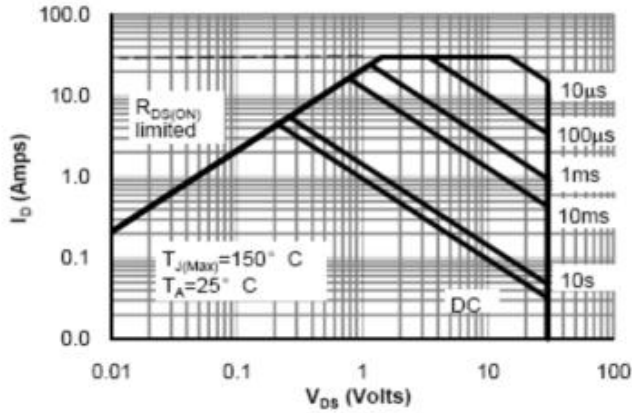


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

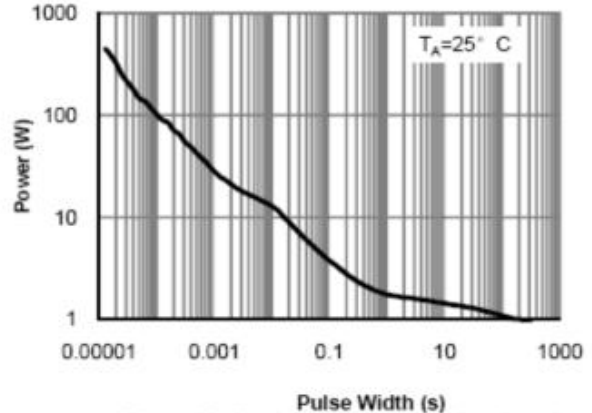


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

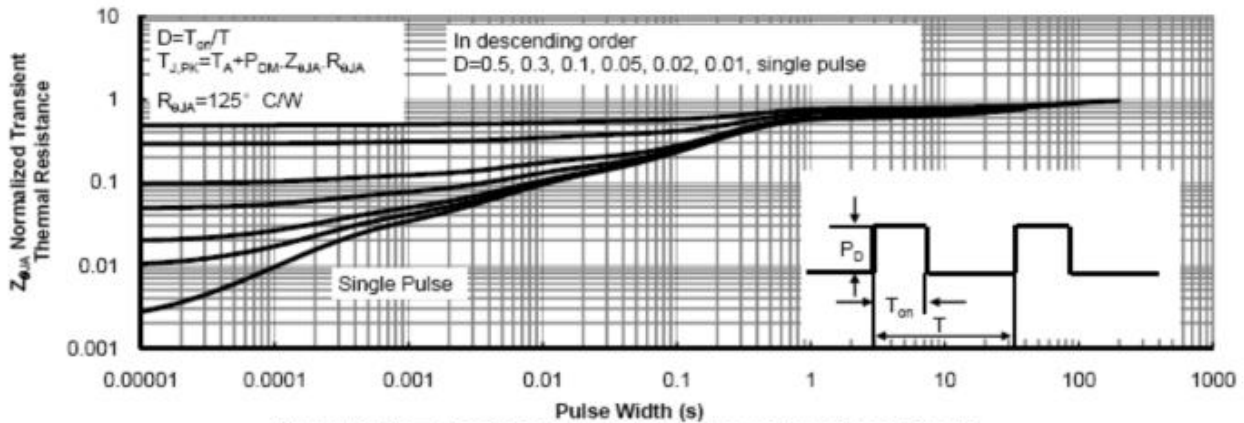
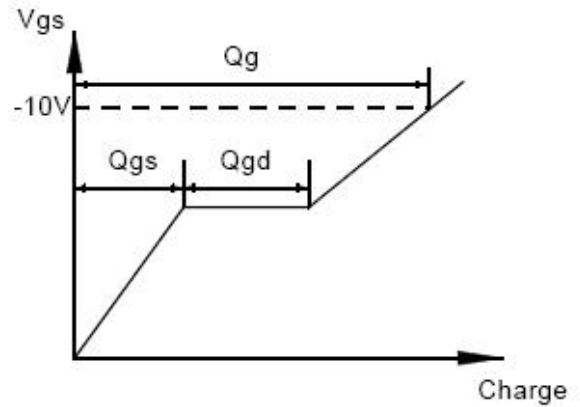
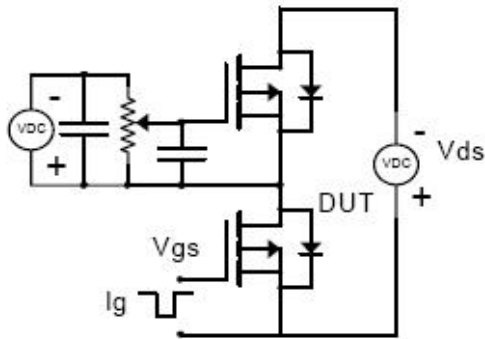


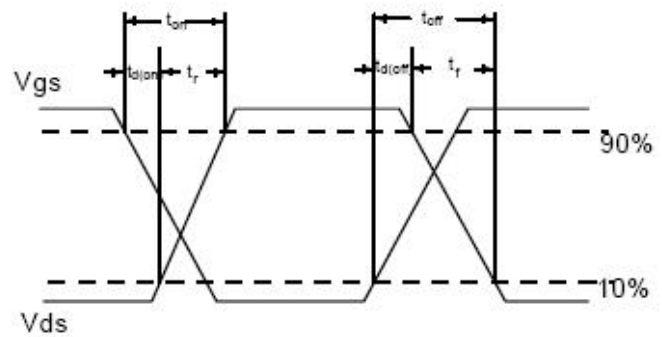
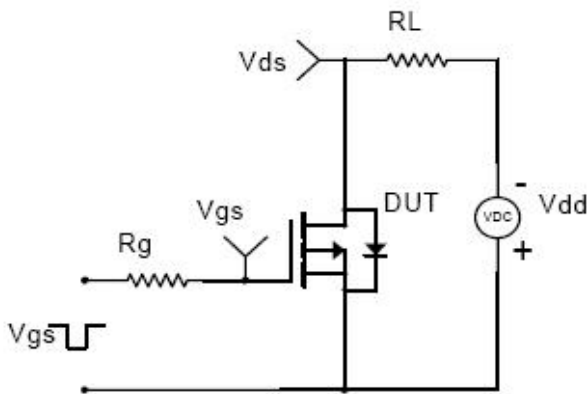
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



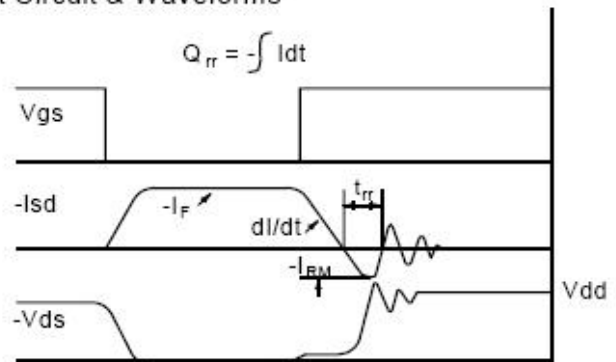
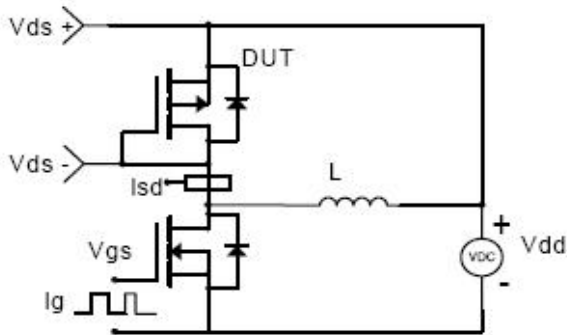
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



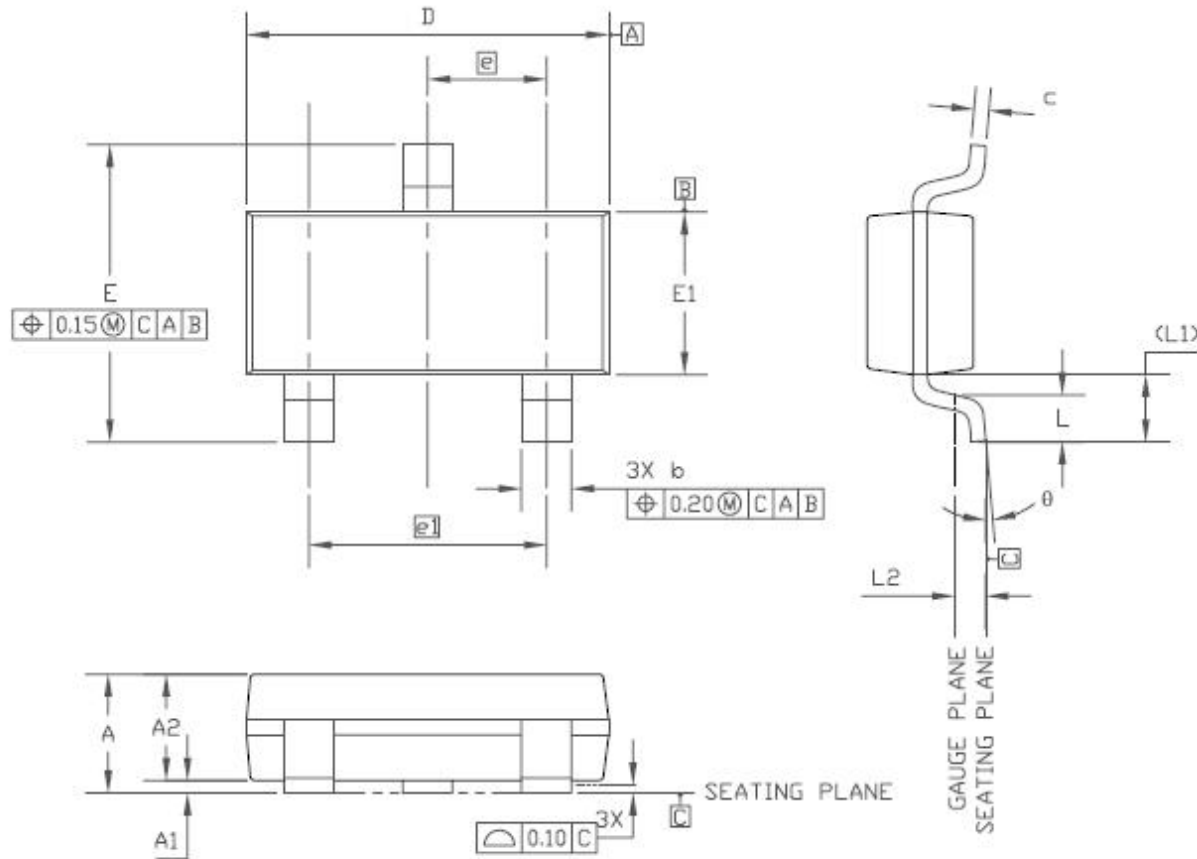
Diode Recovery Test Circuit & Waveforms



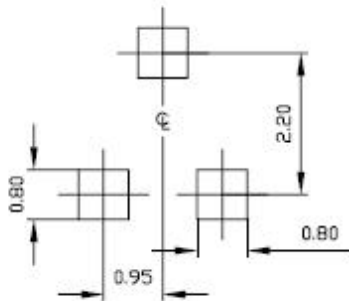


Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
θ	0°	—	8°	0°	—	8°