LP4077

Standalone 300mA Single-Cell Linear Charger

Features

- Easy-to-use standalone single-cell charger
  - 1% regulated voltage accuracy
  - Programmable up to 300mA constant current
  - Trickle charge 30% of constant current
  - Termination current 10% of constant current
- High integration
  - Integrated reverse blocking MOSFET
  - Built-in charge current sensing
  - Internal loop compensation
  - Integrated charge status indication
- Support full charge cycle of trickle current mode, constant current (CC) mode, constant voltage (CV) mode, charge termination and automatic recharge
- 10nA BAT leakage current
- Thermal regulation foldback
- Low active EN function
- RoHS compliant and 100% lead (Pb)-free
- Package: DFN-6(1mm x 1mm)

General Description

The LP4077 device is a highly advanced linear charger for single cell Li-Ion and Li-Polymer batteries. The device is ideally suited for portable applications due to a small DFN-6 package and low number of external components required.

The device employs a full charge algorithm with trickle current mode, constant current (CC) mode, constant voltage (CV) mode, charge termination and automatic recharge. The device supports charge current up to 300mA, programmed by an external resistor.

Without an input supply, the battery leakage current is only 10nA when ambient temperature is 25℃， so it can save energy and improve standby time.

The device provides input under voltage lockout (UVLO) and thermal regulation foldback protection that is implemented by reducing the charge current while the junction temperature reaches 125℃.

The LP4077 is available in a DFN-6 (1mmx1mm) package.

Applications

- Smart Watches
- Gaming Devices
- Portable Media Players
- Handheld Battery-Powered Devices
- Fitness Accessories
- Bluetooth Handsets

Order Information

LP4077 □□ □ □□□

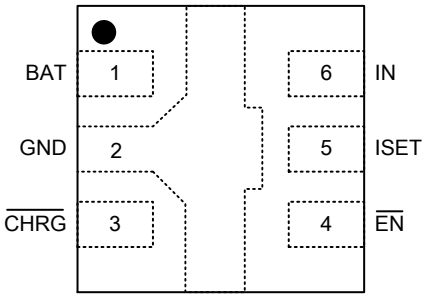
- Battery Voltage
  - Default:4.20V
  - 435:4.35V
  - 44:4.40V
- F: Pb-Free
- Package Type
  - QV: DFN-6

Device Information

Part Number	Top Marking	Battery Voltage	Moisture Sensitivity Level	Package	Shipping
LP4077QVF	BYW	4.20V	MSL3	DFN-6	12K/REEL
LP4077QVF-435	BQW	4.35V	MSL3	DFN-6	12K/REEL
LP4077QVF-44	BaW	4.40V	MSL3	DFN-6	12K/REEL
Marking indication: W: Production week.					

Pin Diagram

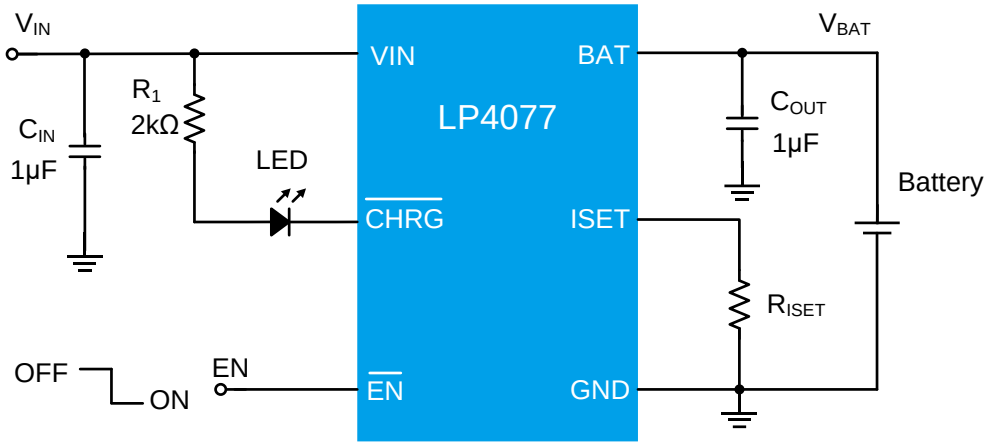
DFN-6 (Top View)



Pin Description

Pin DFN-6	Name	Description
1	BAT	Battery Pin. Connect to the battery, A 1μF capacitor is needed typically.
2	GND	GND. Connect to the system ground.
3	CHRG	Open-Drain Charge Status Output. When the device is in charging state, the CHRG pin is pulled low by an internal NMOS. When the charge cycle is completed, the internal NMOS turned-off, the pin could be pulled high by an external pull-up resistor.
4	EN	Charge Enable Input. Low active.
5	ISET	Constant Charge Current Program Pin. Connect this pin with an external resistor R_{ISET} to GND to program the constant charge current.
6	VIN	Positive Supply Voltage Input. Place a 1μF ceramic capacitor from IN to GND and place the capacitor as close as possible to IC.

Typical Application Circuit



Absolute Maximum Ratings (1)

- VIN, CHRG, BAT, ISET, EN Pin to GND ---------- -0.3V to 7V
- Maximum Power Dissipation ---------- 0.5W
- Maximum Junction Temperature (T_J) ---------- 150℃
- Storage Temperature ---------- -55℃ to 150℃
- Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

- HBM (Human Body Model) ---------- 2kV
- MM (Machine Model) ---------- 200V

Recommended Operating Conditions

- Input Voltage ---------- 4.5V to 6V
- Maximum Charge Current ---------- 300mA
- Operating Junction Temperature Range (T_J) ---------- -20℃ to 125℃
- Operating Ambient Temperature Range (T_A) ---------- -20℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = 5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range		4.5	5	6	V
$I_{IN\_Standby}$	Input Supply Current	V_{EN}=0V, Standby mode (Charge terminated)		1.7		μA
$I_{IN\_Disable}$		V_{EN}=5V		0.9		μA
V_{UVLO}	Under Voltage Lockout Threshold	V_{IN} Rising		3.0		V
V_{UVLO_HYS}	V_{UVLO} Hysteresis	V_{IN} Falling		200		mV
BAT LEAKAGE CURRENT						
$I_{BAT\_Leakage}$	Battery Leakage Current	LP4077QVF V_{IN} floating, V_{BAT}=4.2V		10		nA
$I_{BAT\_Standby}$	Battery Standby Current	Charge Terminated LP4077QVF V_{IN}=5V, V_{BAT}=4.2V		77		nA
BATTTERY CHARGER						
V_{FLOAT}	Regulated Output Voltage	LP4077QVF	4.158	4.2	4.242	V
		LP4077QVF-435	4.307	4.35	4.394	V
		LP4077QVF-44	4.356	4.4	4.444	V
I_{BAT}	Constant Charge Current	R_{ISET}=1kΩ, Constant Current Mode	98.8	104	109.2	mA
		R_{ISET}=2kΩ, Constant Current Mode	49.4	52	54.6	mA
		R_{ISET}=10kΩ, Constant Current Mode	9.45	10.5	11.55	mA
I_{TERM}	Termination Current threshold	Constant Voltage Mode		10%		I_{BAT}
I_{TRIKL}	Trickle Charge Current	V_{BAT}<V_{TRIKL}		30%		I_{BAT}
V_{TRIKL}	Trickle Charge Threshold Voltage	LP4077QVF V_{BAT} Rising		2.9		V
		LP4077QVF-435 V_{BAT} Rising		2.9		V
		LP4077QVF-44 V_{BAT} Rising		2.9		V
V_{TRHYS}	Trickle Charge Hysteresis Voltage	LP4077QVF V_{BAT} Falling		190		mV
		LP4077QVF-435 V_{BAT} Falling		190		mV
		LP4077QVF-44 V_{BAT} Falling		190		mV

ΔV_{RECHRG}	Battery Recharge Voltage Difference Threshold (V_{FLOAT} -V_{RECHRG})	LP4077QVF V_{BAT} Falling		150		mV
		LP4077QVF-435 V_{BAT} Falling		150		mV
		LP4077QVF-44 V_{BAT} Falling		150		mV
$V_{Headroom}$	V_{IN}-V_{BAT} Threshold Voltage	V_{BAT}=3.5V, V_{IN} Rising		150		mV
V_{HRHYS}	V_{IN}-V_{BAT} threshold Hysteresis	V_{BAT}=3.5V, V_{IN} Falling		90		mV
T_{J_LIMIT}	Junction Temperature Limit	Thermal Foldback Protection State		125		℃
R_{DS}	VIN-BAT MOSFET on-resistance			2.2		Ω
ISET/CHRG PINs						
V_{ISET_CC}	ISET Pin Voltage	Constant Current Mode		1		V
V_{ISET_TR}		Trickle Current Mode		0.3		V
V_{STAT}	STAT Pin Output Low Voltage	I_{STAT}=5mA			0.5	V
I_{STAT}	CHRG Pin Sink Current				5	mA
EN PIN						
V_{EN_ON}	EN Logic-Low Voltage Threshold	EN Falling	0		0.4	V
V_{EN_OFF}	EN Logic-High Voltage Threshold	EN Rising	1.2			V
I_{EN}	EN pin leakage current	V_{EN}=5V or V_{EN}=0V	-1		1	μA

Typical Characteristics

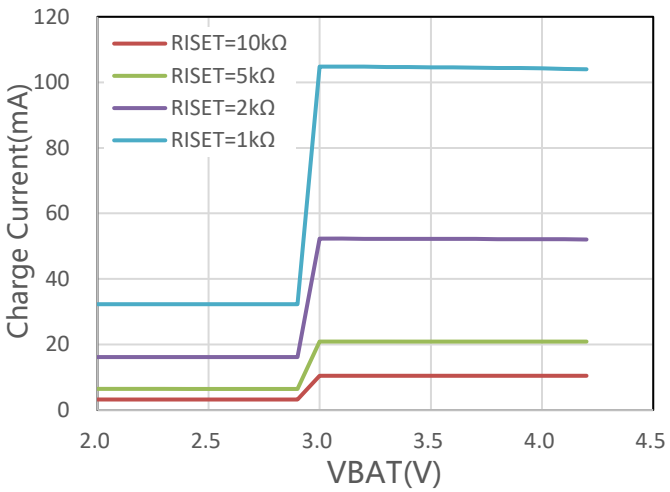


Figure 1. Charge current vs BAT voltage, 25℃

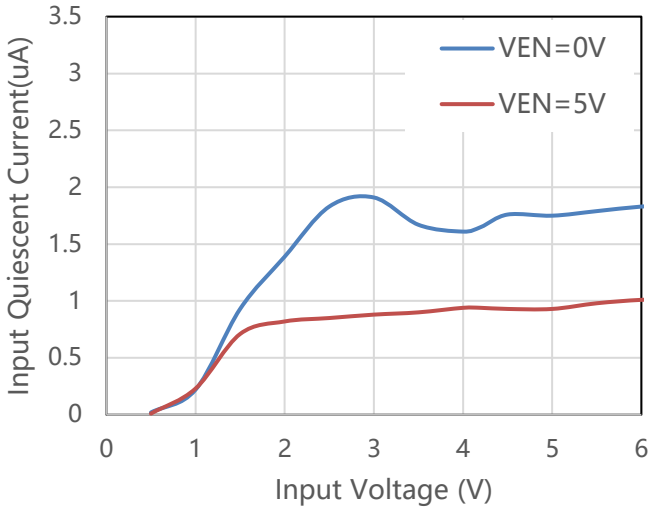
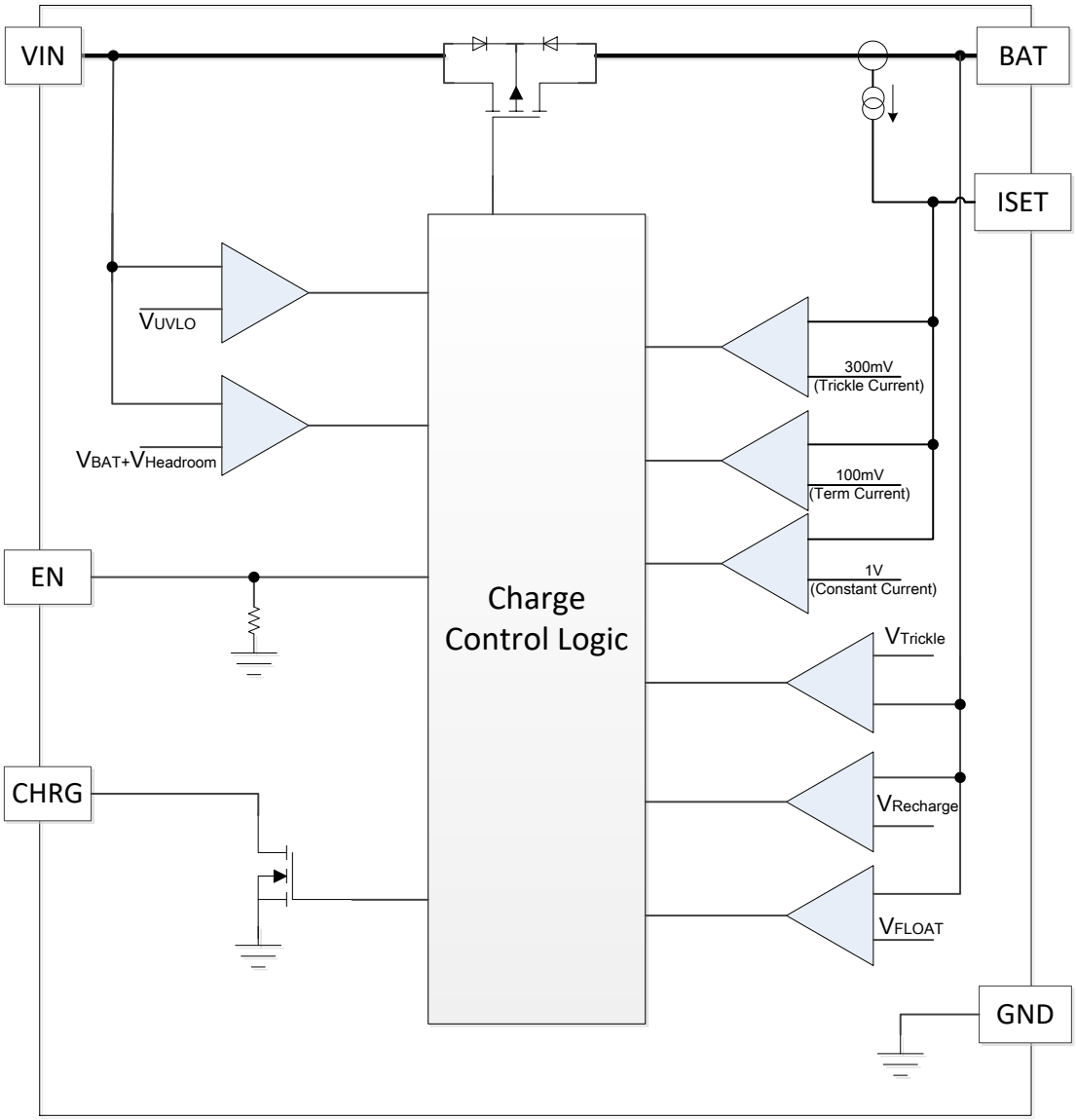


Figure 2. Input quiescent current vs input voltage, 25℃

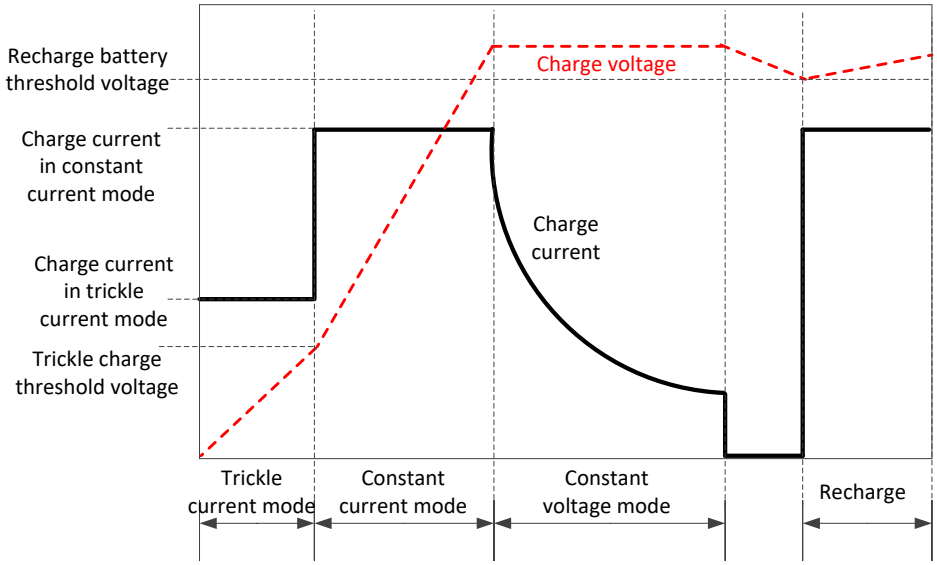
Functional Block Diagram



Detailed Description

Overview

The LP4077 device is a highly advanced linear charger with up to 300mA maximum charge current for single cell Li-Ion and Li-Polymer batteries. The device charges the battery with full charge cycle: trickle current mode, constant current (CC) mode, constant voltage (CV) mode, charge termination and recharge. The typical charge profile showed as below figure.



When the battery voltage is lower than Trickle Charge Threshold Voltage (V_{TRIKL}, 2.9V typical), the device charges in the trickle current mode, the charge current will be set to Trickle Charge Current (I_{TRIKL}), which is approximately 30% of the ISET programmed Constant Charge Current (I_{CC}) to bring the battery voltage up to a safe level for full current charging. When the battery voltage rises to V_{TRIKL}, the device enters the constant current mode, where the charge current is 100%I_{CC}. When the battery voltage approaches the Regulated Output Voltage (V_{FLOAT}), the device goes to constant voltage mode, the charge current starts to decrease. When the charge current is lower than the Termination Current threshold (I_{TERM}), which is 10%I_{CC}, the device will terminate the charging.

The device will automatically recharge the battery while the battery voltage drops ΔV_{RECHRG} (150mV typical) from the Regulated Output Voltage (V_{FLOAT}).

Constant Charge Current Programming

The Constant Charge Current (I_{CC}) is set by an external resistor (R_{ISET}) connecting from the ISET pin to GND. The relationship of the constant current and the programming resistance is established by the following formula:

$$I_{CC} = \frac{V_{ISET\_CC} \times 104}{R_{ISET}}$$

where V_{ISET_CC}=1V typical.

Charge Termination and Automatic Recharge

A charge cycle will be terminated when the charge current falls to I_{TERM} (10%I_{CC}, typical), as the battery voltage reached V_{FLOAT}. The function is implemented by monitoring the ISET pin voltage and comparing to a 100mV threshold voltage. When the ISET pin voltage falls below 100mV for longer than 1ms typically, the

charging will be terminated.

Once the charge cycle is terminated, the LP4077 continuously monitors the voltage on the BAT pin by a comparator. A new charge cycle restarts when the battery voltage drops by a voltage difference ΔV_{RECHRG} (150mV, typical) from V_{FLOAT}, which means the battery level drops to approximately 80% to 90% capacity. This ensures that the battery always keeps at or near a fully charged condition.

Undervoltage Lockout (UVLO) and $V_{Headroom}$

An internal UVLO circuit monitors the input voltage and keeps the device in shutdown mode until the input supply rises above the Under Voltage Lockout Threshold (V_{UVLO}). The UVLO circuitry has a built-in hysteresis of 200 mV. The UVLO circuit always be active.

Again, the input supply must be $V_{Headroom}$ (150mV, typical) higher than the battery voltage before the LP4077 become operational. Whenever the input supply is below the V_{UVLO} or lower than a voltage that is 150mV above the VBAT pin, the LP4077 is in shutdown mode.

Enable Function

The LP4077 features an enable/disable function. An input "Low" signal or floating connection on EN pin will enable the device. To ensure the device be active, the EN low voltage level must be lower than 0.4V. The device will enter the shutdown mode when the voltage on the EN pin is higher than 1V. If the enable function is not needed in a specific application, the EN pin could be shorted to GND or floating to keep the device continuously active.

Charge Status Indicator (CHRG)

When the input voltage is above the UVLO and above the voltage of $V_{BAT}+V_{Headroom}$, CHRG has two different states: strong pull-down (~5mA) and high impedance. The strong pull-down state implemented by an internal NMOS indicates that the LP4077 is in a charge cycle. After the charge current decreased to I_{TERM} in CV mode and then charging terminated, the CHRG pin will become high impedance.

Function	CHRG
Charging	Low
Charge Terminated	Hi-Z

Junction Temperature-Limit Protection

An internal thermal regulation foldback loop reduces charge current if the junction temperature reaches a preset value of approximately 125℃ to prevent further temperature rise. This function protects the device from excessive temperature and allows the user to get the limits of the power handling capability of a given circuit board without risk of damaging the device. The charge current can be set according to typical ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.

Charge termination function won't be active on the thermal foldback regulation protection status.

Application Information

Thermal Consideration

Due to the low efficiency of linear charging, the most important factors are thermal design and cost, which are a direct function of the input voltage, charge current and thermal impedance between the battery charger and the ambient cooling air.

The power dissipation can be calculated approximately:

$$P_D = (V_{IN} - V_{BAT}) \times I_{BAT}$$

Where PD is the power dissipation, V_{IN} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current.

The worst-case situation is when the device has transitioned from the trickle current mode to the constant current mode. In this situation, the battery charger has to dissipate the maximum power.

In this case, with a 5V input voltage source, 300mA constant current, the max power dissipation could be,

$$P_{Dmax} = (5V - 2.9V) \times 0.3A = 0.63W$$

This power dissipation with the battery charger in the DFN-6 package may cause thermal regulation foldback to reduce the charge current at high ambient temperature. Then a trade-off must be made between the charge current, cost and thermal requirements of the charger.

External Capacitors

In order to maintain good stability in the whole charge cycle, a capacitance of 1μF is recommended to bypass the BAT pin to GND. In addition, the battery and interconnections appear inductive at high frequencies. These elements are in the control feedback loop during constant voltage mode. Therefore, the bypass capacitance may be necessary to compensate for the inductive nature of the battery pack.

ISET Resistor

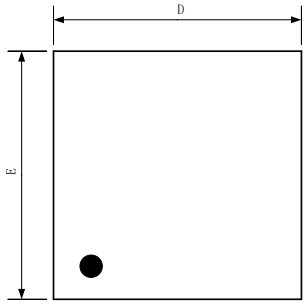
In order to assure the accuracy of the constant current, better than 1% precision resistance is recommended.

Layout Consideration

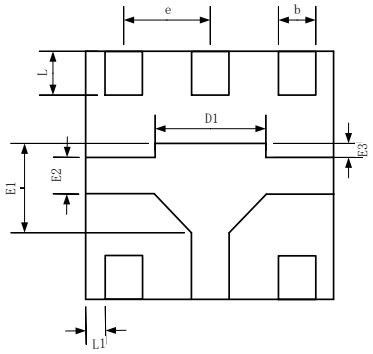
For optimum voltage regulation, place the battery pack as close as possible to the device's BAT and GND pins. This is recommended to minimize voltage drops along the high current-carrying PCB traces. If the PCB layout is used as a heat sink, adding many vias in the heat sink pad can help conduct more heat to the PCB backplane, thus reducing the maximum junction temperature. It is also recommended to place the capacitor C_{IN} and C_{OUT} as close as possible to the corresponding pins and the GND pin.

Packaging Information

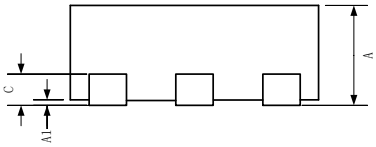
DFN-6



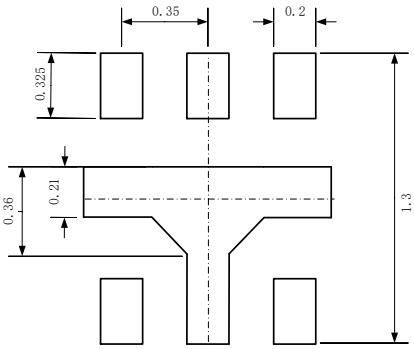
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.36	0.38	0.40
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
c		0.127REF	
D	0.95	1.00	1.05
D1	0.40	0.45	0.50
E	0.95	1.00	1.05
E1	0.31	0.36	0.41
E2	0.10	0.15	0.20
E3	0.005	0.055	0.105
e		0.35BSC	
L	0.125	0.175	0.225
L1		0.075REF	