Features

- Input over-voltage protected up to 16V
- Charge Management
  - Programmable charge current up to 1A
  - Programmable floating voltage with 0.3% accuracy
  - Programmable trickle charge and termination current
- Charge and discharge current monitor
- Automatic re-charge and thermal foldback
- I2C bus to SoC with an interrupt pin
- Low drop-out fast charge function and low heat
- Power path management
- Charge safety timer and watchdog
- High accuracy current mirror for gauge application
- Rich protections: UVLO, OVP, SCP
- 0.6-μA ultra-low iq in standby mode
- 0.4-μA ultra-low iq in ship mode
- 2mm X 2mm QFN-12 package
- RoHS Compliant and 100% Lead (Pb) Free
-

Applications

- Wearable
- Fitness Application
- Smart Watch

General Description

The LP4081 is an ultra-low power linear charger targeting at wearable applications protected up to 16V input voltage. It contains a linear charger to charge the Li-ion battery. The charger has an ideal-diode mode for high efficiency and low heat operation. The LP4081 integrates the power path management function to support SoC powerup even with a deeply-discharged battery. The LP4081 features 150mΩ low $R_{ds,on}$ of the BAT_FET from the battery to the system to achieve high discharge efficiency and low heat under full load range. An I2C interface is offered for programmability and flexibility of the device.

The LP4081 provides rich protections, including the input Under-volage lockout protection (UVLO), input over-voltage protection (OVP) and system short circuit protection (SCP).

The typical quiescent current of LP4081 is 0.6-μA and the battery current is reduced to 0.4-uA in ship mode.

The whole system is in a 12-pin 2 X 2 QFN package.

Order Information

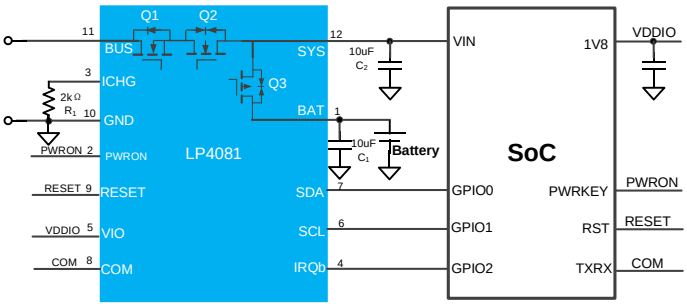
LP4081 □□ □

F: Green/Pb-Free

Package Type

QV : QFN

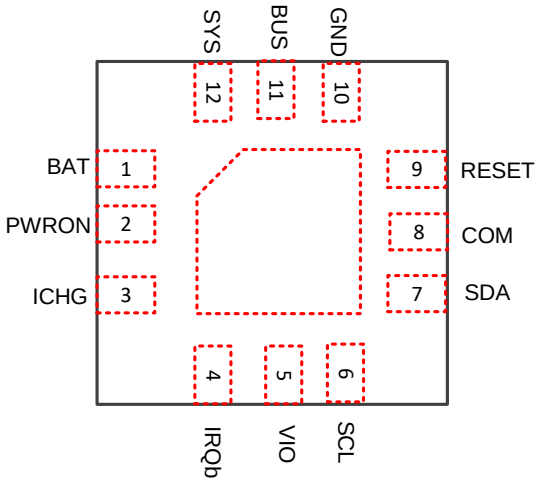
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping
LP4081QVF	LPS LP4081 YWX	12-pin 2 X 2 QFN	4K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.			

Pin Diagram



LP4081 Pinout

Pin Description

Pin #	Name	Description
1	BAT	Battery pin of the linear charger.
2	PWRON	Power-on signal output. This pin is open drain output.
3	ICHG	charge and discharge current monitor pin. Refer to Charger section for details.
4	IRQb	interrupt output. No pull-up
5	VIO	bias voltage for bi-directional communication
6	SCL	Clock line of the I2C bus. This pin open-drain output. 100k pull up to VIO
7	SDA	Data line of the I2C bus. This pin open-drain output. 100k pull up to VIO
8	COM	Communication pin, connect to the UART of the Bluetooth SoC
9	RESET	Reset signal output. This pin is open drain output.
10	GND	Ground
11	BUS	Input power supply. No capacitor is needed on this pin
12	SYS	System power pin. either power from BUS or BAT.
Thermal PAD		Connect to ground panel for thermal dissipation.

Absolute Maximum Ratings (Note)

BUS to GND ---------- -0.3V to 16V

All other pins to GND ---------- -0.3V to 6.5V

Maximum Junction Temperature (TJ) ---------- 150°C

Operating Ambient Temperature Range (TA) ----------40℃ to 85℃

Maximum Soldering Temperature (at leads, 10 sec) ----------260℃

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV

CDM (Charged Device Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ----------65℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{bus}	Input voltage	3		5.6	V
I_{bus}	Input current			1.5	A
T_A	Ambient temperature range	-40		85	°C
C_{bus}	Input decoupling capacitor, 115200bps UART			1	nF
C_{sys}	System capacitor	1			μF
C_{bat}	Battery capacitor	1			μF

Electrical Characteristics

(The specifications are measured under conditions V_{bus} = 5V, T_J = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_bus}	BUS UVLO	BUS falling, no deglitch		3.0		V
V_{ULVO_H}	BUS UVLO hysteresis	BUS rising		100		mV
V_{OVP_bus}	BUS OVP BUS	BUS rising, no deglitch	5.6	5.7	5.8	V
V_{OVP_H}	BUS OVP BUS hysteresis	BUS falling		100		mV
I_{q_bus}	BUS Input quiescent current	BUS=5.0V，BAT=4.3V，EN_CHG=1,		100	130	uA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ds,on_bus}	Q1+Q2, NMOS on- resistance			0.3	0.4	Ω
I_{IN_LIM}	Input current limit	IIN_LIM=0	0.5	0.65		A
	Hiccup wait time			60		ms
BATTERY SECTION						
V_{BAT_POR}	BAT Power-on-reset	battery voltage rising	1.6		2.4	V
$V_{BAT\_POR\_hys}$	BAT POR hysteresis			100		mV
I_{BAT_Dis}	Quiescent current from BAT	Discharge mode，BUS=0V, BAT=3.8V, SYS=Float DIS[1:0]=10, EN_WTD=1		30		uA
I_{BAT_CHG}		Charge mode，BUS=5V, BAT=4.5V, EN_Term=1		2	3	uA
I_{BAT_STD}		Standby mode，BUS=0V, BAT=3.8V, DIS[1:0]=00, EN_WTD=0，		0.6	1	uA
I_{BAT_SHIP}		Ship mode，BUS=0V, BAT=3.8V		0.4		uA
Charge Management						
V_{TRK}	Trickle charge voltage threshold	BAT rising edge, Vtri=3.0V	2.95	3.0	3.05	V
V_{TRK_hys}	Trickle charge voltage hysteresis			100		mV
I_{TRK}	Trickle charge current	Iterm[2:0]=001, 3mA	2.7	3	3.3	mA
I_{CC}	CC current	25°C	28.5	30	31.5	mA
V_{CV}	CV voltage	25°C	-0.35		0.35	%
		From -10°C to 85°C	-0.5		0.5	%
V_{RECHG}	Re-charge threshold	BAT falling edge, Reference to CV voltage		-150		mV
t_{drechg}	Recharge deglitch time [1]			200		ms
I_{term}	Charge termination current	Iterm[2:0]=001, 3mA	2.7	3	3.3	mA
t_{dterm}	termination deglitch time[1]			30		ms

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SYS_DPM}	SYS Dynamic Power Management	DPM[2:0]= 011, 3.6V	3.55	3.6	3.65	V
T_{therm}	Thermal foldback threshold		100	120	140	°C
t_{Tri_safe}	Trickle charge safety timer			0.75		hr
t_{Fast_safe}	Fast charge safety timer	From exit Trickle to charge terminate		3.75		hr
Power Path Management						
R_{ds,on_bat}	BAT_FET on resistance	BAT=3.8V		0.15	0.2	Ω
I_{DIS_LIM}	Discharge SCP limit	IDIS_LIM[1:0]=00,		0.44		A
t_{denter_ship}	Enter shipping mode delay time[1]			1		s
t_{dexit_ship}	Exiting shipping mode by pulling IRQb pin delay time[1]			2		s
V_{UV_BAT}	Battery UVLO	BAT falling edge		3.0		V
		hysteresis		0.2		V
t_{d_BATUV}	BAT_UV deglitch			40		ms
I2C and IRQb						
V_H	Logic High		1.2			V
V_L	Logic Low				0.4	V
I_{sink}	SDA, SCL, IRQb sink current capability	BAT=3.8V， VIRQb=0.4V	0.5			mA
t_{irqb}	IRQb low pulse width			256		us
RESET						
t_{dreset}	Reset deglitch timer[1]		5	7.5	10	s
t_{pulse_reset}	RESET pulse width[1]		100	150	200	ms

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{Hreset}	RESET output high level	Loaded with 10kΩ resistor, ref to BAT			-100	mV
PWRON						
t_{dpwron}	PWRON deglitch timer[1]		0.5	0.75	1	s
t_{pulse_pwron}	PWRON pulse width[1]		1.5	2.25	3	s
V_{Hpwron}	PWRON output high level	Loaded with 10kΩ resistor, ref to BAT			-100	mV
One-wire timing						
	One-wire logic input high[1]	BAT=3.8V			1.2	V
	One-wire logic input low[1]	BAT=3.8V	0.4			V
t_{PRE_START}	Pre_start time[1]	Pre-start operating time before receiving the one-wire code	1	2	3	ms
t_{START}	Start bit time[1]	Start time after a falling edge sensed at VIN pin.	8	10	12	ms
t_{bit}	Code bit time[1]	1 bit code (‘0’ or ‘1’) cycle time	0.8	1	1.2	ms
t_{1h}	Code ‘1’ high time[1]	Code 1 high level time	704	880	1056	us
t_{1l}	Code ‘1’ low time[1]	Code 1 low level time	96	120	144	us
t_{0h}	Code ‘0’ high time[1]	Code 0 high level time	96	120	144	us
t_{0l}	Code ‘0’ low time[1]	Code 0 low level time	704	880	1056	us
t_{stop}	Stop time[1]	Stop time after a rising edge sensed at VIN pin.	0.8	1	1.2	ms

[1]: Not production tested. Guaranteed by design

Typical Characteristics

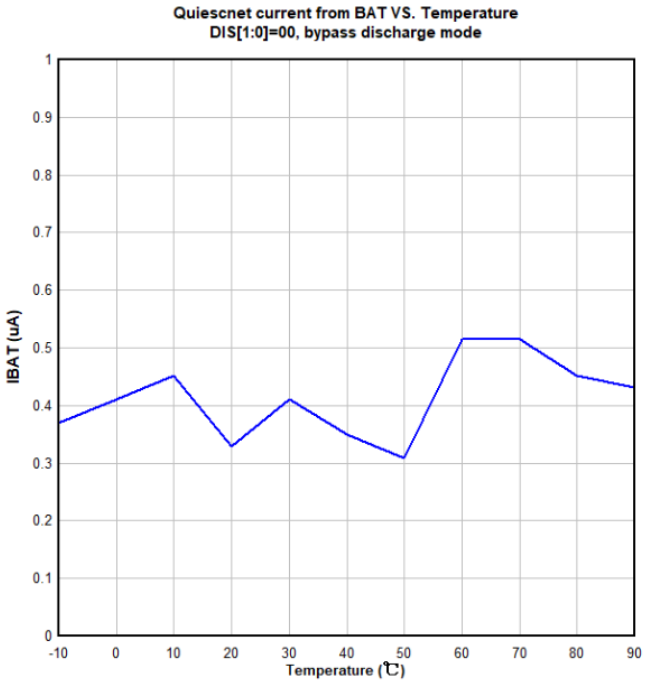


Figure 1. Battery Quiescent Current VS. Junction Temperature, BAT=3.6V, bypass mode

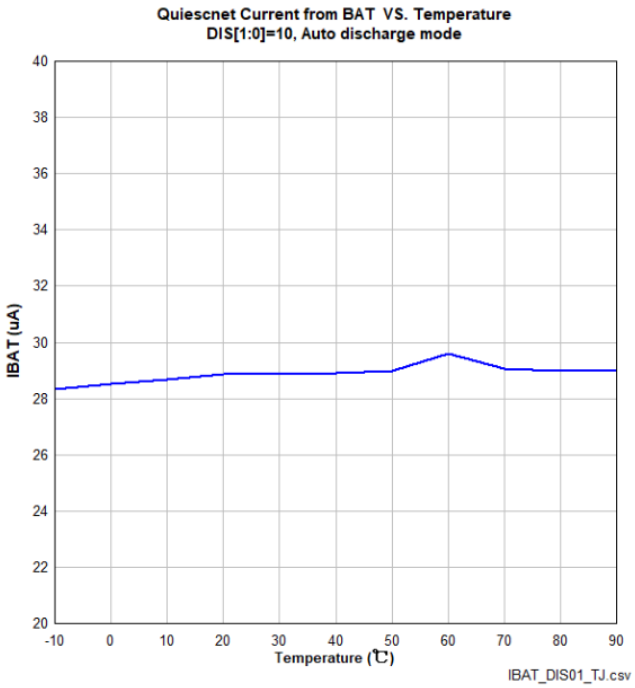


Figure 2. Battery Quiescent Current VS. Junction Temperature, BAT=3.6V, Auto mode

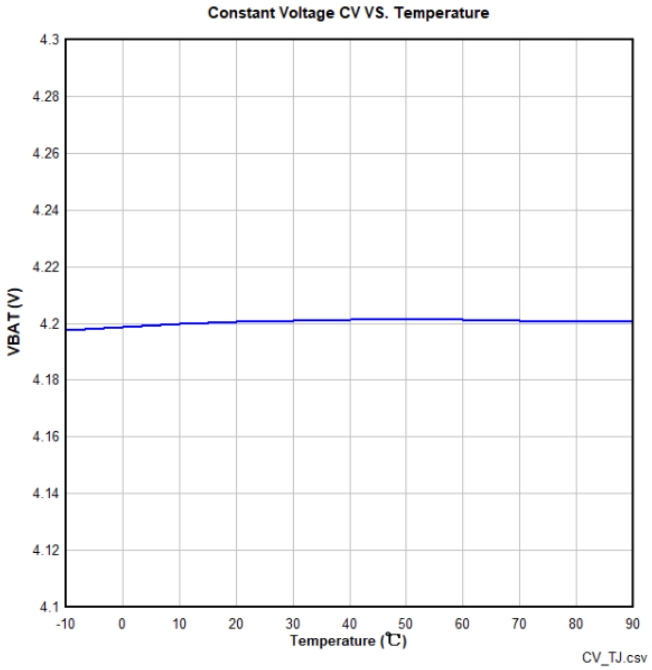


Figure 3. Battery Floating Voltage VS. Junction Temperature

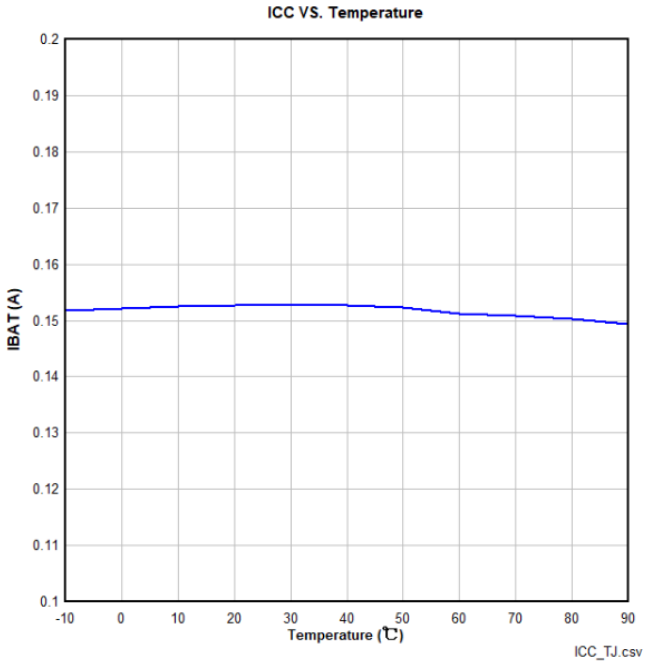


Figure 4. Battery Constant Current VS. Junction Temperature

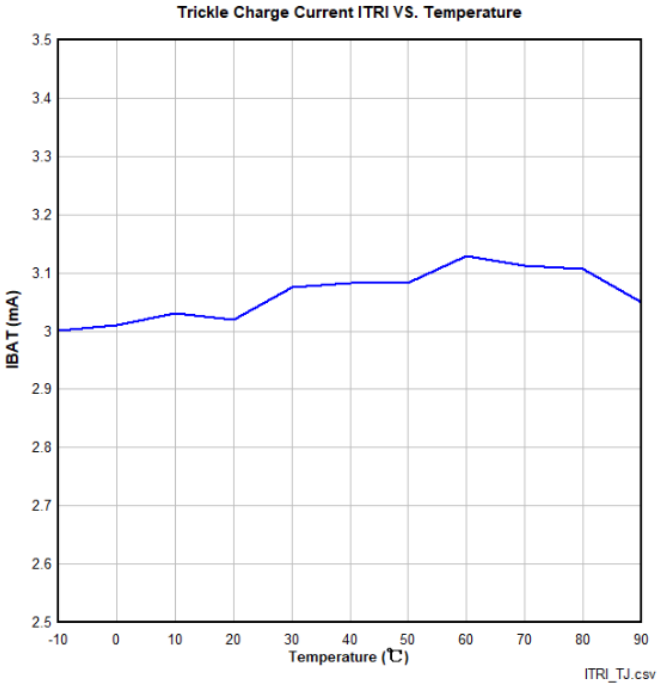


Figure 5. Trickle Charge Current VS. Junction Temperature

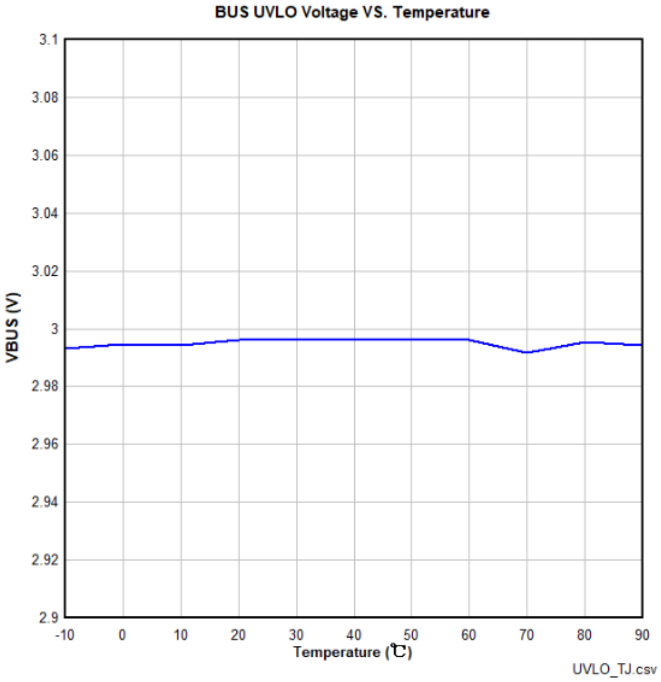


Figure 6. BUS UVLO Threshold VS. Junction Temperature

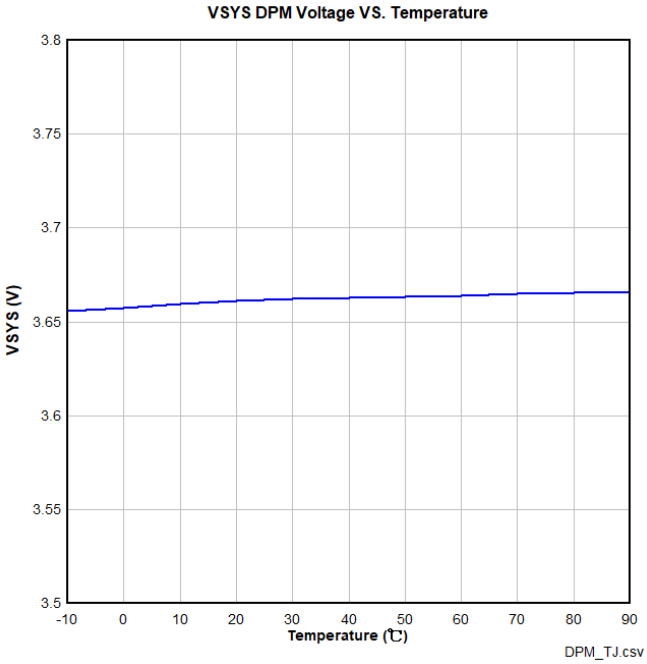
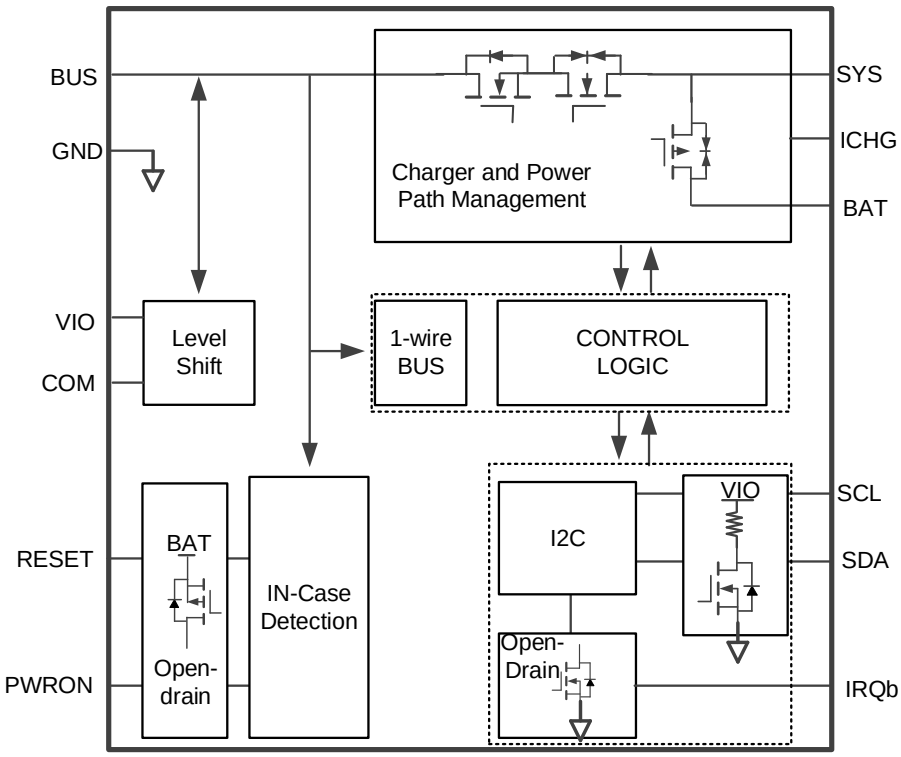


Figure 7. SYS pin DPM Voltage VS. Junction Temperature

Functional Block Diagram



Detailed Description

Overview

The LP4081 is a fully integrated linear charger solution with power management function targeting at wearable applications. It contains a standard linear charger to charge the Li-ion battery with an I2C interface and an IRQb interrupt indication. The charger has an ideal-diode mode to achieve high efficiency and low heat performance when fast charge is needed. The power path management function allows the system to be powered from the input voltage even with a dead battery.

When the linear charger is not in operation, the BAT leaks 0.6-μA current.

Input Section

When one of the events below occurs, the LP4081 will perform a power-on reset. All registers will be set to the default values.

- Battery insertion without input voltage
- The input voltage is present without battery

The SoC or MCU can access all the registers after POR.

Under-voltage lockout (UVLO) and over-voltage protection (OVP)

The input block monitors the BUS pin voltage to determine when to turn on the input FETs.

The LP4081 detects an over voltage (OV) event when the Input voltage is higher than OVP threshold V_{OVP_bus}. The LP4081 turns off the input FETs immediately.

The LP4081 detects an under voltage (UV) event when the Input voltage is lower than BUS_UVLO threshold V_{ULVO_bus}. The LP4081 turns off the input FETs as well after a typical 100-us deglitch time.

BUS Powerup

When the input voltage is higher than the UVLO threshold but lower than the OVP threshold, the PGD bit is set and the SYS voltage ramps up after a 1-ms deglitch time. Otherwise, the input FETs remains open until the Input voltage falls to the PGD range.

The input voltage is connected to the SYS after PGD is set. But the charger function is still OFF unless the EN_CHG bit is set by I2C interface.

Reverse-current Protection (RCP) and Forward Regulation

The input FETs integrates a 50mV forward regulation amplifier, when the Input voltage drops to only 50mV higher than the SYS voltage, the input FETs increase the R_{ds,on_bus} to limit the current to SYS. When the Input voltage drops to only 25mV above the SYS voltage, the input FETs turn off to prevent the reverse current from the SYS capacitor.

Current Limit and Short Circuit Protection (SCP)

The input FETs integrate a typical 0.65A current limit function. The LP4081 monitors the input current when the BUS is present. When the SYS drops below 2.5V, the LP4081 enters hiccup mode.

Charge Management

The charger is a typical linear charger with three charging modes, i.e., trickle, constant current (CC), and constant voltage (CV) modes. The EN_CHG bit can enable the charger. The default value at power-on reset is low, which disables the charger.

1. The linear charger starts charging when all the conditions below are valid:

- BUS power up (PGD=1)
- EN_CHG is set by I2C

all the charge related timers are reset when a new charge cycle starts.

2. **Trickle charge:** The trickle-charge voltage threshold is programmable via Vtri bit with 3.0V default value. The

LP4081 starts trickle charging when the battery voltage is below the trickle threshold. The trickle-charge current is programmable in the ITERM[2:0] register. If the Vtri is not reached before the trickle charger safety timer(0.75Hr), the charging cycle is terminated forcedly and the TRI_TE status register is set. A low-level pulse is sent out at IRQb pin at the same time.

3. **CC charge:** The LP4081 starts CC charging when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The charging current is determined by ICC[5:0] registers and the ICC_EXT bit register via I2C bus. The CC current is programmable from 10~470mA when ICC_EXT is set to 0 and the range is extended to 25~1175mA when the ICC_EXT bit is set to 1. The default charging current is 30mA and ICC_EXT bit is 0.

   The fast charge safety timer is 3.75Hrs. The TERM_TE bit is set when the CC charging time expires. The charge progress is terminated and the IRQb pin outputs a low-level pulse as well when EN_Term is set to 1.

4. **CV charge:** The LP4081 starts CV charging when the battery voltage rises above the CV threshold. The charging decreases gradually until the charging termination is triggered in this phase. The CV voltage is programmable via the BAT_CV[4:0] register. The default value is 4.2V.

5. **Ideal diode mode and forward regulation**: When the power supply to the BUS pin has a current capability lower than the programmed CC charge current, the linear charger will enter an ideal diode mode. The LP4081 integrates a typical 25mV forward regulation amplifier. The BAT_FET will be fully turned on when the voltage drop from SYS to BAT is higher than 25mV. The BAT_FET Rds,on is regulated when the charging current is not high enough to achieve the 25mV voltage drop.

6. **Power path management**: The minimum system voltage is set by DPM[2:0] register. When the SYS voltage is below DPM[2:0], the charging current reduces until a new balance is reached. Even with a dead battery, the system voltage is regulated above the minimum system voltage.

7. **Termination:** The termination current is programmable in the ITERM[2:0] register as well. When the BAT voltage is higher than the recharge voltage and charge current drops to the termination current, the low-level pulse is sent out from IRQb pin. The charge cycle is terminated immediately when EN_term bit is set to 1, otherwise, the charging continues until fast charge safety timer time expire.

8. **Recharge:** A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage while the BUS is still available. The charging cycle starts again and the safety timer re-counting.

9. **Charge current foldback** ： When the die temperature reaches 120 °C, the charger current decreases until a new temperature balance is reached.

10. **EN_CHG**: When EN_CHG is set to 0, the charging process is terminated immediately and safety timer counting is reset. When EN_CHG is set to 1 from 0. The charging cycle starts again and the safety timer re-counting.

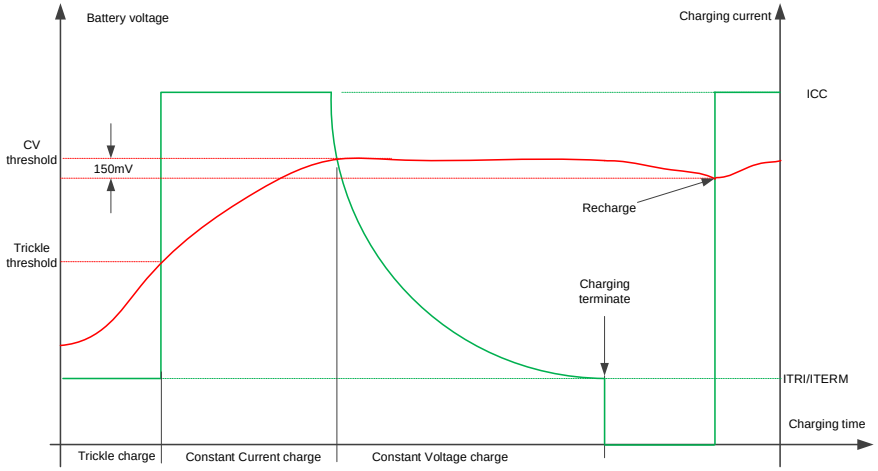


Figure 8. Charging profile

Discharge Management

The LP4081 integrates the power path management function. The SYS is always powered either from the input voltage

or the battery. The system voltage drops to the battery voltage when the input power source is removed.

The LP4081 supports two discharge modes when the input voltage is not present by configuring the BAT_FET into different operation region. The BAT_FET can be set to bypass, power down reset and auto mode by configure the DIS[1:0] register. When DIS[1:0] is set to 00, the BAT_FET is turned on forcedly and works in bypass mode but without current limit function and thermal shutdown protection. When DIS[1:0] is set to 01, the BAT_FET is turned OFF for 8s and the SoC can reset itself. When DIS[1:0] is set to 10, the BAT_FET is in auto mode with current limit function and thermal protection. The default current limited is 0.44 A in auto mode. Just the same as the SCP in charge mode, the LP4081 functions a hiccup operation when SYS is short to ground.

The BAT_FET can be set to bypass, power down reset and auto mode by one-wire bus as well.

When the battery voltage is lower than 3.0V, the discharge function is disabled immediately and the BAT_UV is set. IRQb low pulse is sent.

System reset

The LP4081 integrates 3 different methods to reset the SoC system.

1. RESET pin. RESET pin will output a high pulse when earphone is inserted the charging case. This method will not cut off the SYS power supply. (Details in RESET section). Registers will not be reset in this mode.
2. Watchdog. The LP4081 integrates a typical 40-s watchdog. The LP4081 turns off the input FETs and the BAT_FET for 8s. (Details in WATCHDOG section). All the registers reset to default values after 8s time over.
3. DIS[1:0] register. The LP4081 turns off the input FETs and the BAT_FET for 8s as well when DIS[1:0] is set to 01 by I2C or one-wire. All the registers reset to default values after 8s time over.

RESET and PWRON outputs

The LP4081 integrates the earphone insertion and removal detection circuits. The RESET or PWRON signal are sent when the earphone is inserted or removed.

The RESET and PWRON are open drain outputs. A resistor pulled to ground should be connected to each pin.

RESET:

When the input voltage is higher than the in-case detection threshold, an internal reset timer starts. The input voltage falling below the in-case detection threshold will clear the timer. If the timer lasts for 7.5s, the RESET output is set to high (BAT) for 150ms and then falls to low.

The RESET signal can be stopped via the one-wire operation. If a one-wire signal sets a RESET STOP bit before the reset timer expires, no reset signal will be sent. The RESET STOP bit is cleared at the BUS power on reset.

PWRON:

When the Input voltage falls below in-case detection threshold for 0.75s (indicating the earphone has left the case), the PWRON pin will output a 2.25s high pulse (BAT) to turn on the earphone SoC automatically.

For applications that has a Hall sensor to indicate the opening of the case, the charging case can send a one-wire signal to start the PWRON signal immediately and stop sending a repeating PWRON signal when the earphone leaves the case. A PWRON STOP bit will be set during the operating, which stops the 2.25s high pulse. The PWRON STOP bit will be cleared during the power-on reset.

PWRON is open drain output as well.

Standby state

The LP4081 enters two different standby states as described below (EN_WTD=0, no input voltage):

1. The earphone leaves the charging case and the PWRON signal transmission is completed.
2. The earphone is in the charging case and the Input voltage stays higher than the in-case detection threshold but lower than the UVLO threshold.

The LP4081 only consumes 0.6-uA quiescent current in standby state from the battery. Only one wire is active in standby mode.

The LP4081 exits standby state immediately with each of the following conditions is met:

1. The battery POR event occurs.
2. The input voltage is present (BUS voltage higher than BUS_UVLO)
3. One-wire communication is active.
4. The earphone insertion event is triggered.

Shipping mode

The LP4081 supporting shipping mode by setting the SHIP bit (DIS[1:0] =11) by I2C or one-wire communication interface. The DIS[1:0] bits should be set to 10 before entering shipping mode. The LP4081 turns off all the active circuits after receiving the SHIP mode command with a typical 1s deglitch time. The LP4081 only consumes 400nA in shipping mode and a valid BUS voltage higher than the BUS_UVLO threshold can force the LP4081 exiting the shipping mode.

The LP4081 does not respond to the one-wire instructions in shipping mode and all the registers are set to the default values.

One-wire bus

The LP4081 has a one-wire bus to accept private instructions from the charging case. Each one-wire communication session starts with a PRE_START pulse followed by a START bit, a 4-bit frame, and then a STOP bit. When LP4081 receives an instruction successfully, an ACK signal will be sent back to the MCU in the charging case (marked blue). The ACK consists of a start bit and a 7-bit header code. The LP4081 integrates 12 instructions.

The one-wire bus is not valid when the battery voltage drops below 2.7V.

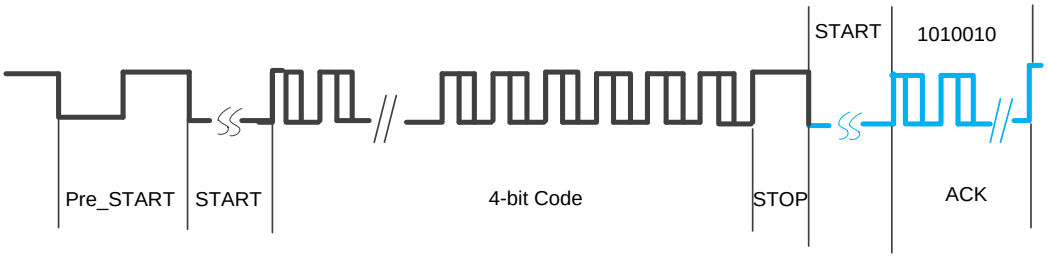


Figure 9. one-wire communication protocol

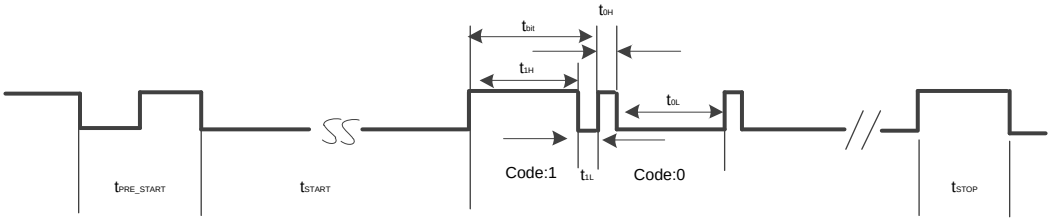


Figure 10. one-wire timing sequence

Table 1 . one-wire instructions list

Code	Description	Function
0X A417	Clear RESET-STOP	RESET-STOP bit is cleared, no other bits are affected
0X A43E	Set RESET-STOP	RESET-STOP bit is set, no other bits are affected
0X A445	Clear RESET bit	RESET outputs low
0X A46C	Set RESET high	RESET outputs high. The RESET pin will be pulled to BAT pin internally.
0X A49A	Clear PWRON-STOP	PWRON-STOP bit is cleared. PWRON signal will be sent when the headphone leaves the charging case.
0X A4B3	Set PWRON-STOP	PWRON signal will not be sent when the headphone leaves the charging case.
0X A4C8	Clear PWRON bit	PWRON outputs low

0X A4E1	Set PWRON high	PWRON outputs high. The PWRON pin will be pulled to BAT pin internally.
0X A50D	BAT_FET ON	Q3 is in bypass mode
0X A524	BAT_FET RESET	Q3 is in reset mode. The SYS is power down for 8s
0X A55F	BAT_FET Auto	Q3 is in auto mode with current mirror and forward regulation function.
0X A576	SHIP	LP4081 enters ship mode. 5V at BUS exit ship mode.

Watchdog

A 40s typical wait time watchdog is integrated. The Bluetooth SoC should write the WTD bit to 1 before time expires.

When the watchdog timer expiration, all the power FETs are forced to be turned off 8s. In this way, the SoC can reset itself. All the registers recover to the default values after watchdog expires.

Once be enabled, the watchdog is always active, either the input voltage or the battery is present.The watchdog can be turned off to save quiescent current by setting EN_WTD bit to 0.

Thermal Shutdown

When the internal junction temperature of LP4081 exceeds the thermal shutdown threshold of 150° C, the LP4081 disables all the power paths. The LP4081 recovers to the default setting after the junction temperature falls to the 130 ° C .

I2C Bus and Interrupt

The LP4081 has an I2C bus with an interrupt IRQb pin and the internal registers. The LP4081 operates as a slave device and the I2C slave address is 6BH (7bit, 1101011), a 1 or 0 should be placed at the end of the address which represents read or write operation. The interrupt pin IRQb is an open-drain output that pulls to low for 256us when an interruptible event happens in the chip. These events are included:

- Input power is present or removed.
- SYS pin short circuit happens
- Trickle charge timer expires
- Fast charge timer expires
- Watchdog timer expires
- charge status changes
- Battery is fully charged
- Battery voltage is UVLO

All of the SDA, SCL and IRQb are open-drain outputs. SoC can pull up these pins to the digital IO power rail internally.

DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

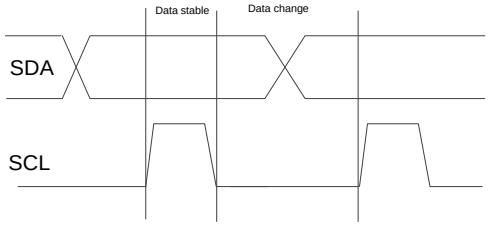


Figure 11. I2C Data validity

Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the SDA line while the SCL is high means a data transfer starts. A rising edge on the SDA line while the SCL is at high means a data transfer stops.

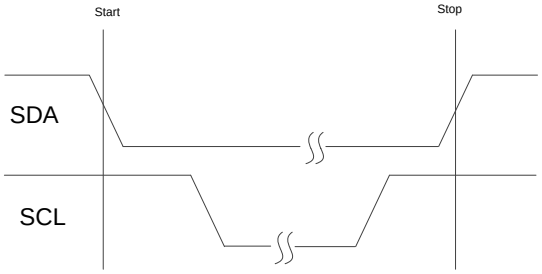


Figure 12. I2C Start and Stop Conditions

Byte format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

Single Byte Read and Write

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 13. Single byte write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK
							8 bit	1bit	1bit
							Data from Address	NACK	STOP

Figure 14. Single byte read

Multi-Read and Multi-Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit							
START	Slave address	0	ACK	Register address	ACK	START							
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit		
				Data to Address	ACK	Data to Address	ACK	.....	Data to Address	ACK	stop		

Figure 15. Multi-byte write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit					
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1					
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit		
				Data from Address	ACK	Data from Address	ACK	.....	Data from Address	NACK	stop		

Figure 16. Multi-byte read

Register Maps

Table 2． Device Registers

Reg Name	Addr		7	6	5	4	3	2	1	0	Def
Status register 0	00H	RO	TRI_TE	TERM_TE	WTD_TE	BAT_UV	SCP	CHG	CHG	PGD	00
Mask register 0	02H	RW		mBAT_UV	mEOC	mSCP	mCHG	mPGD	mTimer	n/a	00
Control register 0	03H	RW			ICC_EXT	IDSI_LIM	IDIS_LIM	IIN_LIM	DIS	DIS	00
Control register 1	04H	RW	ITERM	ITERM	ITERM	BAT_CV	BAT_CV	BAT_CV	BAT_CV	BAT_CV	24
Control register 2	05H	RW	EN_CHG	VTRI	ICC	ICC	ICC	ICC	ICC	ICC	44
Control register 3	06H	RW	WTD	EN_WTD	n/a	EN_Tri_Timer	EN_Term	DPM	DPM	DPM	43

Note:**RO**: read only; **RC**: read and clear; **RW**: read and write

Status Register 0 /Address: 00H (default: 0x00)

Table 3． Status register 0

Bit	Symbol	Description	Read/Write	Default
7	Trickle_TE	=1 Trickle charge timer expiration	r	0
6	Term_TE	=1 Fast charge timer expiration	r	0
5	WTD_TE	=1 Watchdog timer expiration	r	0
4	BAT_UV	=1 battery UVLO	r	0
3	SCP	=1 SYS is short circuit	r	0
2	CHG	00: not in charging mode, 01: trickle	r	0
1	CHG	10: CC/CV 11: EOC	r	0
0	PGD	=1 when input is between UVLO and OVP.	r	0

Interrupt Mask Register/Address: 02H (default: 0x00)

Table 4．Interrupt mask register

Bit	Symbol	Description	Read/Write	Default
7		reserve	r/w	0
6	mbat_uv	Mask interrupt	r/w	0
5	meoc		r/w	0
4	mscp		r/w	0
3	mCHG		r/w	0
2	mPGD		r/w	0
1	mTimer		r/w	0
0		reserve	r/w	0

Control Register 0/Address: 03H (default: 0x00)

Register 03H sets masks for interrupts described in the interrupt register above.

Table 5 . Control Register0

Bit	Symbol	Description	Read/Write	Default
7		reserve	r/w	
6		reserve	r/w	
5	ICC_EXT	=1, All the charge related current extension by 2.5 times, including: trickle/CC/termination current =0, default setting, no extension function	r/w	0
4	IDIS_LIM	discharge current limit 00: 440mA 01: 1A 10:2A 11: 3A	r/w	0
3	IDIS_LIM		r/w	0
2	IIN_LIM	input current limit =1: 1.5A, =0: 650mA	r/w	0
1	DIS[1]	BAT_FET operation mode control: 00: BAT_FET bypass mode, 01: SYS power down 8s, 10: auto mode, 11: ship mode	r/w	0
0	DIS[0]		r/w	0

Control Register 1/Address: 04H (default: 0x24)

Table 6 . Register 3

Bit	Symbol	Description	R/W	Default
7	Iter[2]	Trickle and Termination current set: 000:1mA, 001:3 mA, 010:5 mA, 011:7 mA, 100:9 mA 101:11 mA, 110:13 mA, 111:15 mA All these current will be X 2.5 times when the ICC_EXT is set to 1	r/w	3mA 001
6	Iter[1]		r/w	
5	Iter[0]		r/w	
4	BAT_CV[4]	Battery CV voltage set: 00000:4.0V, 00001:4.05V, 00010:4.1V,00011:4.15V, 00100:4.2V, 00101:4.22V,00110:4.24V,00111:4.26V, 01000:4.28V,01001:4.3V 01010:4.32V,01011:4.34V,01100:4.35V,01101:4.36V, 01110:4.38V 01111:4.4V,10000:4.42V,10001:4.44V, 10010:4.46V,10011:4.48V, 10100:4.5V, 10101~1111: not valid	r/w	4.2V 00100
3	BAT_CV[3]		r/w	
2	BAT_CV[2]		r/w	
1	BAT_CV[1]		r/w	
0	BAT_CV[0]		r/w	

Control Register 2/Address: 05H (default: 0x44)

Table 7 . Register 4

Bit	Symbol	Description	R/W	Default
7	EN_CHG	=1: Charge enable. =0: Charge disable	r/w	0
6	VTRI	Trickle charge threshold set: =1: 3.0V =0:2.8V	r/w	1
5	ICC[5]	Constant current set: 000000:10 mA,000000~100010, 5mA/step, 10~180mA 100011:190mA, 10011~111111, 10mA/step, 190~470mA All the current is extended 2.5 times if ICC_EXT bit is set to 1	r/w	30mA 000100
4	ICC[4]		r/w	
3	ICC[3]		r/w	
2	ICC[2]		r/w	
1	ICC[1]		r/w	
0	ICC[0]		r/w	

Control Register 3/Address: 06H (default: 0x43)

Table 8． Register 5

Symbol	Description	R/W	Default
WTD	Write WTD 1 will reset watchdog timer SoC need write this bit to 1 before watchdog timer count out.	r/w	0
EN_WTD	=1 watchdog function is enabled =0 watchdog function is disabled	r/w	1
	Reserve	r/w	0
EN_Tri_Timer	=1 enable 0.75Hr trickle charge safety timer =0 disable 0.75Hr trickle charge safety timer	r/w	0
EN_Term	=1 stop charging after EOC, =0 continue charging after EOC until 3.75Hr safety timer time expiration	r/w	0
DPM[2]	VSYS DPM threshold: 000:3.0V, 001:3.2V, 010:3.4V, 011:3.6V, 100:3.8V, 101:4.0V, 110:4.2V, 111:4.4V	r/w	011
DPM[1]		r/w	
DPM[0]		r/w	

Application Information

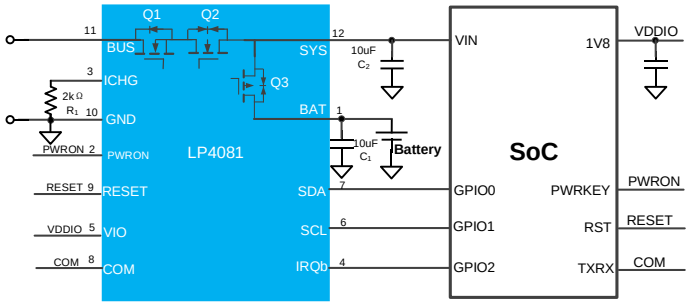


Figure 17. Typical Application Schematic

A typical application consists of the multi-function-in-one power management IC of LP4081 and a host SoC or MCU. When powering up in default mode, the battery CV voltage of LP4081 is 4.2V, the constant charging current is 30mA, the termination current and trickle charge current is 3mA. The minimum SYS voltage is 3.6V. The SoC can change all the default values by I2C interface.

Capacitor selection

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the BAT, and SYS pin to the GND pin. The BAT capacitor C_1 should be at least 6.3V rating with minimum 10uF capacitance. The SYS capacitor C_2 should be at least 6.3V rating with minimum 10uF capacitance. The BUS capacitor should not higher than 1nF to guarantee 115200bps UART communication.

Resistor selection:

The LP4081 support charge and discharge current monitor function for a simple gauge application. The current ratio is 1:400 when the LP4081 is charging and changes to 1:100 during discharging. The ratioed current is output at ICHG pin. A 5.1K resistor with 1% accuracy is recommended for the application with 250mA charging current and 50mA discharge current. A 2K resistor with 1% accuracy is recommended for the application with 250mA charging current and 100mA discharge current.

Application Waveforms

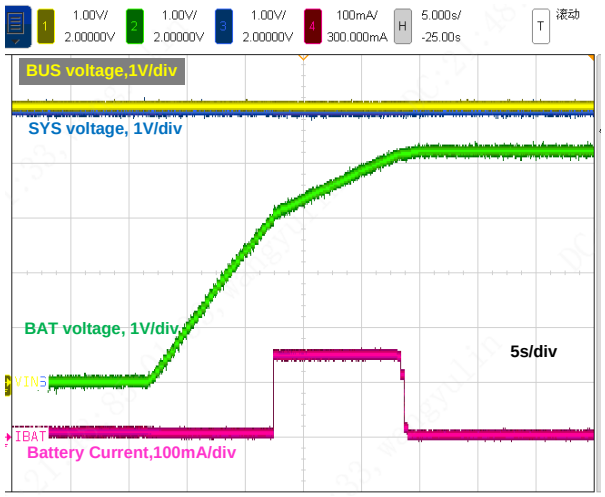


Figure 18. Battery Charging Curve

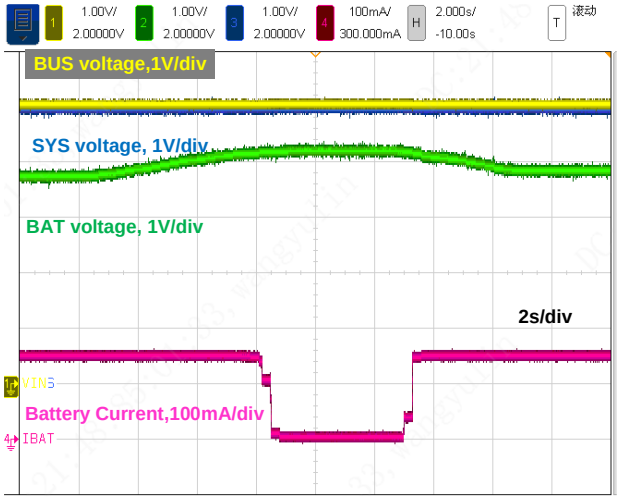


Figure 19. Auto-Recharge

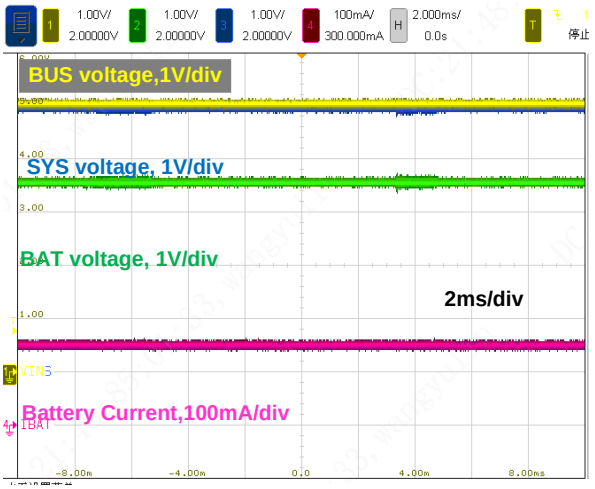


Figure 20. CC Steady State

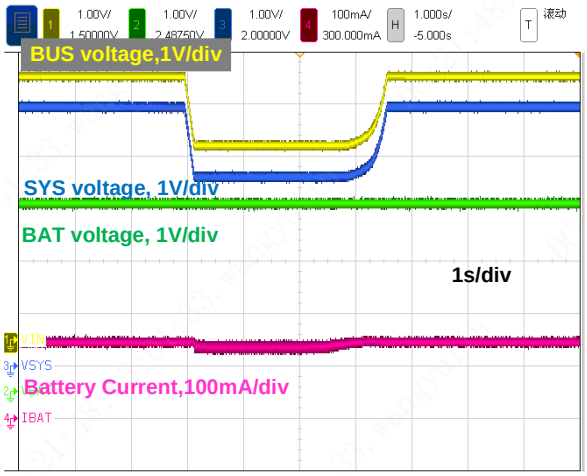


Figure 21. VIN Based PPM

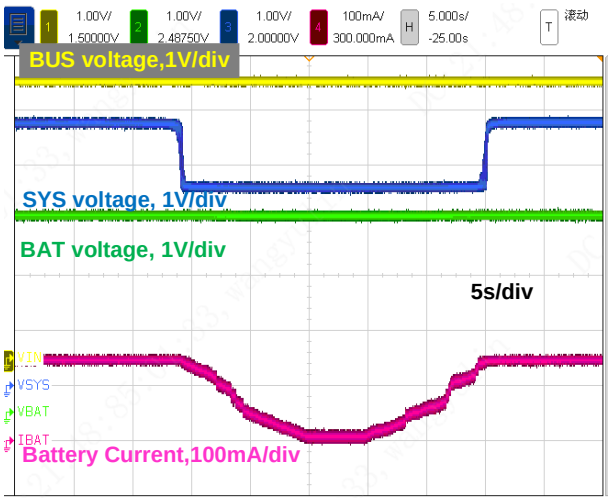


Figure 22. Input Current Limit Based PPM

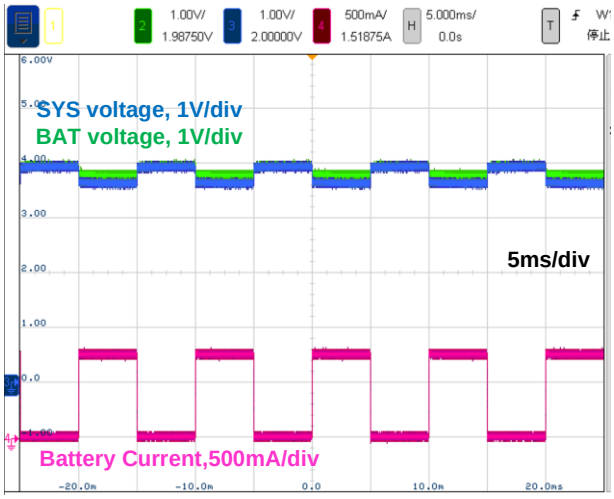


Figure 23. SYS Load Transient, 0A-0.8A-0A, BAT=4.0V, bypass mode

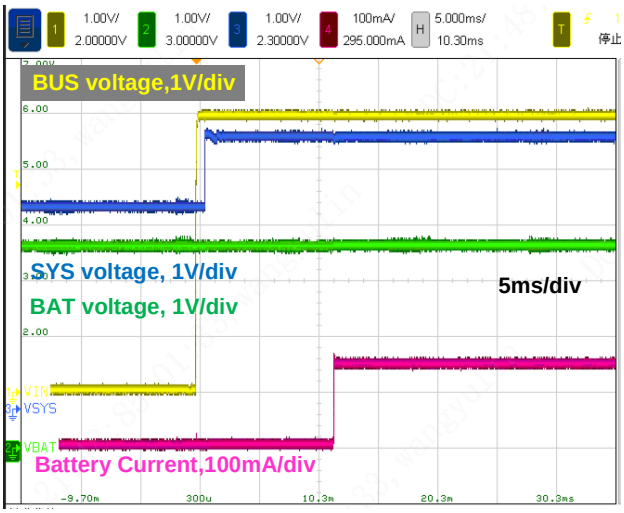


Figure 24. VIN Power Up

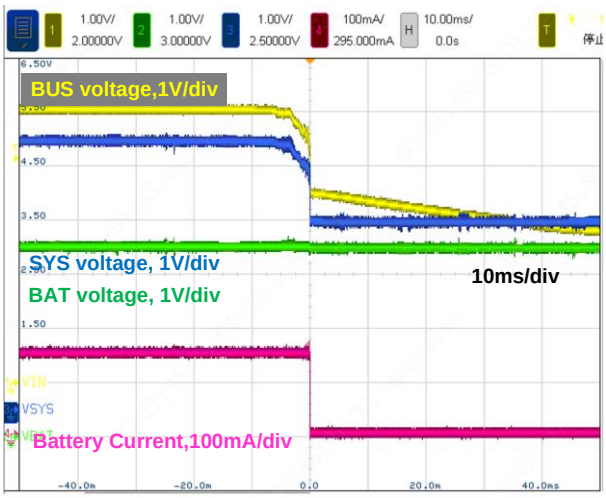


Figure 25. VIN Power Down

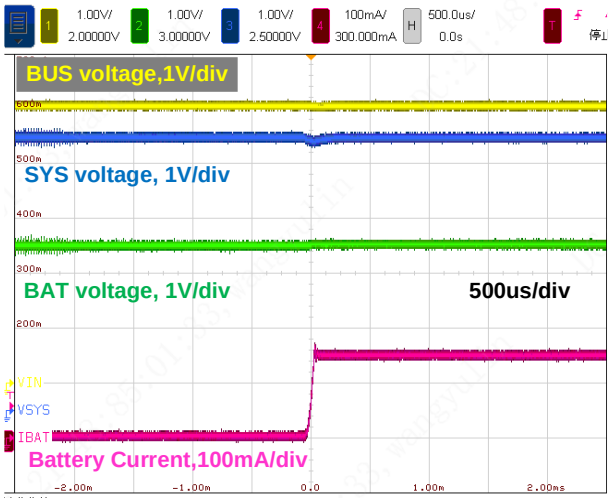


Figure 26. Charge Enable

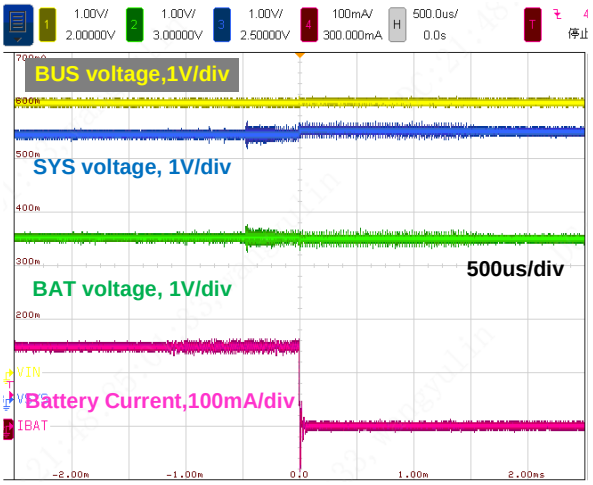


Figure 27. Charge Disable

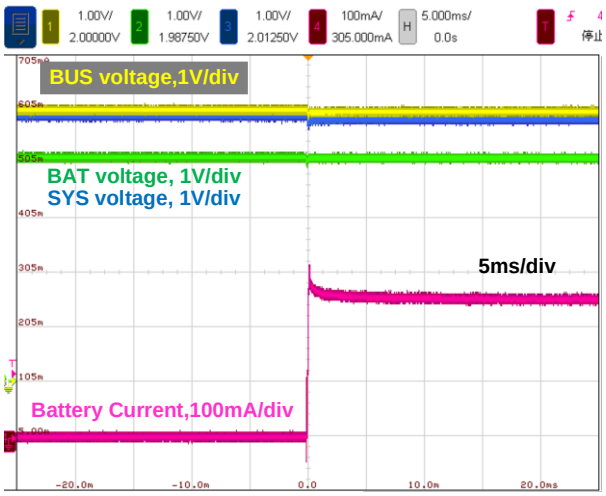


Figure 28. Battery Insert

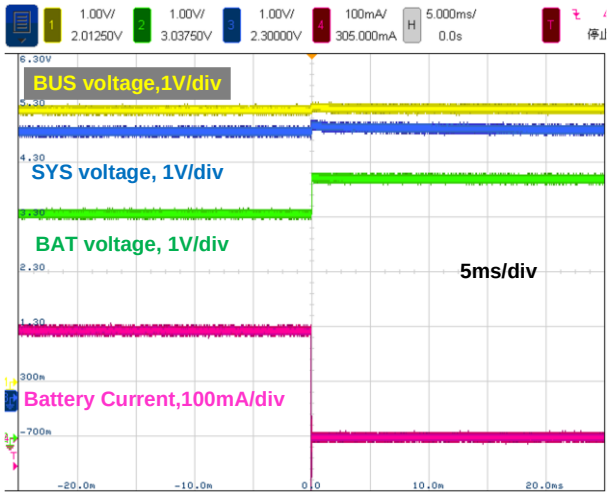


Figure 29. Battery Removal

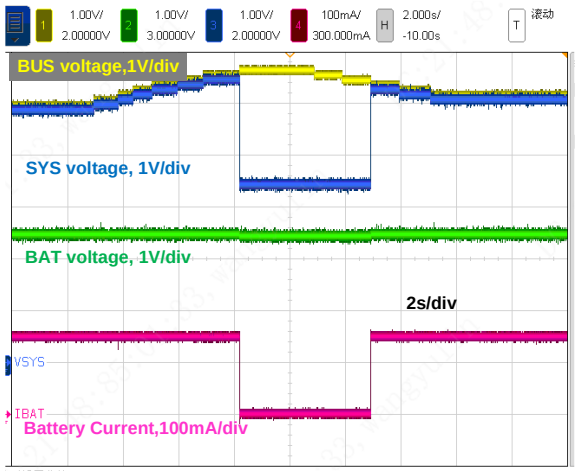


Figure 30. VIN OVP and recover

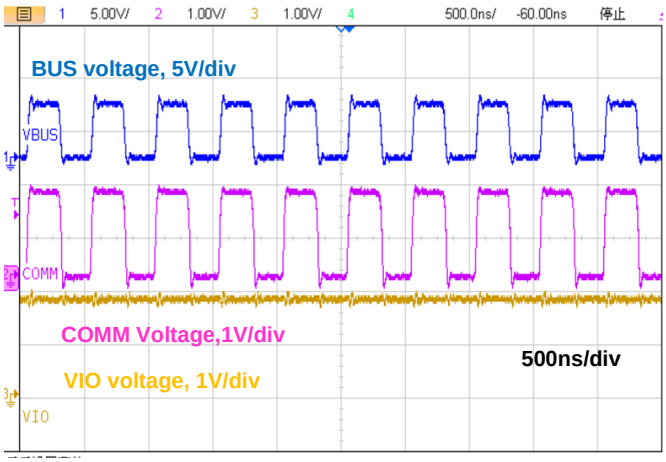


Figure 31. 2MHz UART communication level shift, SoC RX

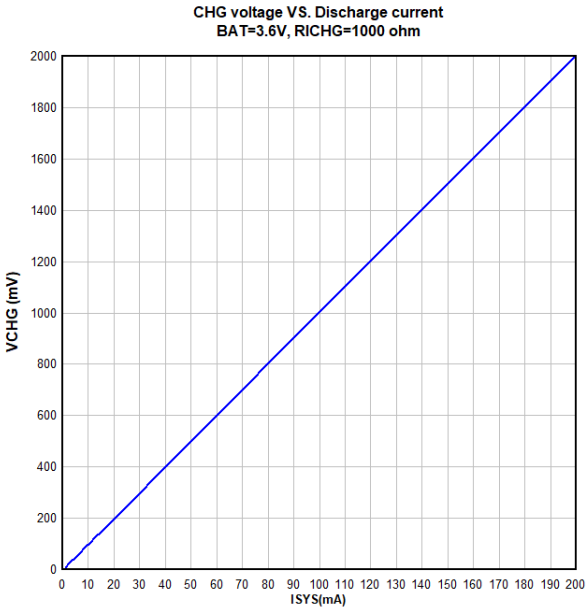


Figure 32. Discharging current monitor, VBUS=0V

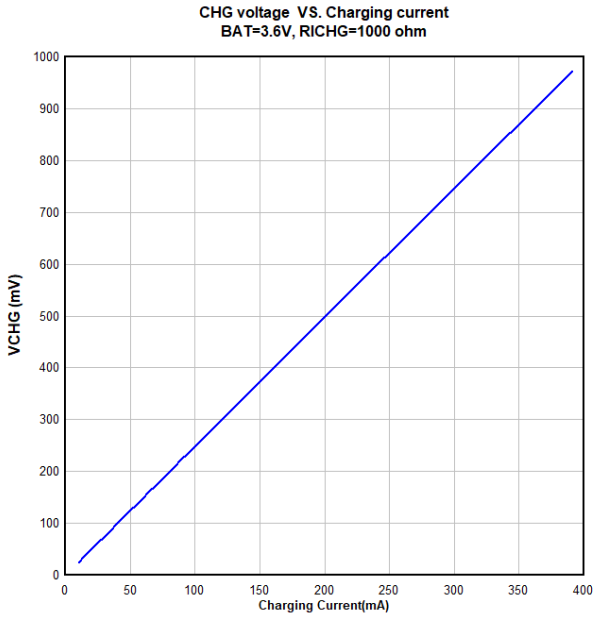


Figure 33. Charging current monitor, VBUS=5.0V

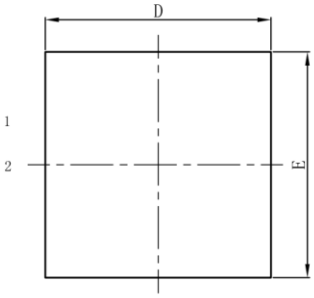
PCB Layout Guidelines

Please follow the rules when designing the PCB layout.

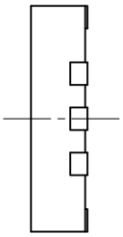
1. the high frequency filtering capacitor should be placed as close to the pin and GND as possible.
2. both the BUS , VBAT and GND power paths should be wide and short to improve the system efficiency.
3. no capacitors should be placed at the BUS pin to guarantee the UART communication speed.
4. the thermal pad should connected to the ground plane to help dissipating the power from the silicon.

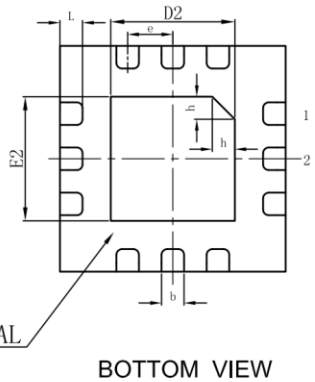
Packaging Information

2x2 QFN package



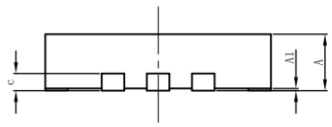
TOP VIEW





BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.00	1.10	1.20
e	0.40BSC		
E	1.90	2.00	2.10
E2	1.00	1.10	1.20
L	0.15	0.20	0.25
h	0.15	0.20	0.25
L/F载体尺寸 (mil)	53X53		



SIDE VIEW

Revision History

Revision	Date	Change Description
Rev 1p0	10/5/2022	Release Version 1.0