LP3988H

Ultra-Low Noise and High PSRR LDO

Features

- Low current consumption: 24μA (Typ)
- Wide input voltage range: 2.0V to 5.5V
- High output voltage accuracy: ±1.5%
- Ultra high PSRR: 98dB at 20mA/1kHz
- Ultra low noise: 10 μV_{RMS} (TBD)
- Low dropout voltage:
  - 165mV at 250mA (V_{OUT} = 1.8V)
  - 480mV at 500mA (V_{OUT} = 1.8V)
- Integrated over-current protection
- Active-high EN pin
- Robust ESD capability:
  - Human Body Model: 4 kV
  - Charged Device Model: 1 kV
- Available in small packages:
  - SOT23-5
  - TDFN-4 (1.0mm × 1.0mm)

Applications

- Wearable Devices
- Portable Medical Equipment
- PDAs, Mobile Phones GPS devices

Description

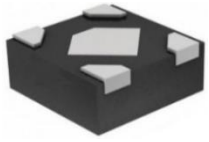
The LP3988H is a low-dropout voltage regulator with very low noise and high PSRR in ultra-small package. The LP3988H can deliver output current up to 600mA. The output voltage could be selected to 1.8V, 2.5V, 2.8V, 3.0V or 3.3V.

The LP3988H is integrated over current protection and short circuit protection in order to protect system abnormal.

The input and output capacitor as small as 1μF will be good enough for LP3988H.

The LP3988H is available in 4 pins ultra-small TDFN-4 package with only 1mm × 1mm size or normal SOT23-5 package.

SOT23-5



TDFN-4

Naming Information

LP3988H - □□ □□ □

- F: Pb-Free
- Package Type:
  - B5 : SOT23-5
  - QV : TDFN-4
- Output Voltage:
  - 18: 1.8V
  - 25: 2.5V
  - 28: 2.8V
  - 30: 3.0V
  - 33: 3.3V

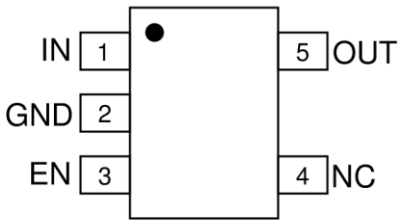
Ordering Information

Device	Marking	Moisture Sensitivity Level	Package	Shipping
LP3988H-18QVF	8CX	MSL3	TDFN-4	12K/REEL
LP3988H-25QVF	8DX	MSL3	TDFN-4	12K/REEL
LP3988H-28QVF	8HX	MSL3	TDFN-4	12K/REEL
LP3988H-30QVF	8GX	MSL3	TDFN-4	12K/REEL
LP3988H-33QVF	8EX	MSL3	TDFN-4	12K/REEL
LP3988H-18B5F	LPS 8CYWX	MSL3	SOT23-5	3K/REEL
LP3988H-25B5F	LPS 8DYWX	MSL3	SOT23-5	3K/REEL
LP3988H-28B5F	LPS 8HYWX	MSL3	SOT23-5	3K/REEL
LP3988H-30B5F	LPS 8GYWX	MSL3	SOT23-5	3K/REEL
LP3988H-33B5F	LPS 8EYWX	MSL3	SOT23-5	3K/REEL

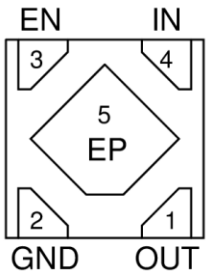
Marking indication:
Y: Production year, W: Production week, X: Production batch

Application Diagram

Pin Configuration



SOT23-5
(Top View)

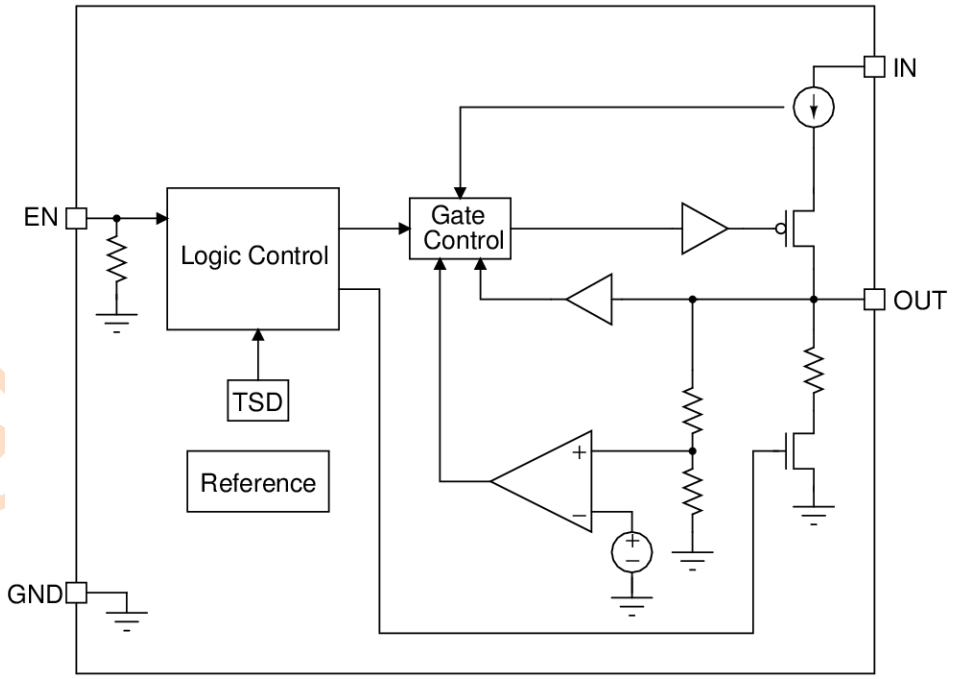


DFN-4
(Bottom View)

Pin Description

Pin No.	Name	Description
TDFN-4		
1	OUT	Regulated output. A minimum 0.1μF ceramic capacitor is needed from it to ground.
2	GND	Ground.
3	EN	Active-high enable pin. 1: enable the device. 0 or floating: disable the device.
4	IN	Input and power source. A small capacitor is recommended from this pin to ground.
5	EP	Exposed Pad for thermal dissipation. Need to be tied to ground.
SOT23-5		
1	IN	Input and power source. A small capacitor is recommended from this pin to ground.
2	GND	Ground.
3	EN	Active-high enable pin. 1: enable the device. 0 or floating: disable the device.
4	NC	Not connected.
5	OUT	Regulated output. A minimum 0.1μF ceramic capacitor is needed from it to ground.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- IN to GND ---------- -0.3V to 6V
- OUT to GND ---------- -0.3V to (V_{IN} + 0.3V) or 6V
- EN to GND ---------- -0.3V to 6V
- Output Current ---------- 700mA
- Maximum Junction Temperature (T_J) ---------- 150°C
- Maximum Soldering Temperature (At leads, 10 sec) ---------- 260°C

*Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- Maximum Power Dissipation (TDFN-4L, P_D, T_A <= 25℃) ---------- 480mW
- Maximum Power Dissipation (SOT23-5L, P_D, T_A <= 25℃) ---------- 610mW
- Thermal Resistance (TDFN-4L, θ_{JA}) (Note 2) ---------- 256 °C/W
- Thermal Resistance (SOT23-5L, θ_{JA}) (Note 2) ---------- 203 °C/W

*Note 2: Measured using 2S2P JEDEC standard PCB with ambient temperature < 25°C

Electro-Static Discharge and Latch-up

- HBM (Human Body Model, JEDEC JS-001) ---------- 4000V
- CDM (Charged Device Model, JEDEC JS-002) ---------- 1000V

Recommended Operating Conditions

- Input and supply voltage on IN ---------- 2.5V to 5.5V
- Output DC current ---------- Up to 600mA
- Input and Output capacitor ---------- > 1μF
- Operating ambient temperature ---------- -40°C to 85°C

Electrical Characteristics

The parameters are specified under conditions: V_{IN} is equal to the greater value between $V_{OUT(NOM)}$ + 0.5V and 2.0V, -40°C ≤ T_J ≤ 85°C, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Units
Output Voltage at 25°C	V_{OUT}	VIN = 2.8V, LP3988H-18B5F/QVF	1.77	1.80	1.83	V
		VIN = 3.5V, LP3988H-25B5F/QVF	2.46	2.50	2.54	V
		VIN = 3.8V, LP3988H-28B5F/QVF	2.76	2.80	2.84	V
		VIN = 4.0V, LP3988H-30B5F/QVF	2.95	3.00	3.05	V
		VIN = 4.3V, LP3988H-33B5F/QVF	3.24	3.30	3.36	V
Output voltage accuracy		$V_{OUT(NOM)}$ = 1.8V, T_J = 25°C	-1.5		1.5	%
Output voltage accuracy over temperature		$V_{OUT(NOM)}$ = 1.8V, -40°C ≤ T_J ≤ 85°C	-2.0		2.0	%
Input quiescent current	I_Q	V_{IN} = 2V to 5.5V, V_{EN} = V_{IN}, no load		24		μA
Input shutdown current	I_{SHDN}	V_{IN} = 2V to 5.5V, V_{EN} = 0V, no load			1	μA
Line regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	I_{OUT} = 1mA, V_{IN} = ($V_{OUT(NOM)}$ + 1V) to 5.5V, T_A = 25°C		0.002		%/V
Load regulation	ΔV_{LOAD}	I_{OUT} = 1mA to 600mA, V_{IN} = $V_{OUT(NOM)}$ + 1V, T_A = 25°C		12		mV
Dropout voltage in SOT23-5	V_{DROP}	$V_{OUT(NOM)}$ = 1.8V, I_{OUT} = 250mA, T_A = 25 °C		165		mV
		$V_{OUT(NOM)}$ = 1.8V, I_{OUT} = 500mA, T_A = 25 °C		480		mV
Output current limit	I_{LIM}	$V_{OUT(NOM)}$ = 1.8V, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$		960		mA
Output voltage noise	V_{NOISE}	BW = 10Hz to 100kHz, I_{OUT} = 20mA		10		μV_{RMS}
Power supply rejection ratio	PSRR	V_{IN} = $V_{OUT(NOM)}$ + 1V, I_{OUT} = 20mA, f = 1kHz, ΔV_{RIPPLE} = 0.2 × V_{PP}		98		dB
EN logic high voltage level	V_{IH}		1.1			V
EN logic low voltage level	V_{IL}				0.4	V
EN pull-down current	I_{EN_PD}			200		nA
Thermal Shutdown Threshold	T_{SD}			160		℃
Thermal Shutdown Hysteresis	ΔT_{SD}			30		℃
Output discharge resistance	R_{DIS}	V_{EN} = 0V		300		Ω

Function Description

Overview

The LP3988H is a Low dropout voltage regulator with ultra-low noise and ultra-high PSRR. It has fixed output voltage with good transient performance and no external setting resistors needed. The product is available in ultra-small package 1mm x 1mm TDFN-4 or traditional SOT23-5.

Selectable output voltage

The product will output fixed voltage as long as the input voltage is higher than $V_{OUT(NOM)}$ + V_{DROP}. $V_{OUT(NOM)}$, the output voltage, can be selected.

Enable function

The EN pin is an active high Logic input pin that is compatible with 1.8V control logic. The internal power element is turned off when EN pin is tied low.

When the EN pin is pulled high, the LP3988H will be activated and output voltage according to setting.

Auto discharge

The LP3988H has a quick discharge function. When the device is disabled by pulled down EN pin, a discharge resistor is connected between OUT and GND. The resistance is 300Ω (typical).

Power Supply Rejection Ratio

The LP3988H is working with ultra-high Power Supply Rejection Ratio (PSRR). By selecting proper output capacitor and PCB layout, the PSRR could even be tuned to higher.

Over current protection

The device features a current limit function when the over current event is detected to reach 960mA (Typ). The output current will be clamped and output voltage will drop accordingly, as in the *Electrical Characteristics Table*.

Application Information

Capacitor consideration

External capacitors on IN and OUT are recommended in application, 1μF for C_{OUT} and C_{IN} at least. Closer placement of the capacitors to the device, both IN and OUT, would be better for stability.

Power Dissipation

The internal power dissipation from the power MOSFET, when it is turned on, is the main source of junction temperature rising. In this case, the power dissipation and the junction temperature in conducting mode can be calculated as following:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

P_D: Power Dissipation (W)

V_{IN}: Input voltage (V)

V_{OUT}: Output voltage (V)

I_{OUT}: Output current (A)

$$T_J = P_D \times \theta_{JA} + T_A$$

T_J: Junction temperature (°C)

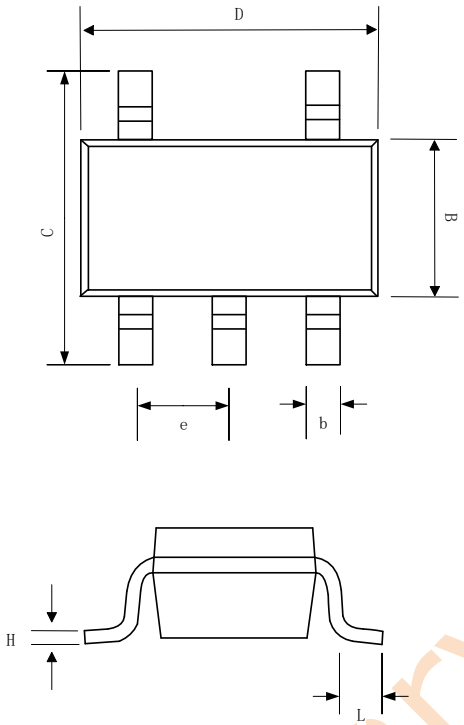
θ_{JA}: Package thermal resistance (°C /W) (Note 4)

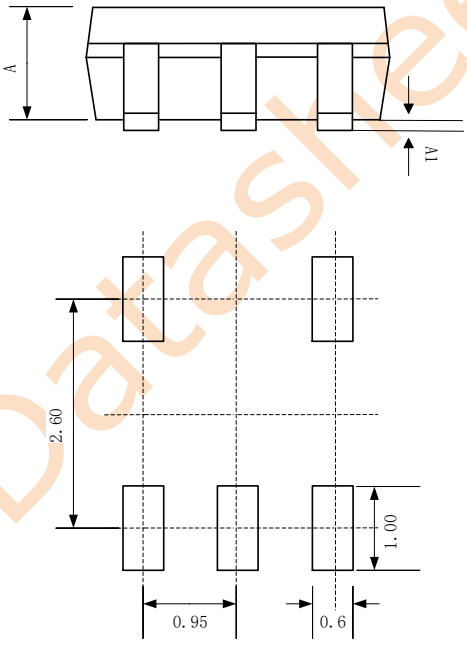
T_A: Ambient temperature (°C)

***Note 4: The calculation base on thermal resistance is only valid in Lab condition. The value of θ_{JA} could change in customer PCB environment.**

Package Dimensions

SOT23-5

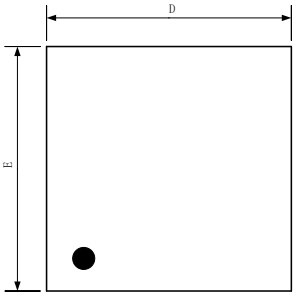




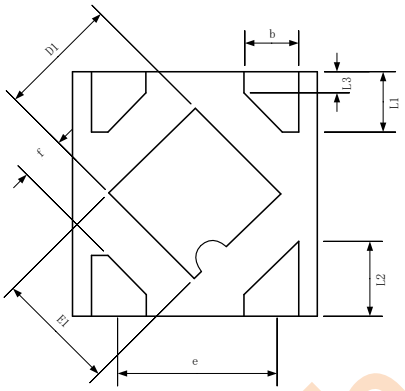
Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e		0.95BSC	
H	0.080	0.152	0.254
L	0.300	0.450	0.610

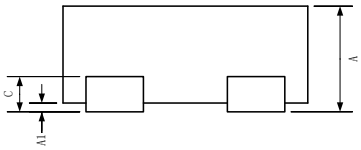
TDFN-4, 1mm x 1mm



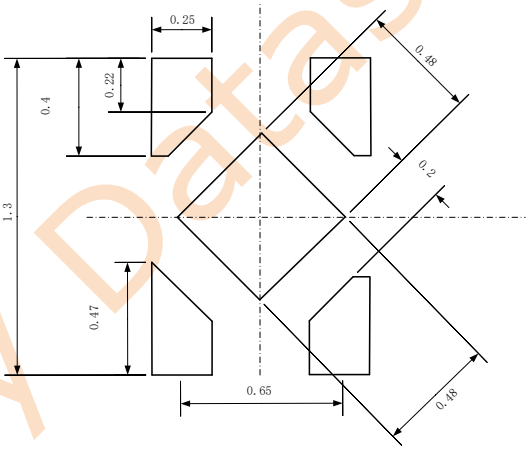
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.07	0.12	0.17
D	0.95	1.00	1.05
D1	0.43	0.48	0.55
E	0.95	1.00	1.05
E1	0.43	0.48	0.55
e	0.65BSC		
L1	0.2	0.25	0.30
L2	0.27	0.32	0.37
L3	0.09REF		
f	0.18REF		