LED Driver with PWM Dimming Control

General Description

The LP3354 contains a PWM boost driver which uses current mode control and fixed frequency operation to regulate the LED current. The LED current is sensed through an external current sense resistor. The voltage across the sensing resistor is compared with feedback voltage, the error amplified to control the pulse width of the power switch thus to regulate the current flowing the LED. Also, the feedback voltage can be programed by IIC interface.

Otherwise, The LP3354 offers external frequency PWM dimming method for a wide range of dimming control.

Other features include over current protection (OCP), output over voltage protection (OVP), and under-voltage lockout (UVLO). The LP3354 is available in a space saving SOP-10 (1mm pitch) and DFN-10 (0.5mm pitch) package.

Features

- Wide V_{IN} Range: 7V to 24V
- Programmable FB Voltage from 0.125V to 0.9V
- Current-Mode PWM Controller
- External PWM Dimming Mode
- Under-Voltage Lockout
- Over Voltage Protection
- Over Current Protection
- Over-Temperature Protection
- Available in SOP-10, DFN-10
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT LCD TV
- TFT LCD Monitor
- Flat Panel Display

Order Information

LP3354□□□
- F: Green
- Package Type
  - SO: SOP-10
  - QV: DFN-10

Marking Information

Device	Marking	Package	Shipping
LP3354SOF	LPS LP3354 YWX	SOP-10	4K/REEL
LP3354QVF	LPS LP3354 YWX	DFN-10	5K/REEL
Y: Year code. **W**: Week code. **X**: Batch number.			

Typical Application Circuit

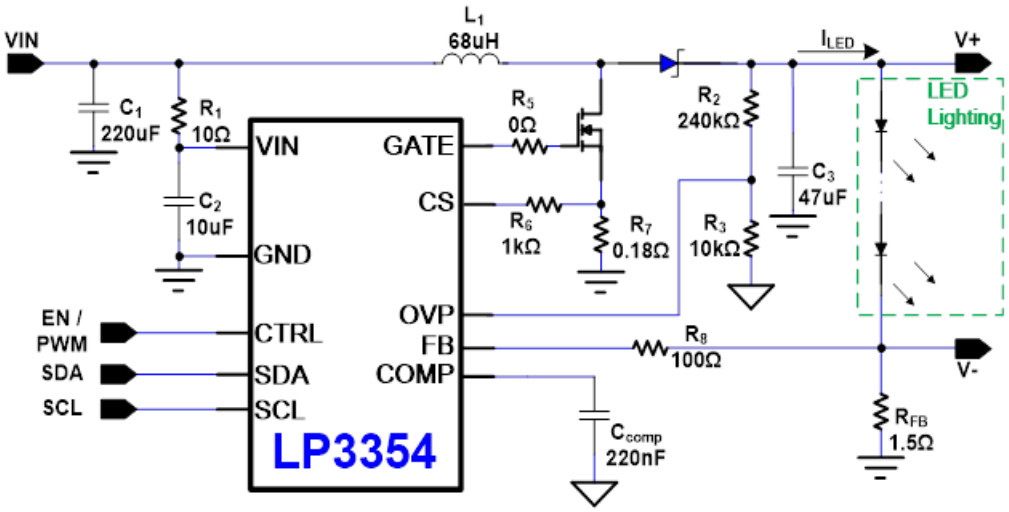


Figure 1. Typical Application Circuit of LP3354

Pin Configuration

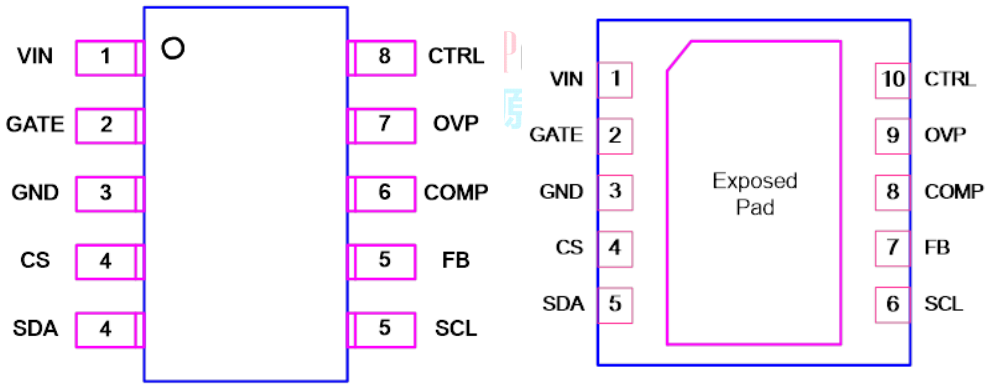


Figure 2. SOP-10 and DFN-10 Package Top View

Function Block Diagram

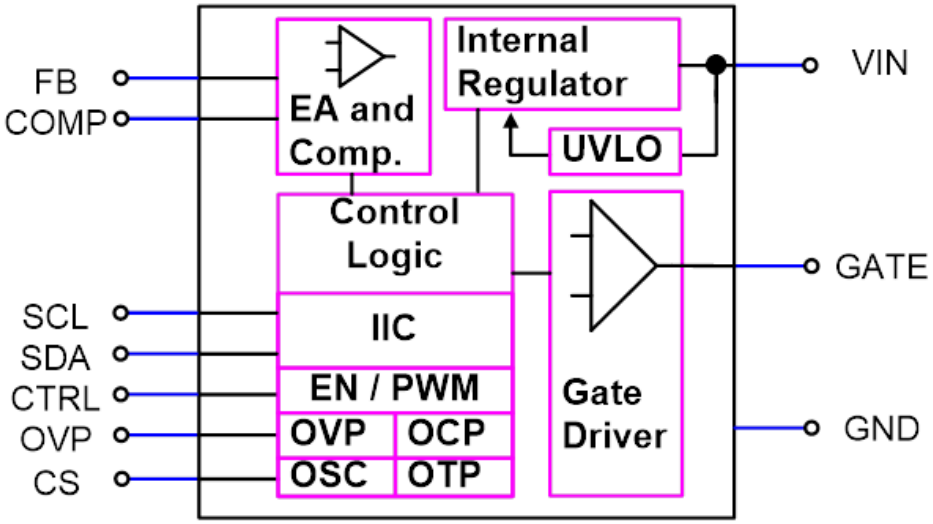


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	VIN	Input Supply Pin. Decouple with 10μF ceramic capacitor close to the pin.
2	GATE	External NMOS Gate Driver Pin.
3	GND	Ground.
4	CS	Current Sense Input Pin.
5	SDA	IIC Interface Data Signal.
6	SCL	IIC Interface Clock Signal.
7	FB	Regulator Feedback Input. Connect to an external resistive to set the output current.
8	COMP	Regulator Error Amplifier Compensation Pin.
9	OVP	Over Voltage Protection Sense Input. Connect to an external resistive voltage divider from the V+ to GND.
10	CTRL	Enable and External PWM Dimming Control Input Pin.
EP	GND	Exposed Pad. Connect EP to GND is suggested.

Absolute Maximum Ratings Note 1

- ✧ VIN to GND ---------- −0.3V to +30V
- ✧ GATE to GND ---------- −0.3V to +20V
- ✧ CS, FB, COMP, OVP, CTRL, SDA, SCL to GND ---------- −0.3V to +7V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40℃ to +150℃
- ✧ Operation Ambient Temperature Range (T_A) ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN}=12V, V_{CTRL}=5V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
Input Supply Voltage	V_{IN}		7	-	24	V
V_{IN} Supply Current	I_Q	Sleep Current	-	130	180	uA
		Operation Current	-	2	3	mA
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{IN} Rising	5.8	6.3	6.8	V
UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$	Falling Hysteresis	-	500	-	mV
Thermal Shutdown Threshold	T_{SD}	Temperature Rising	-	160	-	°C
Internal Oscillator Frequency	F_{OSC}		110	120	130	kHz
Reference Voltage	V_{REF}	Reference voltage at non-inverting input.	0.392	0.4	0.408	V
PWM Control						
Maximum Duty Cycle	D_{MAX}		93	95	97	%
CTRL Threshold Voltage	V_{IH}	Logic High.	1.5	-	-	V
	V_{IL}	Logic Low	-	-	0.7	
Error Amplifier						
Feedback Voltage	V_{FB}	R[00]=07h(typ.)	-2%	0.4	+2%	V
Open Loop Voltage Gain	Am		-	70	-	dB
Transconductance of EA	Gm		-	100	-	uA/V
Gate High Voltage Clamping	V_{Gate}		-	12	-	V
GATE Source Current	I_{Source}		-	30	-	uA
GATE Sink Current	I_{Sink}		-	60	-	uA
Gate Rise Time	T_{Rise}	1nF load	-	40	-	ns
Gate Fall Time	T_{Fall}	1nF load	-	20	-	ns
Protection Threshold						
Over Voltage Protection	V_{OVP}	OVP	1.9	2	2.1	V
Over Current Protection	V_{OCP}	OCP	260	380	500	mV
Fault Trigger Duration	T_{Fault}		-	35	-	ms
CS High Protection Threshold	V_{TH_CS}	Diode or Inductor short	1.1	1.2	1.3	V
CMP High Protection Threshold	V_{TH_CMP}	FB short to GND	2.9	3.2	3.5	V
SCP Threshold	V_{OVP_UV}	Normal Operation	-	250	-	mV
		System Startup	-	400	-	mV

Application Information

1. IIC Interface Specification

The LP3354 can modify the parameters easily by IIC bus. The slave address is shown as below.

Slave Address							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**W/R**
1	0	0	1	0	0	1	0/1

IIC is a two-wire serial interface developed, the bus consists of a clock line (SCL) and a data line (SDA) with pull-up structures. The LP3354 works as a slave mode. The data transfer protocol is following IIC-Bus Specification's standard mode (100kbps) and fast mode (400kbps).

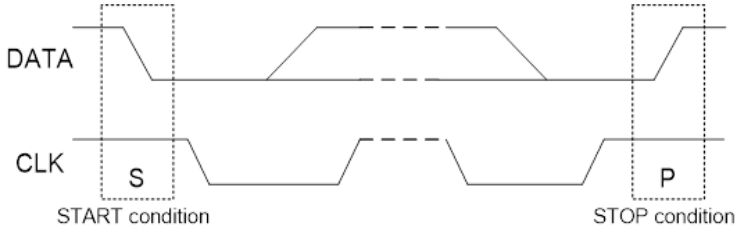


Figure 4 START and STOP Conditions

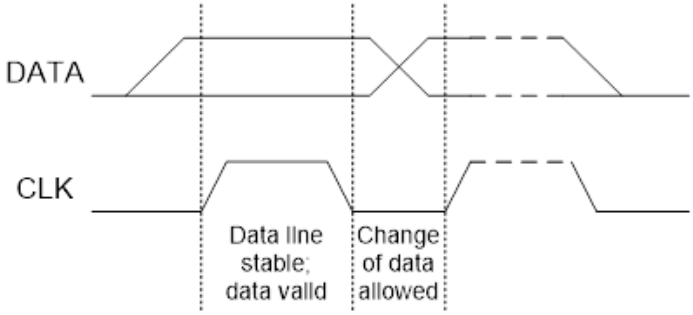


Figure 5. Bit Transfer on the Serial Interface

2. Write Data to Register

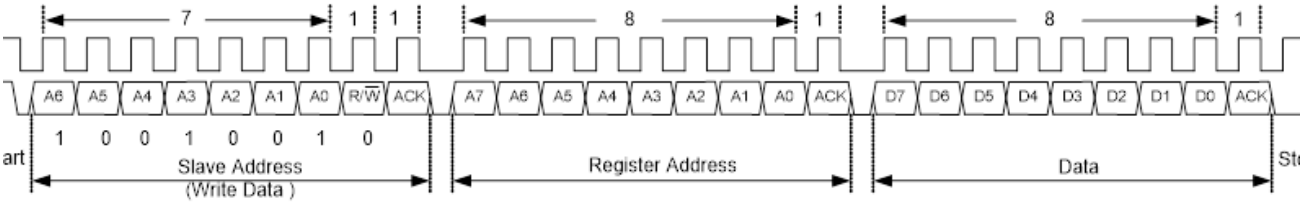


Figure 6. Write Single Byte Data to Register

3. Read Data to Register

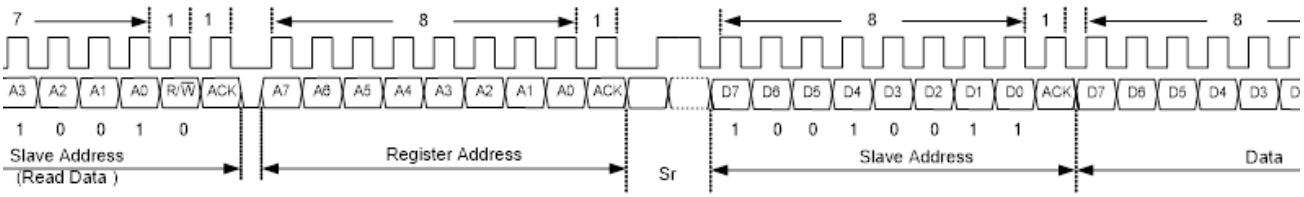


Figure 7. Read Single Byte Data from Register

Application Information (Continued)

4. IIC REGISTER MAP

The lowest bit number (0) represents the least bit, the highest bit number (7) represents the most bit, and R/W indicates whether the bit is read only (R), write only (W), or both read and write (R/W).

Block	Parameter	Symbol	Address	Range	Resolution	EEPROM Factory Value	BIT(Step)
DAC	Adjust FB Voltage	VFB	00h	00h - 1Fh	25mV	0Bh (0.4V)	5bits (32 Steps)

Set Feedback Voltage (Register Address – 00h)

Feedback Voltage							
00h	**Default Value: FB_DAC Register =0x0B (VFB=0.4V)**						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
-	-	-	VFB [4]	VFB [3]	VFB [2]	VFB [1]	VFB [0]

VFB [5:0]							
Register	**Volt (mV)**	**Register**	**Volt (mV)**	**Register**	**Volt (mV)**	**Register**	**Volt (mV)**
00000000	125	00001000	325	00010000	525	00011000	725
00000001	150	00001001	350	00010001	550	00011001	750
00000010	175	00001010	375	00010010	575	00011010	775
00000011	200	**00001011**	**400**	00010011	600	00011011	800
00000100	225	00001100	425	00010100	625	00011100	825
00000101	250	00001101	450	00010101	650	00011101	850
00000110	275	00001110	475	00010110	675	00011110	875
00000111	300	00001111	500	00010111	700	00011111	900

Application Information (Continued)

The LP3354 is designed in a current mode, constant frequency PWM boost converter. It can use dimming input that can by external control signal with a duty ratio of 1% - 100% in 100Hz to 50kHz. LP3354 also offers the protection features to protect the system such as output over voltage protection, boost diode disconnection protection, output short circuit protection and over temperature protection.

Under Voltage Lockout (UVLO)

The LP3354 had an UVLO internal circuit that enables the device once the voltage on the VIN voltage exceeds the UVLO threshold voltage.

Boost Controller

The LP3354 uses 120kHz fixed-frequency, current mode architecture to regulate the output current. The output voltage automatically adjusts its voltage to the LED forward voltage to improve performance.

Boost Loop Compensation

The feedback loop can be compensated with an external compensation network consisted of Rcomp, Ccomp (as Figure 1). Choosing Rcomp to set high frequency integrator gain for fast transient response and Ccomp to set the integrator zero to maintain loop stability.

Over Voltage Protection

The LP3354 converter has an over voltage protection by OVP pin. When the LEDs fail open circuit or LEDs are disconnected from the circuit, the over voltage function will monitor the output voltage through OVP pin to protect the converter. When LP3354 occur OVP, it will latch off until VIN is re-startup or CTRL input is recycled.

LED Current Setting

The LED current is specified by current sense resistor between the FB pin to ground. In order to have the accurate LED current, precision resistors are preferred. The LED current can be programmed by:

$$I_{LED}= V_{REF} /R_{FB}$$

Dimming Control

The LED brightness is controlled by the PWM signal at CTRL pin which has different duty cycle. LP3354 can accept an external PWM signal to CTRL pin in the range of 100Hz to 50kHz.

Over Temperature Protection

The LP3354 device enters over temperature protection (OTP) if its junction temperature exceeds 160°C (Typ.). During over temperature protection none of the device's functions are available. To resume normal operation, the junction temperature need cool down and the outputs will restart.

Current Sense and Over Current Protection (OCP)

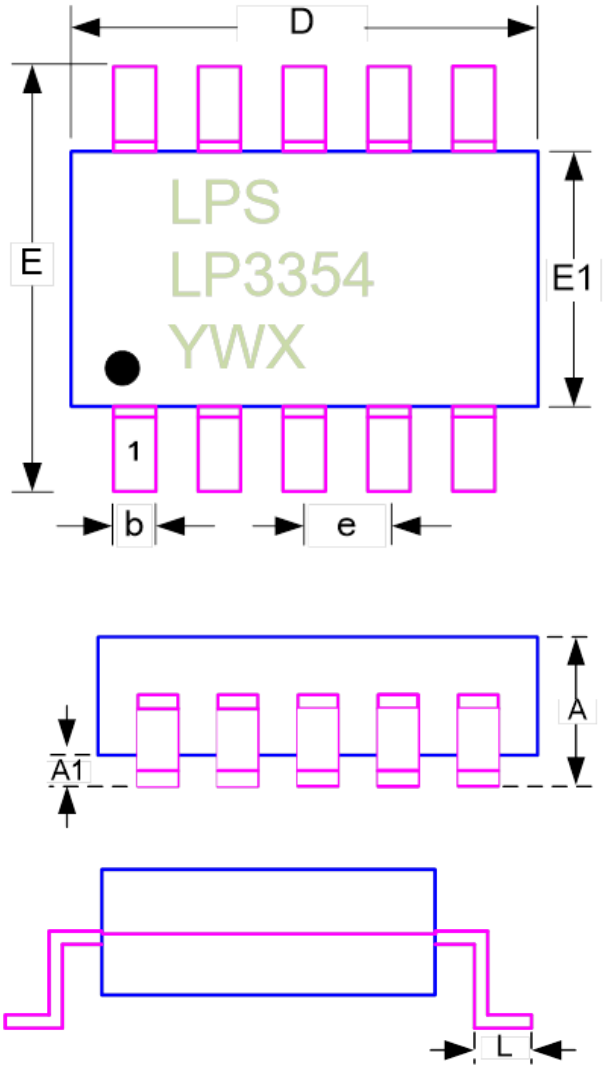
The over current protection level can be set by R7 (as Figure 1) and senses inductor current to compare with current limit value. When the inductor current exceeds the current limit, the switching will be turned off immediately. It prevents large current damaging the external component. The OCP level is calculated as:

$$I_{OCP}= V_{OCP} /R_7$$

The LP3354 uses a current mode control structure. The CS pin not only has current sense function but also build-in a slope compensation to avoid sub-harmonic oscillation. The additional slope compensation lessened the influence of the sensed current in the control loop.

Package Information

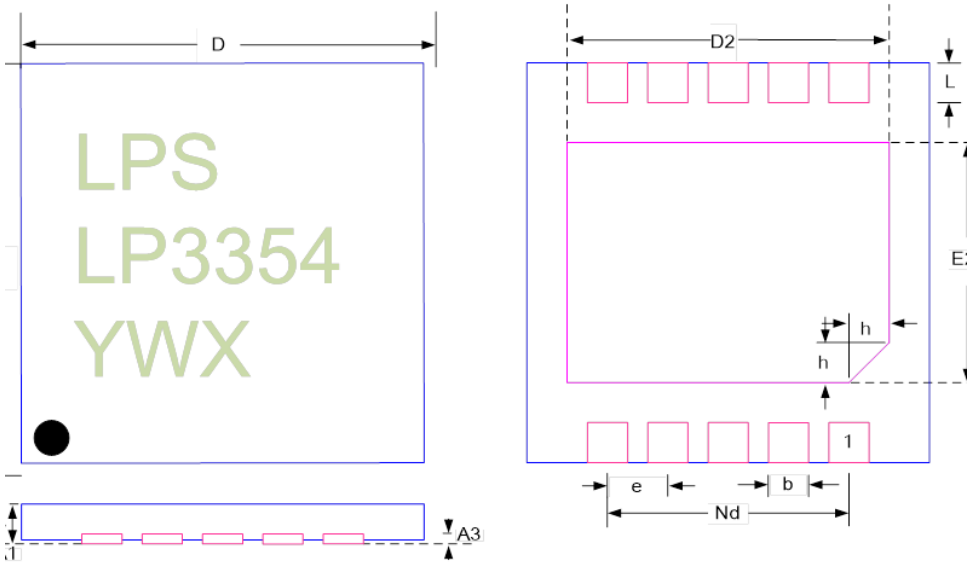
SOP-10 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.750
A1	0.100	--	0.230
b	0.300	--	0.400
D	4.700	4.900	5.100
E	5.800	6.000	6.200
E1	3.700	3.900	4.100
e	1.000BSC		
L	0.400	--	0.800

Package Information (Continued)

DFN-10 Package (3x3) pitch 0.5 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0. 750	0.800
A1	0	0.020	0.050
A3	0.180	0.200	0.250
b	0.180	0.250	0.300
D	2.900	3.000	3.100
D2	2.400	2.500	2.600
E	2.900	3.000	3.100
E2	1.450	1.550	1.650
e	0.500 BSC		
Nd	2.000 BSC		
L	0.300	0.400	0.500
h	0.200	0.250	0.300