# Over Voltage and Over Current Protection IC

## General Description

The LP5305 is a highly integrated circuits, it used to protect low voltage system from abnormal high input voltage. The IC continuously checks the input voltage, the input current, and the battery voltage. When the protection status is occur, the power MOS will turn off at the same time. The LP5305 is safety devices to ensure worked against accidents.

In case of the input voltage exceeds an OVP threshold voltage level, the power MOS will turn off within 1μs. The current limit can is adjustable by external resistor between ISET and GND. And the current is also limited to prevent charging the battery with an excessive current. The LP5305 also monitors the Li-ion battery voltage, when the battery voltage exceeds 4.35V, the IC will turn off the MOS.

Other features include over temperature protection and under-voltage lockout (UVLO). The LP5305 is available in a space saving DFN-8 package.

## Order Information

LP5305□□□
- F: Green
- Package Type
  - QV: DFN-8

## Features

- Withstand High Input Voltage Up to 26V
- Adjustable Over Current Protection
- Input Over Voltage Protection
- Battery Over Voltage Protection
- High Accuracy Protection Thresholds
- Fault Signal Output
- Enable Control
- Under Voltage Lockout
- Output Short-Circuit Protection
- Over-Temperature Protection
- Available in DFN-8
- RoHS Compliant and Halogen Free

## Applications

- Cell Phones
- Digital Cameras
- Portable Instruments

## Marking Information

| Device | Marking | Package | Shipping |
|---|---|---|---|
| LP5305QVF | LPS<br>LP5305<br>YWX | DFN-8 | 4K/REEL |
| Y is year code. W is week code. X is series number. | | | |

## Typical Application Circuit

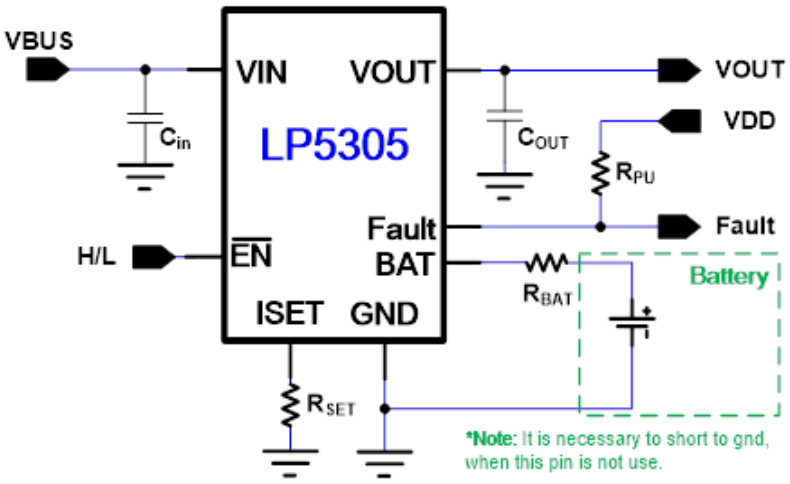



Figure 1. Typical Application Circuit of LP5305 .

## Pin Configuration

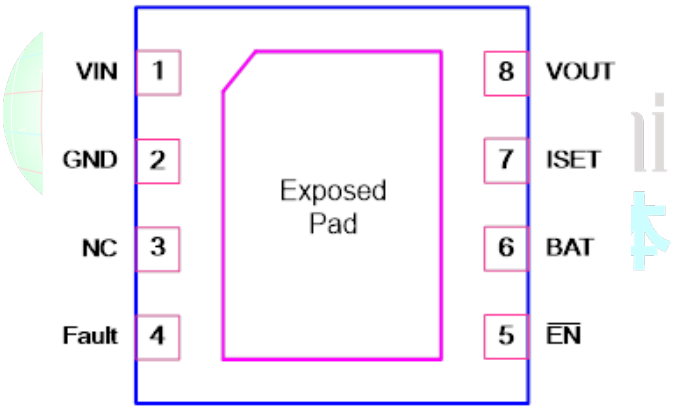



Figure 2. Package Top View

## Function Block Diagram

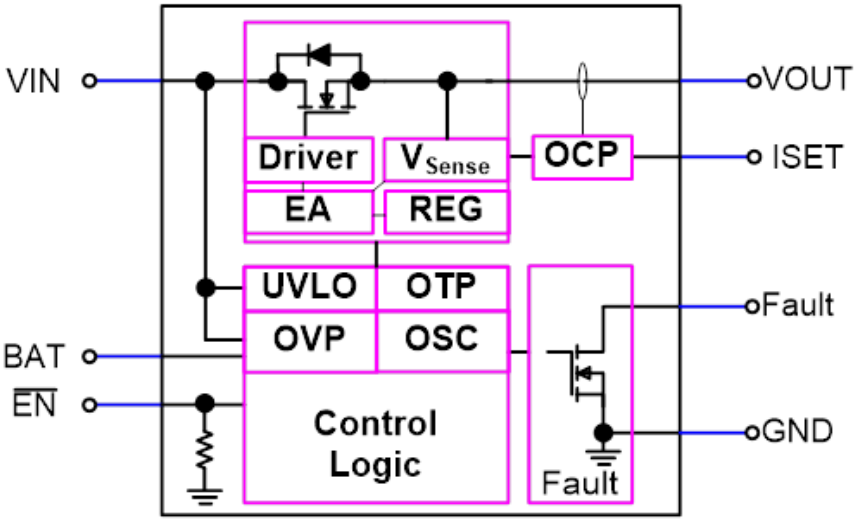



Figure 3. Function Block Diagram

## Functional Pin Description

| Pin NO. | DFN8 | Description |
|---|---|---|
| **VIN** | **1** | Power source input. Connect a ceramic capacitor between VIN and GND. |
| **GND** | **2** | Ground pad. Connect EP to GND is suggested. |
| **NC** | **3** | No connect. |
| **Fault** | **4** | Fault output pin. Open-drain output device status. |
| **$\overline{EN}$** | **5** | Enable pin. Connect it to logic high voltage to close power MOSFET, and connect logic low to turn on power MOSFET. EN is internally an sink current 15uA to ground. |
| **BAT** | **6** | Battery voltage detector input. It can short this pin to gnd, if doesn't use this function. |
| **ISET** | **7** | OCP level setting by an external resistor to GND. Connect a resistor to ground to set the overload current protection threshold: $I_{OCP}=25000\div R_{SET}$ |
| **VOUT** | **8** | Output through the power MOSFET. Bypass VOUT to GND with a ceramic capacitor. |
| | **EP** | Exposed pad. Connect EP to GND is suggested. |

## Absolute Maximum Ratings Note1

- ✧ VIN to GND ---------- -0.3V to +30V
- ✧ VOUT to GND ---------- -0.3V to +7V
- ✧ All Other Pin to GND ---------- -0.3V to +7V
- ✧ Operating Junction Temperature Range ($T_J$) ---------- -40℃ to 150℃
- ✧ Operation Ambient Temperature Range ---------- -40°C to +105°C
- ✧ Storage Temperature Range ---------- -60°C to +125°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C

**Note1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Information

- ✧ Thermal Resistance

  DFN-8, $\theta_{JA}$ ---------- 76.11 °C/W

  DFN-8, $\theta_{JC}$ ---------- 68.46 °C/W

## Recommended Operating Conditions

- ✧ Input Voltage, $V_{IN}$ ---------- 3.3V to 5V
- ✧ Output Current, $I_{OUT}$ ---------- 0.3A to 1.5A
- ✧ OCP Set Resistance, $R_{SET}$ ---------- 15kΩ to 90kΩ
- ✧ Junction Temperature, $T_J$ ---------- -40°C to 125°C

## Electrical Characteristics

($V_{IN}$ = 5V, $T_A$ = 25°C, Unless Otherwise Specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **General Function** | | | | | | |
| Power Source Voltage | $V_{IN}$ | $T_J$= +25 °C | 3.3 | 5 | 26 | V |
| Input UVLO Threshold | $V_{UVLO}$ | $V_{IN}$ Rising | 2.5 | 2.7 | 2.9 | V |
| UVLO Threshold Hysteresis | $\Delta V_{UVLO}$ | Falling Hysteresis | | 200 | | mV |
| Power On Deglitch Time | $T_{Deglitch}$ | Time measured from $\overline{EN}$ trigger to $V_{OUT}$ startup | | 8 | | ms |
| Soft Start Time | $T_{SS}$ | | | 8.2 | | ms |
| Power Source Current | $I_{IN}$ | $V_{IN}$=5V, $\overline{EN}$=L, no loading | | 400 | | μA |
| Shutdown Current | $I_{SD}$ | $V_{IN}$=5V, $\overline{EN}$=H | | 55 | | uA |
| Thermal Shutdown Threshold | $T_{SD}$ | No loading | | 140 | | °C |
| Thermal Shutdown Threshold Hysteresis | $\Delta T_{SD}$ | | | 20 | | °C |
| **Logic Function** | | | | | | |
| $\overline{EN}$ Threshold Voltage | $V_{ENH}$ | | 1.4 | | | V |
| | $V_{ENL}$ | | | | 0.4 | V |
| $\overline{EN}$ Input Resistance to GND | $I_{EN}$ | $\overline{EN}$=2V | | 15 | | uA |
| FAULT Output Logic Low | | Sink 5mA | | 0.2 | | V |
| FAULT Logic High Leakage Current | | $V_{Fault}$=5V | | | 10 | uA |
| **Power MOS** | | | | | | |
| Switch On Resistance | $R_{DS(ON)}$ | $I_{OUT}$=1A | | 160 | 250 | mΩ |
| **Regulation Function** | | | | | | |
| Output Voltage Regulation | $V_{LDO}$ | $V_{IN}$=5.7V | | 5.5 | | V |
| **Protection Functions** | | | | | | |
| Input Over Voltage Protect threshold | $V_{IOVP}$ | $V_{IN}$ from 5V to 9V | | 5.85 | | V |
| Input OVP propagation delay | $T_{OVP}$ | | | | 0.8 | us |
| Input OVP threshold Hysteresis | $\Delta V_{IOVP}$ | $V_{IN}$ from 9V to 5V | | 100 | | mV |
| Input OVP Recovery Delay Time | $T_{OVPR}$ | From ($V_{IOVP}$-$\Delta V_{IOVP}$) trigger to $V_{OUT}$ startup time | | 8.2 | | ms |
| Over Current Protection | $I_{OCP}$ | $R_{SET}$ = 24.9K, 3.3V<$V_{IN}$<$V_{IOVP}$ | 0.9 | 1 | 1.1 | A |
| Short Circuit Current | $I_{SCP}$ | $R_{SET}$ = 24.9K, $V_{OUT}$ short to GND | 0.65 | | | A |
| OCP Blanking Time | $T_{OCP}$ | | | 200 | | us |
| Over Current Recover Delay | $T_{OCR}$ | | | 65 | | ms |
| Battery Voltage OVP | $V_{BOVP}$ | $V_{BAT}$ from 3V to 5V | 4.275 | 4.35 | 4.41 | V |
| Battery OVP Hysteresis | $\Delta V_{BOVP}$ | $V_{BAT}$ from 5V to 3V | | 0.275 | | V |
| Battery OVP Blanking Time | $T_{BOVP}$ | | | 200 | | us |
| BAT Pin Leakage Current | $I_{BAT}$ | $V_{IN}$=0V~5V, $V_{BAT}$=4.4V | | | 10 | nA |

## Typical Performance Curves

$T_A$=25°C, $V_{IN}$= $V_{OUT}$=5V, $V_{BAT}$=4.2V, $V_{DD}$=5V, $V_{EN}$=0V, unless otherwise specified.

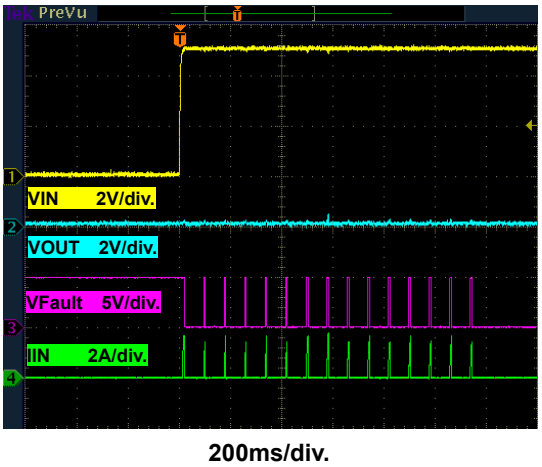



Figure 4. VOUT short to GND

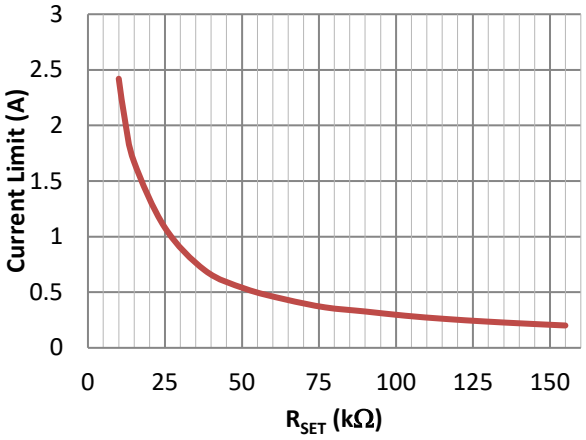



Figure 5. Current vs. RSET

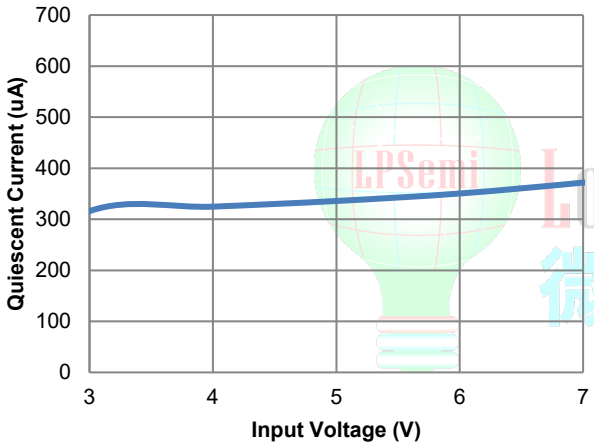



Figure 6. Input Voltage vs. Quiescent Current

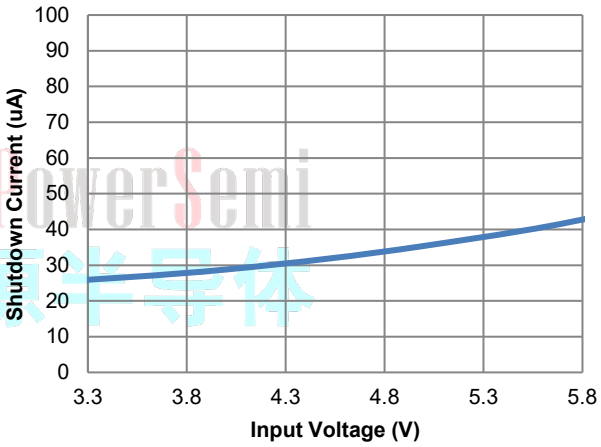



Figure 7. Input Voltage vs. Shutdown Current

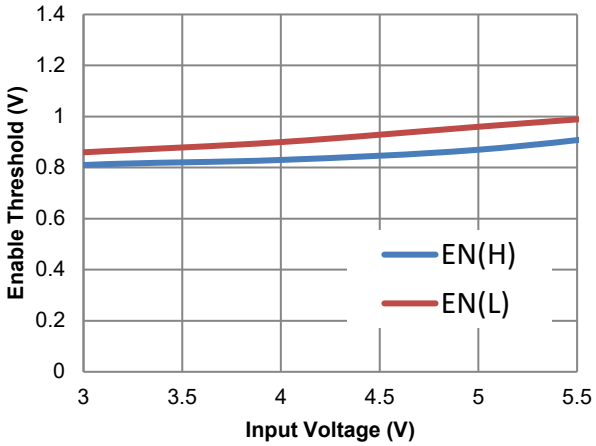



Figure 8. Input Voltage vs. Enable Threshold

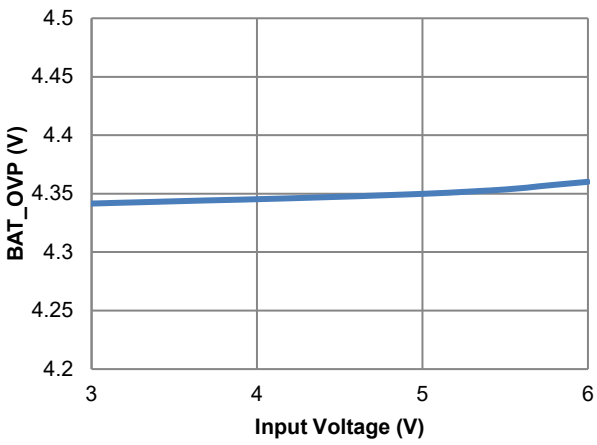



Figure 9. Input Voltage vs. Battery OVP

## Timing Diagram

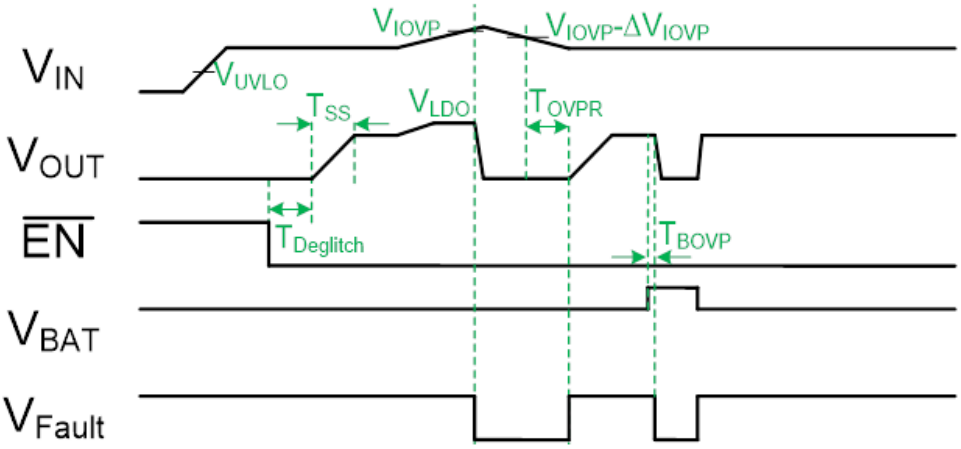



Figure 10. Timing Diagram

# Application Information

The LP5305 devices monitor the input voltage, battery voltage, and output current to protect the charging system of a Li-Ion battery. When enabled, the system is protected against input overvoltage by turning off an internal switch, immediately removing power from the charging circuit. For an over-current condition, the device limits the output current at the setting value, and if the over-current persists, the switch will turn off after a blanking time. Additionally, the device also monitors its own temperature and switches off if device too hot.

## Under Voltage Lockout (UVLO)

The LP5305 had an UVLO internal circuit that enables the device once the voltage on the $V_{IN}$ voltage exceeds the UVLO threshold voltage.

## Input Over Voltage Protection

The LP5305 Input has an over voltage protection to protect the battery charging system. When the VIN voltage rises above 5.85V(Typ.), the system will turns the switch off.

## Battery Over Voltage Protection

The battery overvoltage threshold $V_{BOVP}$ is internally set to 4.35V. If the battery voltage exceeds the threshold, the switch is turned off, and the Fault pin is go low. Once the battery voltage drops to ($V_{BOVP}$-$\Delta V_{BOVP}$), the switch is turned back on. And the switch is turned off permanently, when battery overvoltage occurs 15 times in one charge cycle. For cleared this event, the VIN power or EN need to re-cycle.

## Over Temperature Protection

The LP5305 device enters over temperature protection (OTP) if its junction temperature exceeds 140°C (Typ.). During over temperature protection none of the device's functions are available. To resume normal operation the junction temperature need cool down, and the outputs will restart.

## Enable Control

The LP5305 has an enable pin which can be used to enable or disable the device. When the EN pin is driven high, the switch is turned off. The EN pin has an internal pull-down resistor can be floating.

## Fault Flag

The FAULT pin is open-drain output.

- Input Over Voltage
- Output Over Current
- Battery Over Voltage
- Over Temperature

## Over Current Protection

The Over Current threshold can adjustable by a external resistor RSET connected from the ISET pin to GND. The equation is apply under below:

$$I_{OCP}=25000\div R_{SET}$$

If the output current exceeds the $I_{OCP}$ threshold, the device limits the current for a blanking duration ($T_{OCP}$). If the output current is over the $I_{SCP}$ for $T_{OCP}$, the switch will turn off. The Fault pin is set to low, too. The switches will re-soft start again after $T_{OCR}$. And the switch is turned off permanently; when over current event occurs 15 times in one charge cycle. For cleared this event, the VIN power or EN need to re-cycled.

## Layout Consideration

The proper PCB layout and component placement are critical for all circuit. LP5305 is meant to protect downstream circuit. Here are some suggestions to the layout design.

1. Connected all ground together with one uninterrupted ground plane, which include power ground and analog ground.
2. The input and output capacitor should be located as closed as possible to the chip and ground plane.
3. Other components should be located close to the chip.

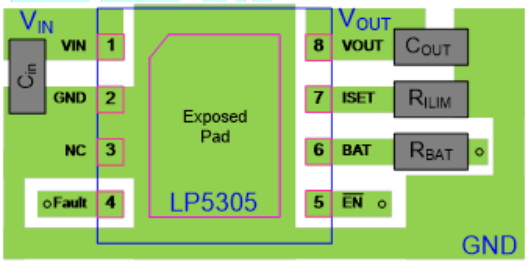
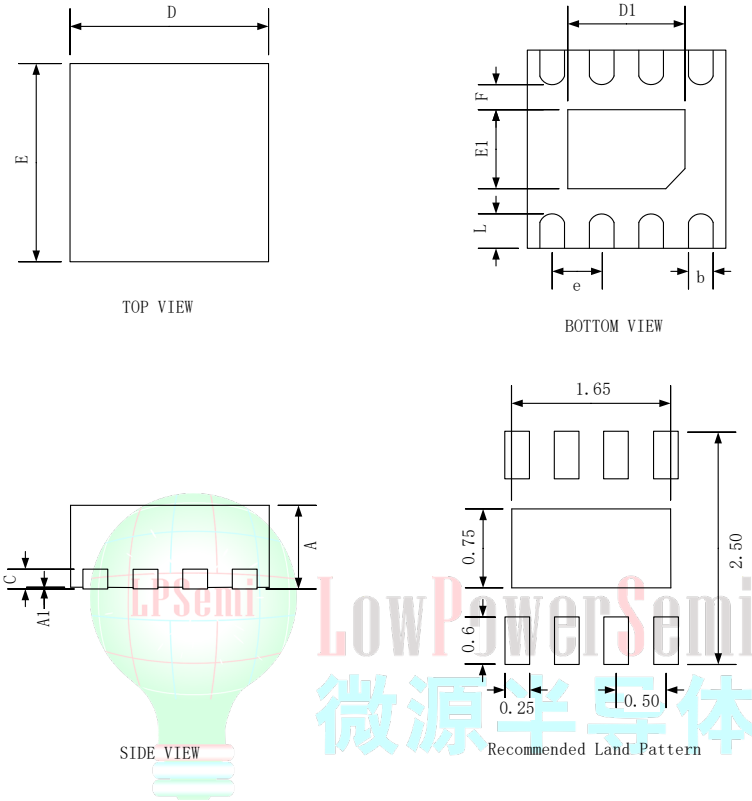



Figure11. Recommended PCB Layout Diagram

# Outline Information

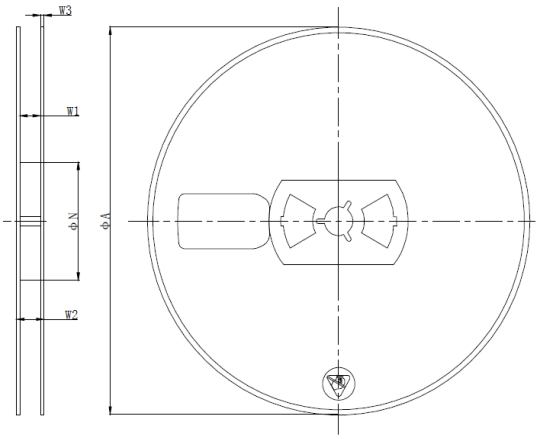
**DFN-8 Package (2x2) pitch 0.5 (Unit: mm)**




| SYMBOL | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | | 0.20 REF | |
| D | 1.90 | 2.00 | 2.10 |
| D1 | 1.10 | 1.30 | 1.65 |
| E | 1.90 | 2.00 | 2.10 |
| E1 | 0.60 | 0.75 | 0.85 |
| e | | 0.50 BSC | |
| L | 0.25 | 0.35 | 0.40 |
| F | 0.25 | 0.30 | 0.35 |

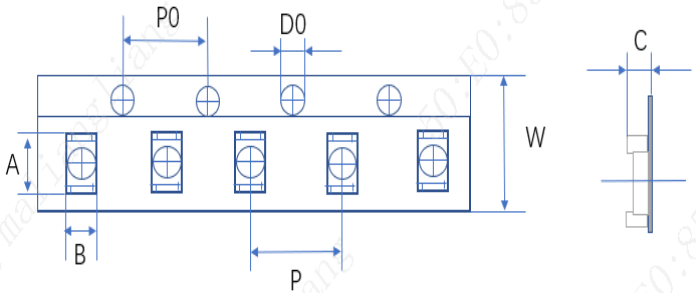
# TAPE AND REEL INFORMATION

REEL DIMENSIONS（Unit:mm）



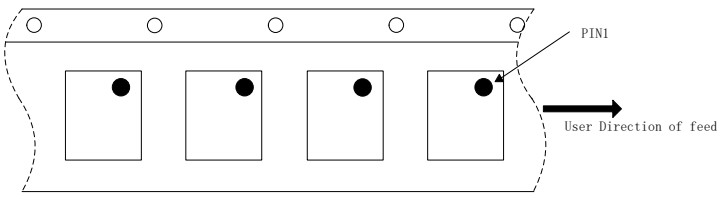

| ΦA | W2 |
|---|---|
| 180±4 | 12±2 |

TAPE DIMENSIONS（Unit:mm）




| A | B | P0 | P | D0 | W | C |
|---|---|---|---|---|---|---|
| 2.15±0.15 | 2.15±0.15 | 4.00±0.10 | 4.00±0.10 | 1.50±0.10 | 8.00±0.30 | 1.00±0.20 |

PIN1 AND TAPE FEEDING DIRECTION



## Classification of IR Reflow Profile

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| Preheat/Soak<br>Temperature Min(TSMIN)<br>Temperature Max(TSMAX)<br>Time(TS) from (TSMIN to TSMAX) | <br>100℃<br>150℃<br>60~120 seconds | <br>150℃<br>200℃<br>60~120 seconds |
| Ramp-up rate (TL to TP) | 3℃/second max | 3℃/second max |
| Liquidous temperature(TL)<br>Time(tL) maintained above TL | 183℃<br>60~150 seconds | 217℃<br>60~150 seconds |
| Peak package body temperature (TP) | For users TP must not exceed theClassification temp in Table 1. For suppliers TP must equal or exceedthe Classification temp in Table 1. | For users TP must not exceed theClassification temp in Table 2. For suppliers TP must equal or exceedthe Classification temp in Table 2. |
| Time(tP)* within 5℃ of the specified classification temperature(TC), see Figure1 | 20* seconds | 30* seconds |
| Ramp-down rate (TP to TL) | 6℃/second max | 6℃/second max |
| Time 25℃ to peak temperature | 6 minutes max | 8minutes max |
| * Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum. | | |

**Table 1Sn-Pb Eutectic Process - Classification Temperatures (TC)**

| Package Thickness | Volume mm3 <350 | Volume mm3 ≥350 |
|---|---|---|
| <2.5mm | 235℃ | 220℃ |
| ≥2.5mm | 220℃ | 220℃ |

**Table 2 Pb-Free Process - Classification Temperatures (TC)**

| Package Thickness | Volume mm3 <350 | Volume mm3 350~2000 | Volume mm3 ≥350 |
|---|---|---|---|
| <1.6mm | 260℃ | 260℃ | 260℃ |
| 1.6mm~2.5mm | 260℃ | 250℃ | 245℃ |
| >2.5mm | 250℃ | 245℃ | 245℃ |

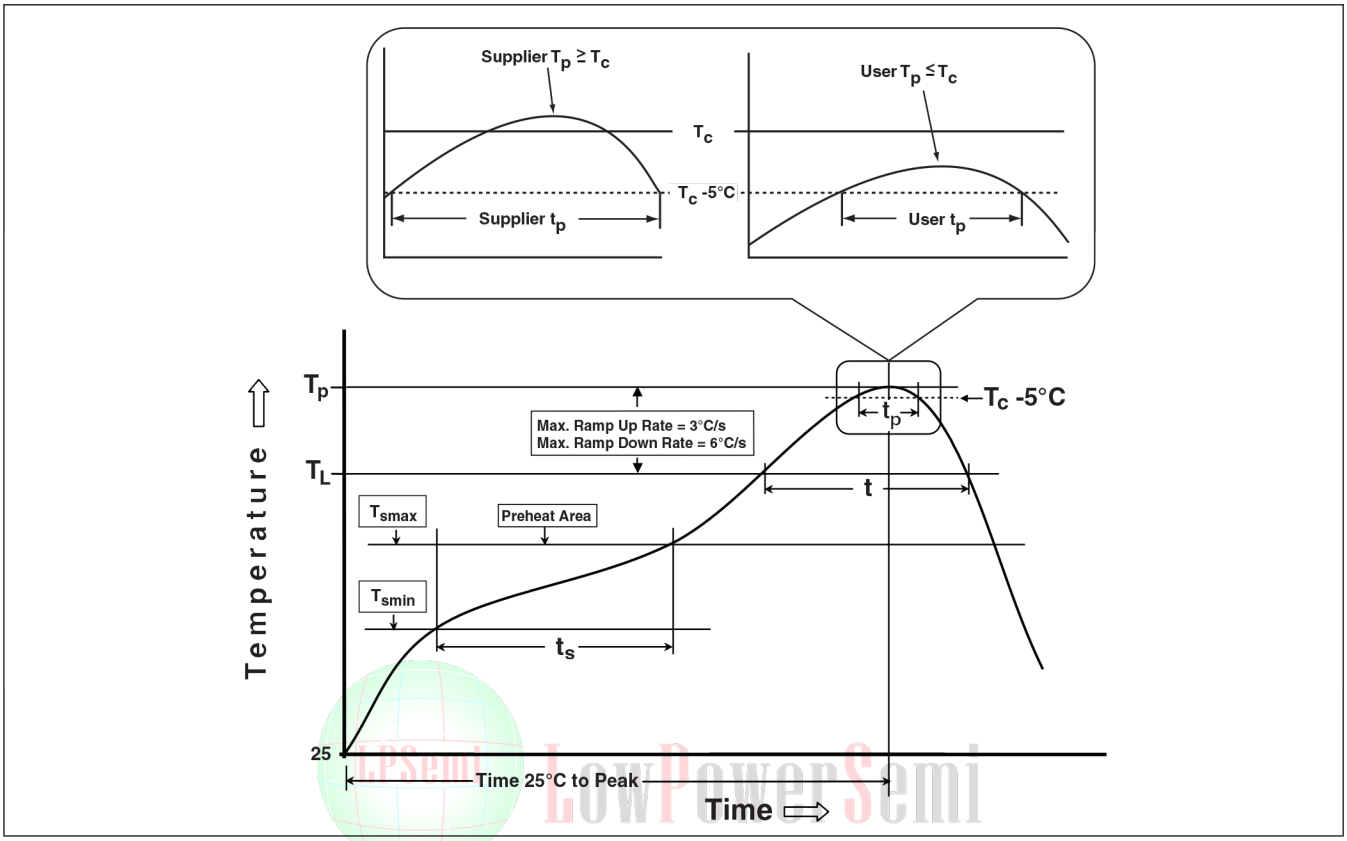



**Figure1Classification Profile (Not to scale)**

**Products conform to "JEDEC J-STD-020C" standards;**

**Products shipped conform to "Rohs" standards;**

**Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;**