Features

- Input Supply Range : 2.5V ~ 5.5V
- Wide VIN Range: 2.7V to 24V
- Current-Mode Boost Converter
- Integrated 2.5A/40V boost power MOS
- Built-in LED soft-start current control
- Six programmable current sinks
  Current up to 30mA per channel
  PWM dimming from 100Hz to 30kHz
  2.5% current matching
  3% current accuracy
- LED string open/short detection
- Over Voltage Protection
- Over Temperature Protection
- Under Voltage Lockout
- QFN-16 (3mm×3mm) Package
- RoHS Compliant and Pb-Free

Applications

- Notebook LED Backlight
- Monitor LED Backlight
- Tablet LED Backlight

Order Information

LP3352 □ □ □

- F:Green
- Package Type
  QV:QFN3X3-16

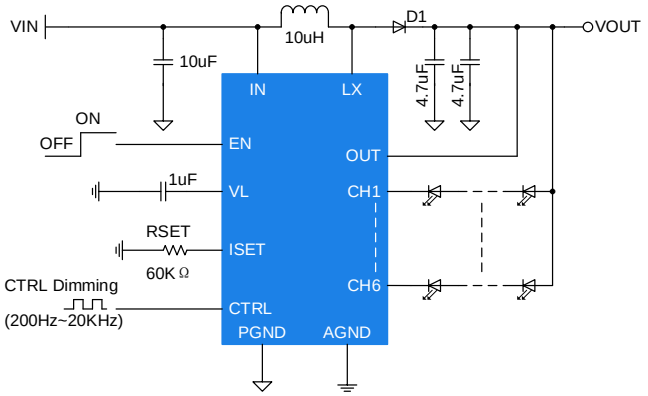
General Description

LP3352 is a cost-effective LED driver optimized for middle size TFT-LCD backlight application. LP3352 offers a high-efficiency current mode boost converter with integrated 2.5A/40V power MOS. The six integrated current sink can be adjusted through an external resistor. An unused LED channel can be disabled by connecting the channel to ground.

In addition, the LP3352 offers an external pulse-width-modulation (CTRL) method for LED dimming control. The LED current is turned on and off in response to the duty cycle and frequency applied at the CTRL pin.

The LP3352 features several protection functions including output over voltage protection (OVP), under-voltage lockout (UVLO), over temperature protection (OTP) and LED string open and short detection. The LP3352 is available in a space saving QFN-16 (0.5mm pitch) package.

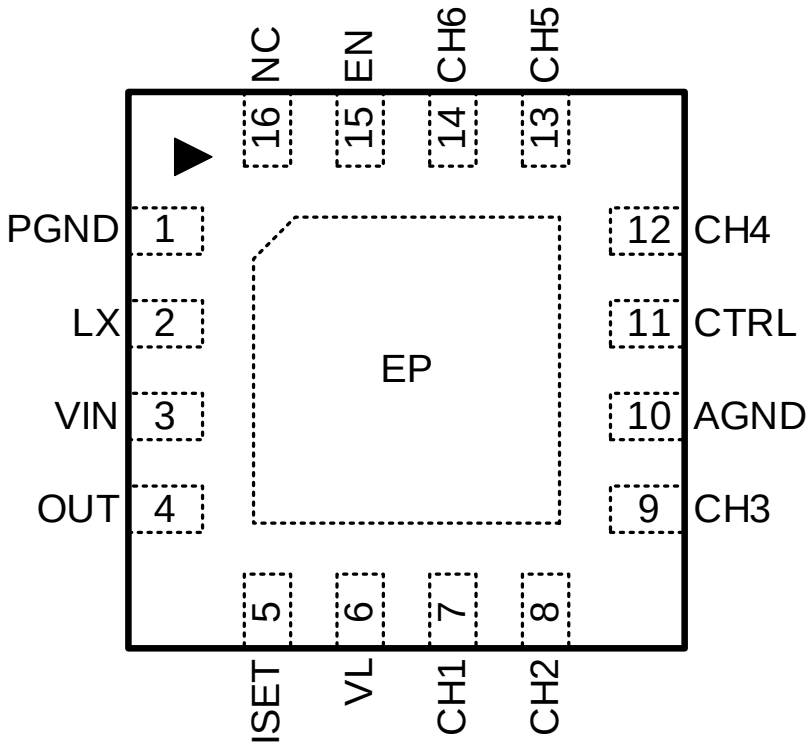
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP3352	LPS LP3352 YWXXX	MSL3	QFN3X3-16	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Configuratuon



LP3352QVF
QFN3X3-16 Package (Top View)

Pin Description

Pin#	Name	Description
1	PGND	Power Ground.
2	LX	Boost Regulator switching Node. Connect the inductor and the Schottky diode to LX.
3	IN	Input Supply Pin. Decouple with 10uF ceramic capacitor close to the pin.
4	OUT	Output voltage Sense Pin. Decouple with 10uF ceramic capacitor close to the pin.
5	ISET	LED Current set pin. Connect external resistor between this pin to GND.
6	VL	Regulator Output Pin. Connect a ceramic capacitor between VL and GND.
7	CH1	LED string current sink channel 1
8	CH2	LED string current sink channel 2
9	CH3	LED string current sink channel 3
10	AGND	Analog Ground.
11	CTRL	External PWM Dimming Control Pin.
12	CH4	LED string current sink channel 4
13	CH5	LED string current sink channel 5
14	CH6	LED string current sink channel 6
15	EN	Enable Pin.
16	NC	No Connection.
17	EP	Exposed thermal pad. Connect to AGND or PGND.

Absolute Maximum Ratings (Note1)

VIN to PGND ----------0.3V to +27V
CH1~CH6, LX, OUT to PGND----------0.3V to +40V
EN, CTRL to AGND ----------0.3V to +27V
VL, ISET to AGND---------- -0.3V to +7V
PGND,AGND to GND----------0.3V to +0.3V

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2KV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ----------150℃
Operating Junction Temperature Range (TJ)---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec)----------260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ----------88℃/W

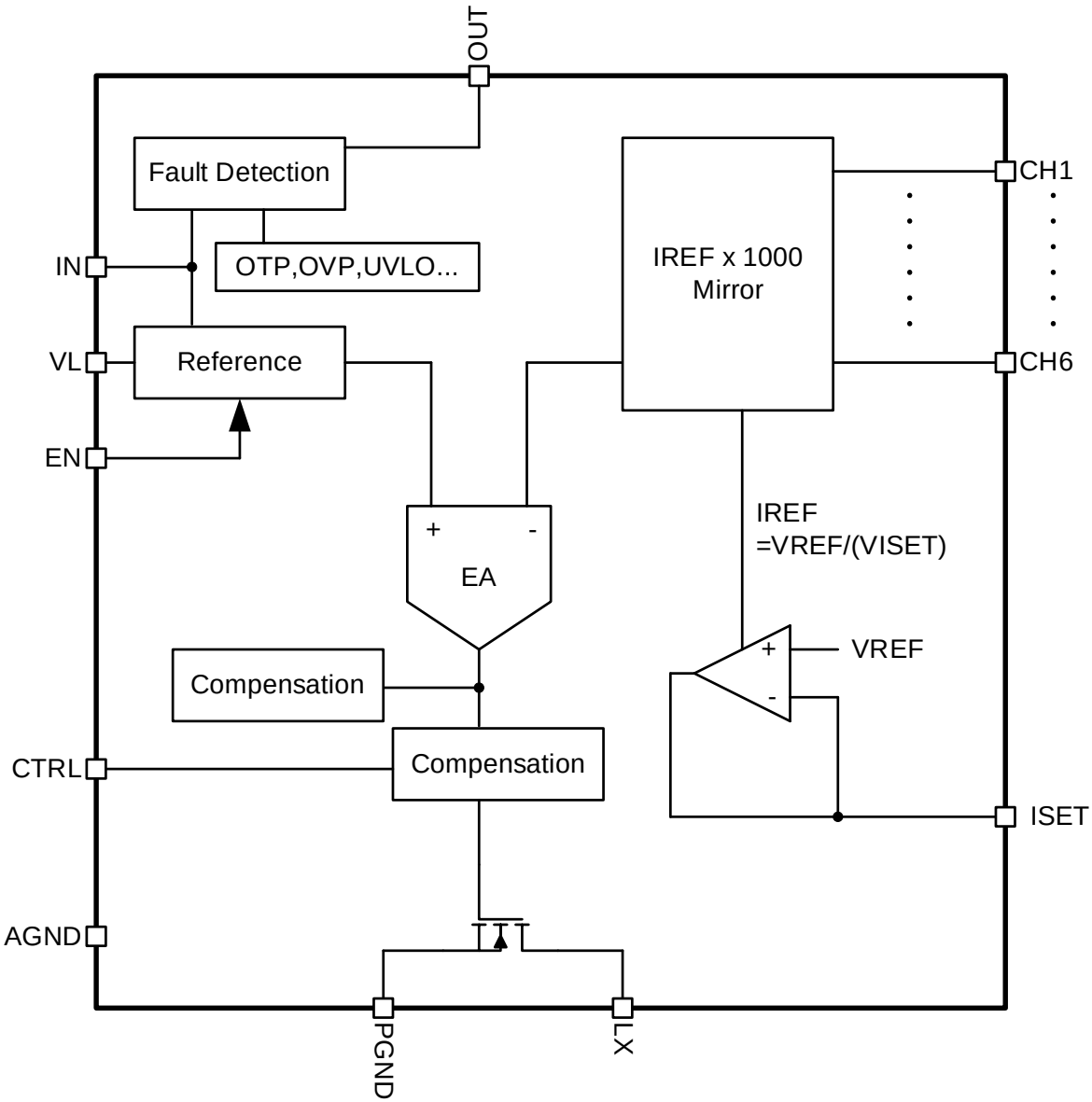
Electrical Characteristics

(Test Condition: V_{IN}=12V, T_A=25℃, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{IN}	Input Supply Voltage		2.7		24	V
I_Q	V_{IN} Quiescent Current	EN=L, CTRL=L		2.5	3	mA
I_{Q_OUT}	VOUT Input Current				30	uA
$V_{IN\_UVLO\_R}$	Input UVLO Threshold	V_{IN} Rising		2.6		V
$V_{IN\_UVLO\_F}$	UVLO Threshold Hysteresis	V_{IN} Falling Hysteresis		100		mV
T_{SS}	Current Soft Start Time			1		ms
T_{SD}	Thermal Shutdown Protection	Temperature Rising				℃
$\triangle T_{SD}$	Thermal Shutdown Protection Hysteresis					℃
Logic Control (EN, CTRL)						
VIH	EN/CTRL Threshold Voltage		1.5			V
VIL	EN/CTRL Threshold Voltage				0.4	V
I_{LC}	EN/CTRL Leakage Current	V_{EN}=V_{CTRL}=3V		15		uA
F_{DIM}	Dimming Frequency		100		30K	Hz
Boost Regulator						
F_{OSC}	Internal Oscillator Frequency		0.8	1.0	1.2	MHz
$R_{DS(ON)}$	Switch On Resistance			250	450	mΩ
I_{LEAK_LX}	LX Leakage current	EN=L, V_{LX}=35V			1	uA
D_{MAX}	Maximum Duty Cycle		85	93		%
D_{MIN}	Minimum Duty Cycle			70		ns
LED Current Rgulation						
	Minimum Regulation Voltage of CHx		600	700		mV
I_{LEAK_CHx}	CHx Leakage Current	EN=L,V_{CHx}=20V			3	uA
I_{LED_MAX}	CHx Maximum Current	V_{IN}>2.7V,CHx>0.7V	30			mA
V_{ISET}	ISET Voltage		1.204	1.229	1.253	V
K_{ISET}	ISET to ICHx Current Ratio	I_{SET}=20uA	970	1000	1030	A/A
I_{LED}	ICHx Current Accuracy	I_{SET}=20uA	19.4	20.0	20.6	mA
	ICHx Current Matching	(I_{MAX}-I_{MIN})/I_{AVG},I_{LED}=20mA		1	2.5	%
Protection Threshold						
V_{OVP}	VOUT Over Voltage Protection	VOUT OVP Threshold	38	39	40	V
V_{OVP_H}	VOUT Over Voltage Protection Hysteresis			1		V
V_{CH_OVP}	CHx Over Voltage Protection	CHx OVP Threshold	15	17	20	V

Note 3. The 40V rated Schottky diode and 50V rated output capacitor are recommended for the 39V(typ.) OVP threshold.
Note 4. The device is not guaranteed to function outside the test conditions.

Functional Block Diagram



Typical Application Circuit

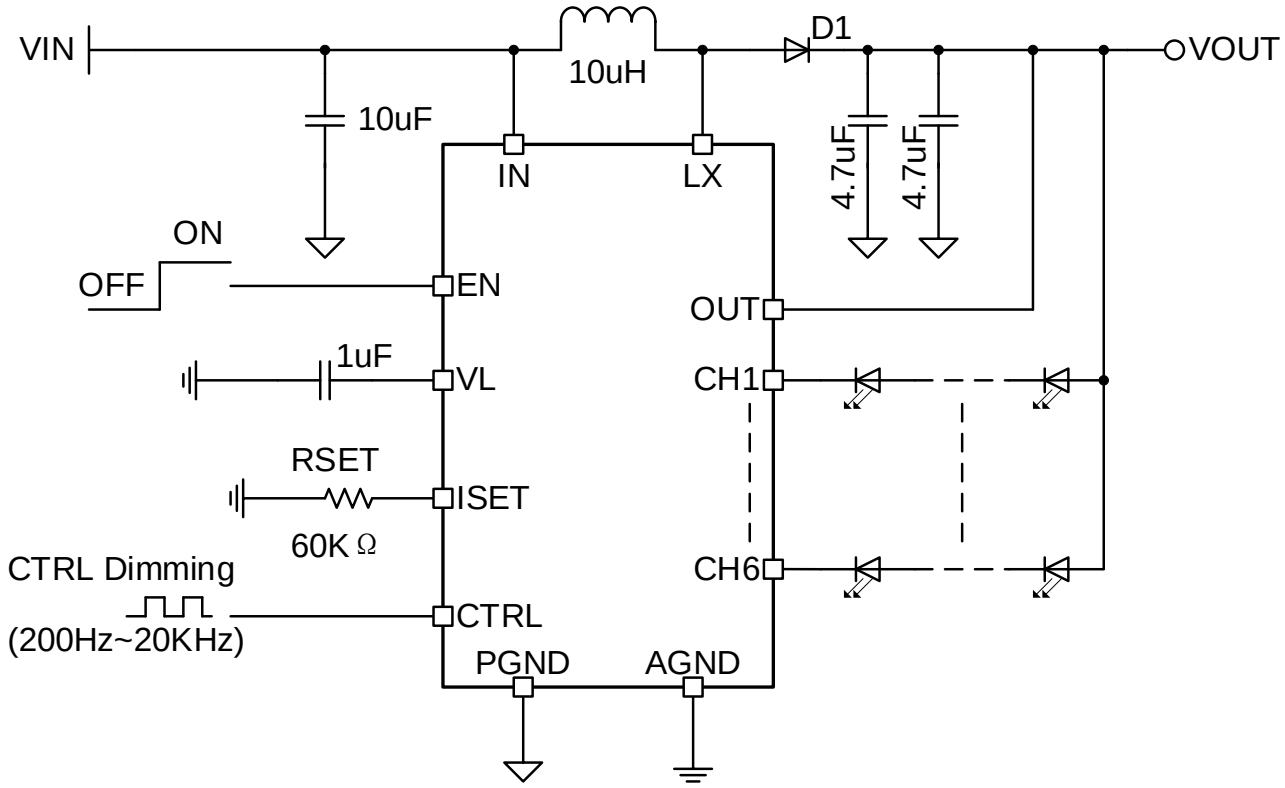
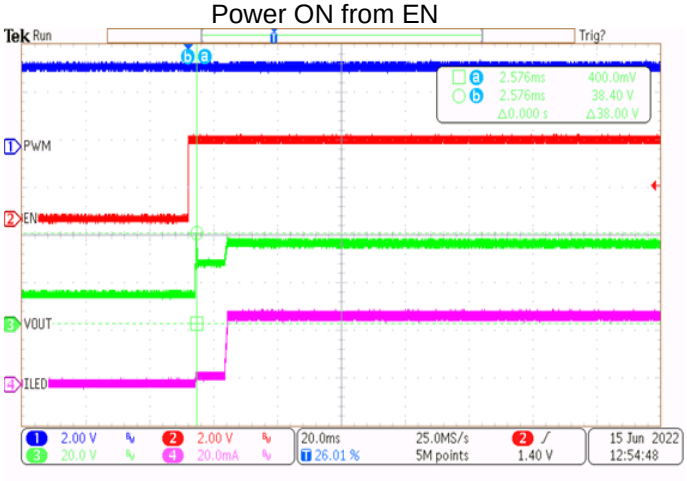


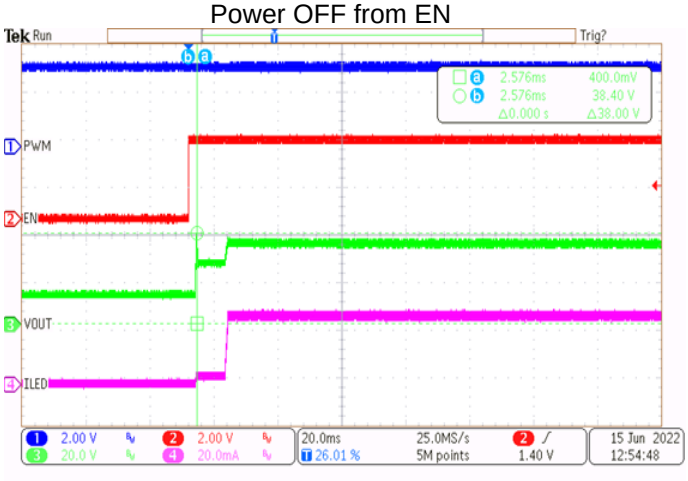
Figure 1 Typical Application

Typical Performance Characteristics

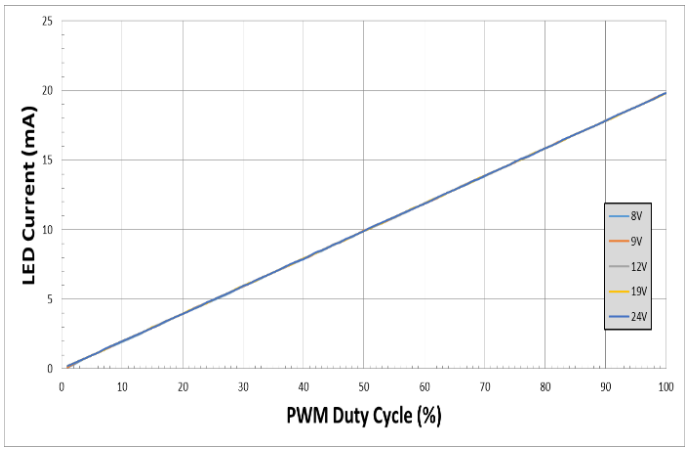
Power ON from EN



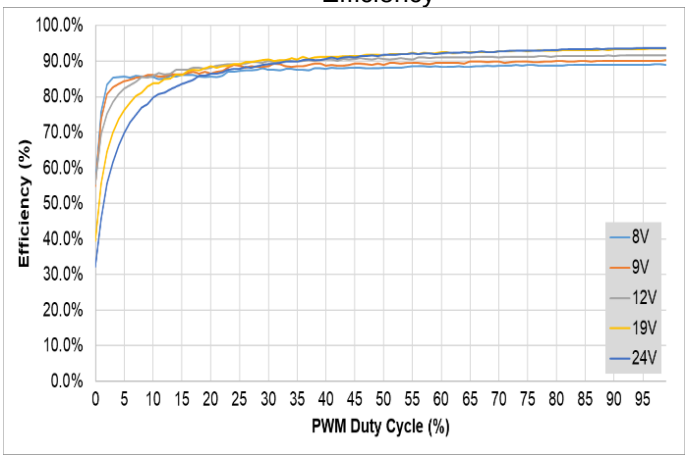
Power OFF from EN

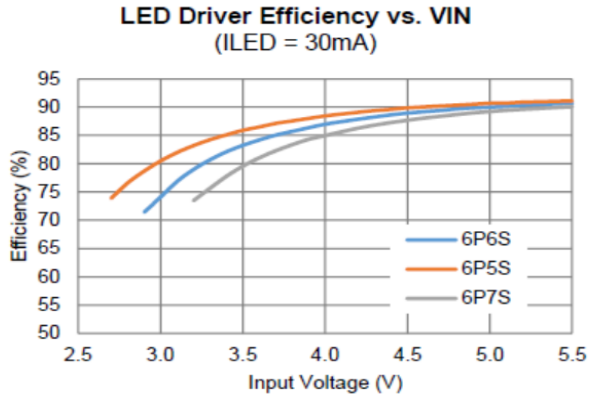


Current Linearity



Efficiency





Power On/Off Sequence

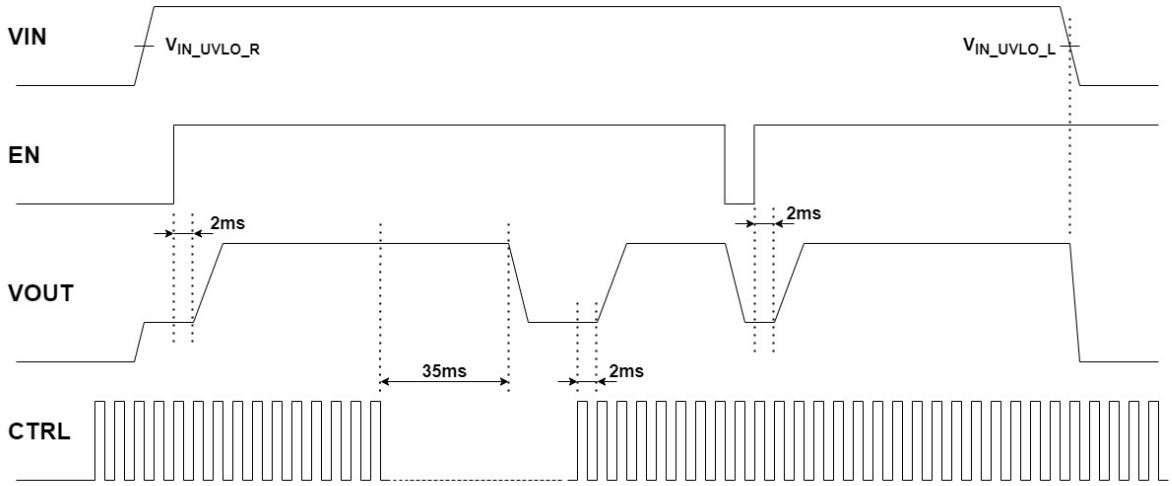


Figure 2. Recommended Power on/off sequence

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The feedback to the boost loop controller is taken from the CHx pins. The numbers of LEDs that can be driven by LP3352 depends on the type of LED chosen in the application. The LP3352 is capable of boosting up to 40V and capable to drive 10 white LEDs in series for each of the 6 channels, enabling a total of 60 pieces of the 3.6V/30mA type of LEDs.

Program LED Current

The brightness should be set by choosing a RSET resistor that sets the LED maximum current as:

$$I_{LED} = \frac{1.229V}{R_{SET}} * 1000$$

Brightness Control

Digital PWM control signal to CTRL pin makes LED current follows the control signal duty.
The average LED current can be calculated as:

$$I_{LED\ (\ AVERAGE\ )} = \frac{1.229V}{R_{SET}} * 1000 * D$$

where D denotes to the duty of digital control signal.
The table list below represents the relation between the frequency and duty of the digital PWM control signal.

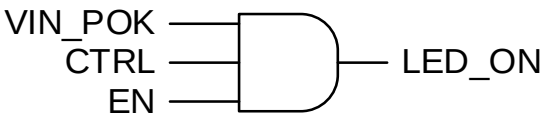
DIM F_{CTRL}(Hz)	D_{MIN}	D_{MAX}
100<F_{CTRL}≦200	0.1%	100%
200<F_{CTRL}≦500	0.25%	100%
500<F_{CTRL}≦1K	0.5%	100%
1K<F_{CTRL}≦2K	1%	100%
2K<F_{CTRL}≦5K	2.5%	100%
5K<F_{CTRL}≦10K	5%	100%
10K<F_{CTRL}≦20K	10%	100%
20K<F_{CTRL}≦30K	15%	100%

Over Voltage Protection

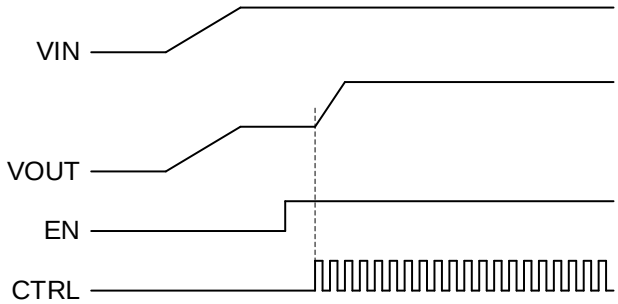
Once all the LED arrays are opened, the CHx feedback will be 0V. It makes the boost output to rise to over voltage threshold (39V typical). The IC will shut down and remains off until there is VIN POR toggling.

LED Control Sequence

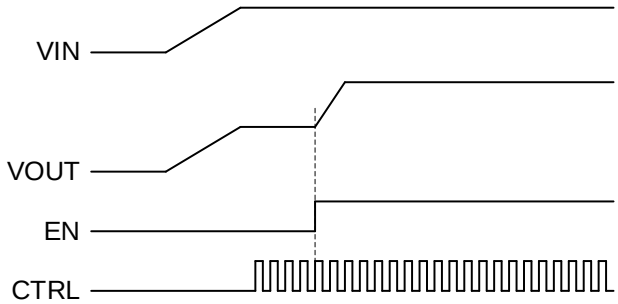
When VIN beyond their UVLO threshold, the control circuit will be ready for CTRL pin and EN pin input control. Only CTRL ="1" and EN="1" powers up the VOUT and the current driver starts to regulate LED current. A simple logic diagram is shown below:



Hence, even VIN ready, the control circuit still waiting for the last arrive of CTRL and EN:

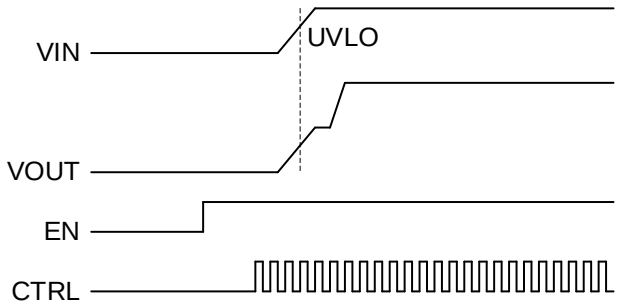


EN prior than CTRL signal



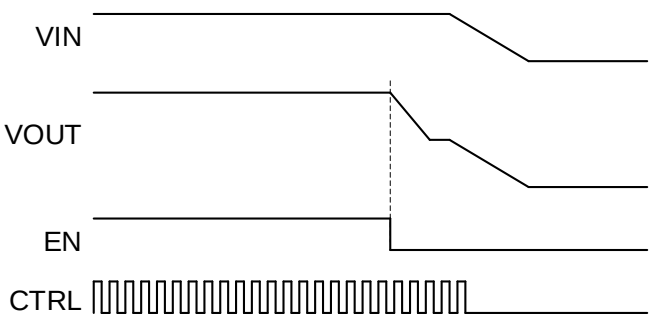
CTRL prior than EN signal

If CTRL and EN control from system are ready before input power supply(VIN), the control circuit will start to turn on LED driver after the input power established:

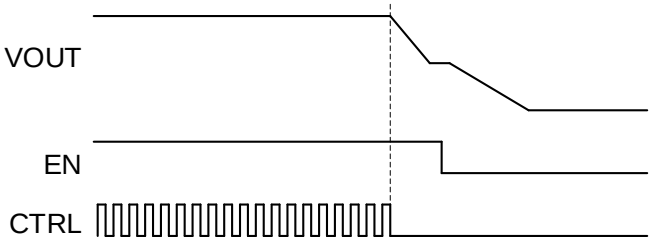


EN/CTRL prior than VIN

It turns off the LED either the CTRL pin or EN pin set to ″0″:

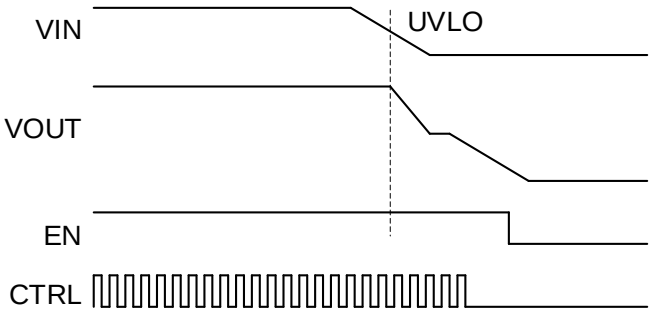


EN prior than CTRL signal



CTRL prior than EN signal

Or the input power supply lost before the control signal (CTRL and EN) inactivate the LED driver:



VIN turn off prior than EN/CTRL

Open LED Protection(OLP)

Once the CHx pin is opened, the voltage on CHx will drop to zero. It will be detected and disabled of CHx feedback until the LED load is closed again.

Over And Short Circuit Protection

The LP3352 has cycle by cycle over-current protection of 2.5A (Typical). The PWM switch turns off when the inductor current reaches the over-current protection threshold. The PWM switch remains off until the beginning of the next switching cycle. When there is sustained over-current condition that makes VOUT far lower the voltage that LED regulated current needed for more than 12ms, the IC would turn off and require VIN POR or the EN pin toggling to restart.

Over Temperature Protection

The LP3352 has over temperature protection function to prevent the excessive power dissipation from overheating. OTP shut down the switching regulator if the junction temperature exceeds 150°C. And it will start switching again after the junction temperature cool down 20°C.

Layout Consideration

The proper PCB layout and component placement are critical for all circuit. The careful attention is needed to prevent electromagnetic interference (EMI) problems. Here are some suggestions to the layout of LP3352 design.

1. Connected all ground together with one uninterrupted ground plane with at least two vias.
2. The input capacitor should be located as closed as possible to the VIN and ground plane.
3. Minimize the distance of all traces connected to the LX node, that the traces short and wide route to obtain optimum efficiency.
4. All output capacitors must be closed to ground plane. The ground terminal of COUT must be located as closed as possible to ground plane.
5. Radiated noise can be decreased by choosing a shielded inductor.

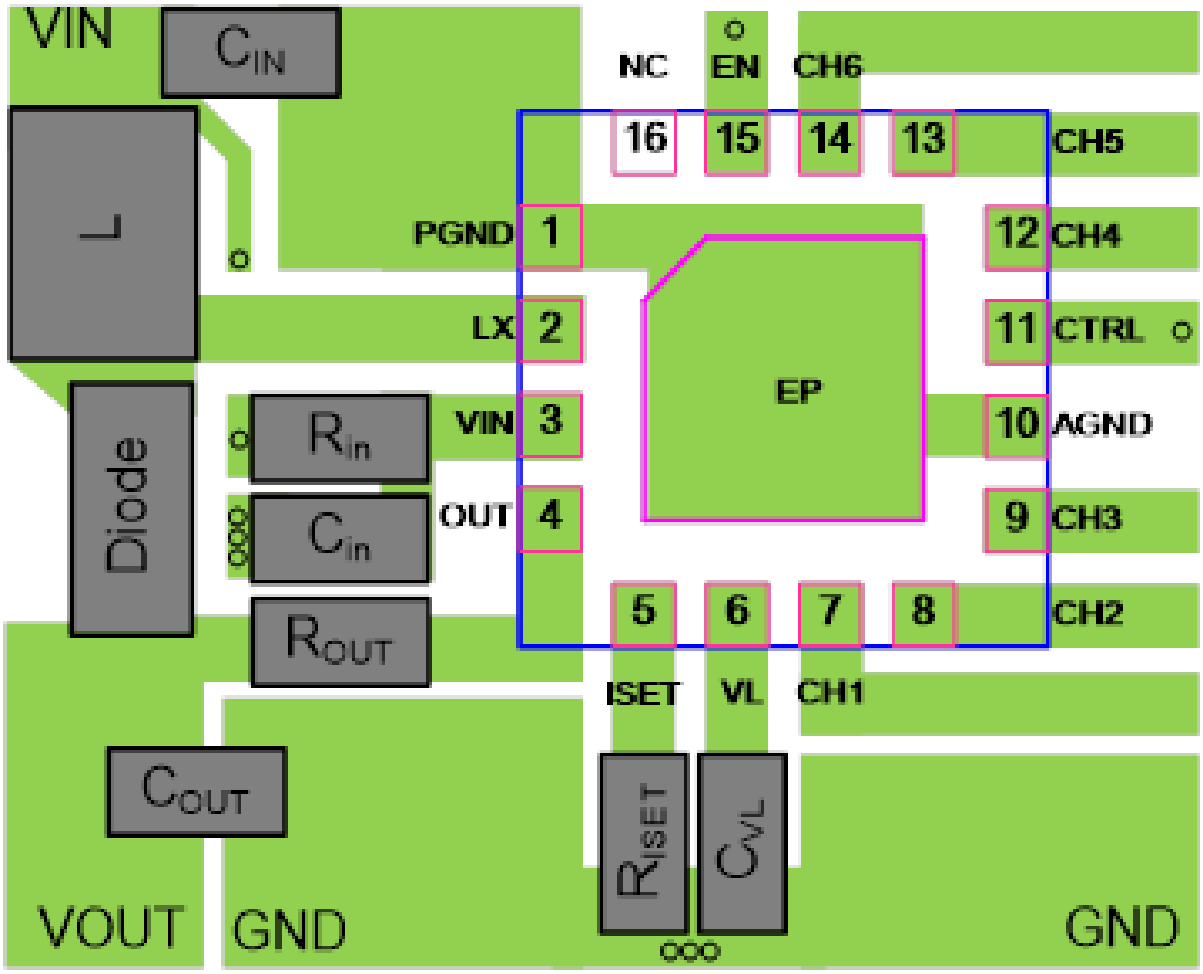
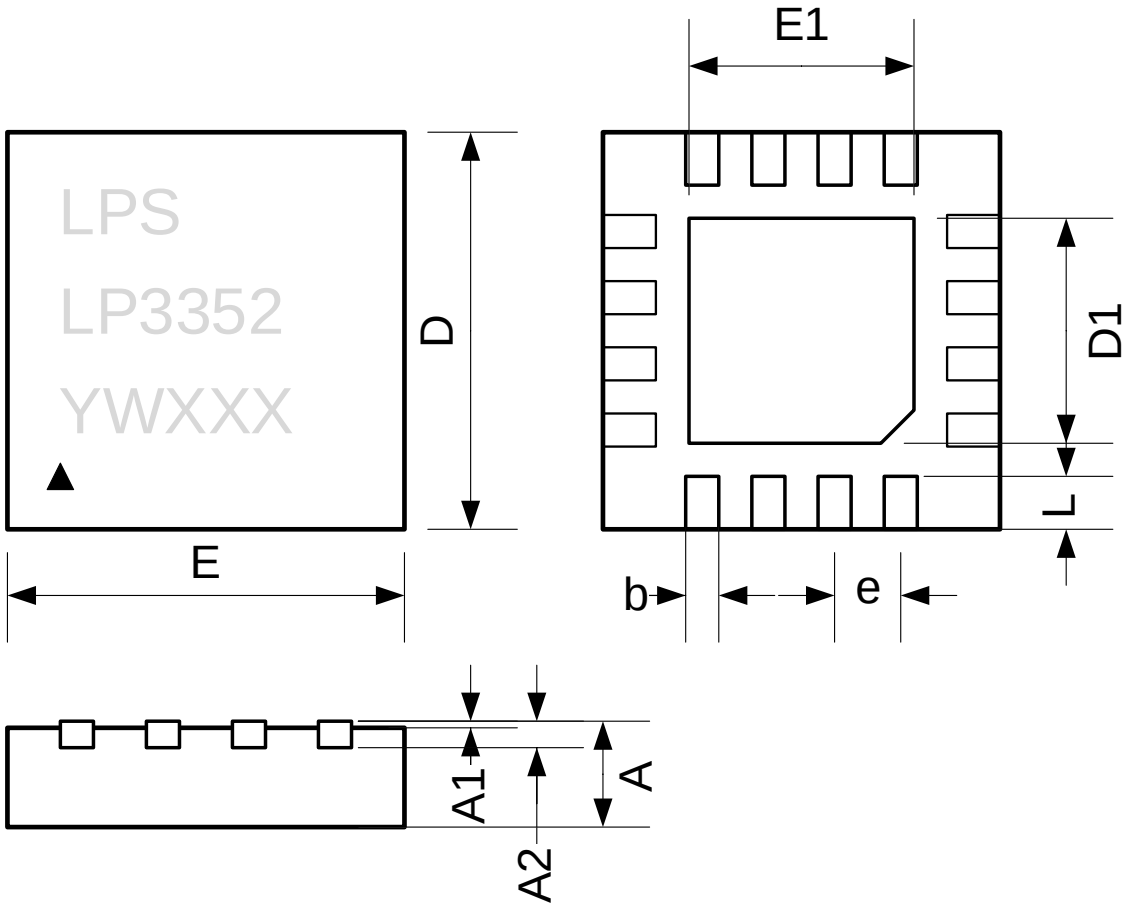


Figure 3. Recommended PCB Layout

Packaging Information

QFN3X3-16



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	1.60	1.70	1.80	0.0630	0.0669	0.0689
E1	1.60	1.70	1.80	0.0630	0.0669	0.0689
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min(T_{SMIN}) Temperature Max(T_{SMAX}) Time(T_S) from (T_{SMIN} to T_{SMAX})	 100°C 150°C 60~120 seconds	 150°C 200°C 60~120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max	3°C/second max
Liquidous temperature(T_L) Time(t_L) maintained above T_L	183°C 60~150 seconds	217°C 60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed theClassification temp in Table 1. For suppliers T_P must equal or exceedthe Classification temp in Table 1.	For users T_P must not exceed theClassification temp in Table 2. For suppliers T_P must equal or exceedthe Classification temp in Table 2.
Time(t_P)* within 5°C of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6°C/second max	6°C/second max
Time 25°C to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

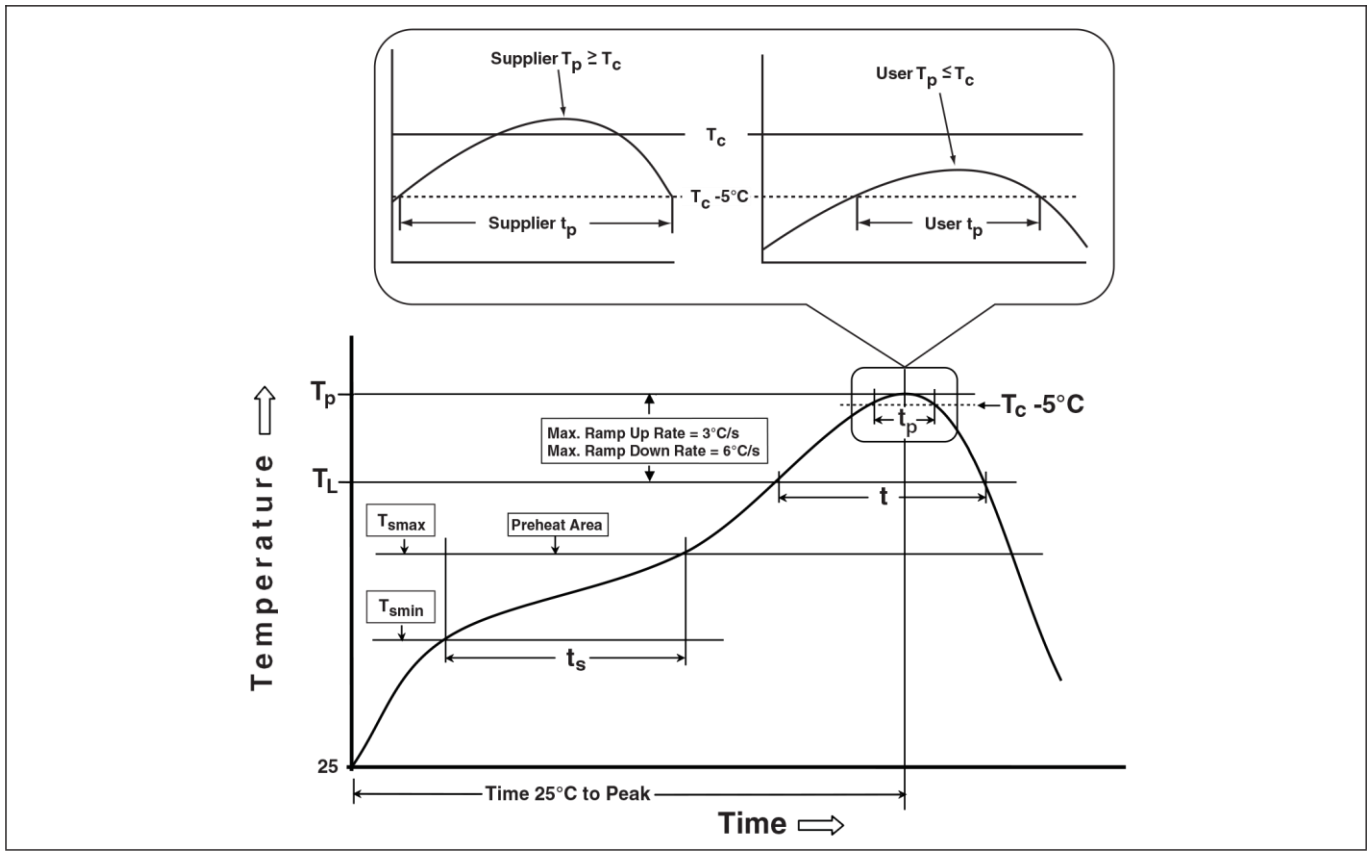


Figure1 Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）