LP3982S

75dB High PSRR 42μV Low Noise LDO

Features

- Wide Input Voltage Range: 2.2V to 5.5V
- Fixed Output Voltage: 1.2V, 1.8V, 2.8V, 3.3V
- Maximum Load Current: 300mA
- High PSRR at Full Frequency Range:
  - 75dB@1kHz
  - 60dB@10kHz
  - 50dB@100kHz
- Low Noise: 42μVrms, V_{OUT}=2.8V
- Low Quiescent Current: 58μA typical
- Low Dropout Voltage:
  - 66mV @ 100mA Load, V_{OUT}=2.8V
  - 200mV @ 300mA Load, V_{OUT}=2.8V
- Output Voltage Accuracy: ±1% @ 1mA
- Short Circuit Current Limit: 110mA
- Thermal Shutdown Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.01%/V typical
- Load Regulation: 16mV typical
- Robust ESD capability:
  - Human Body Model: 4kV
  - Charged Device Model: 1kV
- Package: SOT23-5, DFN-4
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Digital cameras
- Audio devices
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Post regulation
- Wireless handsets

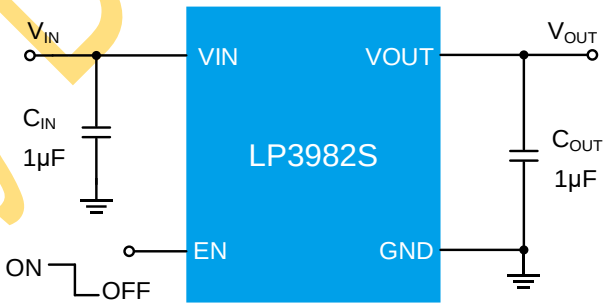
General Description

The LP3982S family are high performance low dropout (LDO) voltage regulators with high PSRR, fast transient response, high accuracy, and low output noise. The devices with advanced CMOS process are suitable for many applications that require regulated supplies of up to 300mA load current.

The family include standard fixed output voltages of 1.2V, 1.8V, 2.8V, and 3.3V. The devices are stable with a 1.0μF~10μF ceramic output capacitor. The devices are protected from short circuit by a current limit function and from over-heating by a thermal overload protection.

The devices are available in standard DFN-4 (1mmx1mm) and SOT23-5 packages.

Typical Application Circuit



Order Information

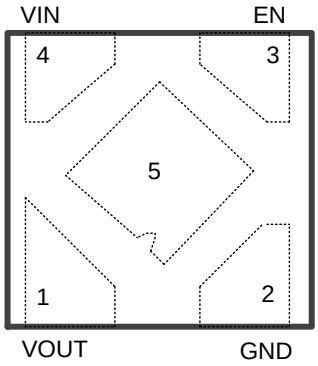
LP3982S □□□□ □

- F: Pb Free
- Package Type
  - B5: SOT23-5
  - QV: DFN-4
- OUT Voltage
  - 12: 1.2V
  - 18: 1.8V
  - 28: 2.8V
  - 33: 3.3V

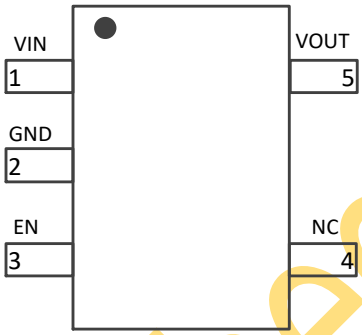
Device Information

Part Number	Top Marking	OUT Voltage	Moisture Sensitivity Level	Package	Shipping
LP3982S-12B5F	LPS GBYWX	1.2V	MSL3	SOT23-5	3K/REEL
LP3982S-18B5F	LPS GCYWX	1.8V	MSL3	SOT23-5	3K/REEL
LP3982S-28B5F	LPS GHYWX	2.8V	MSL3	SOT23-5	3K/REEL
LP3982S-33B5F	LPS GEYWX	3.3V	MSL3	SOT23-5	3K/REEL
LP3982S-12QVF	GBW	1.2V	MSL3	DFN-4	12K/REEL
LP3982S-18QVF	GCW	1.8V	MSL3	DFN-4	12K/REEL
LP3982S-28QVF	GHW	2.8V	MSL3	DFN-4	12K/REEL
LP3982S-33QVF	GEW	3.3V	MSL3	DFN-4	12K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

Pin Diagram



DFN-4（top view）

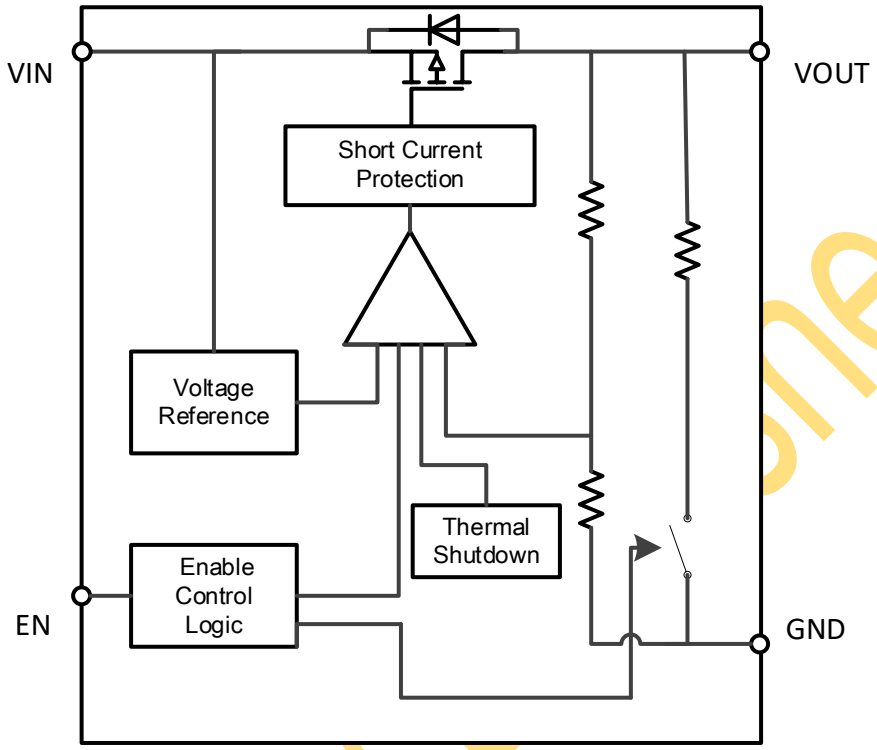


SOT23-5（top view）

Pin Description

Pin		Name	Description
DFN-4	SOT23-5		
1	5	VOUT	Output pin. Bypass with a 1μF or greater ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.
2	2	GND	Ground.
3	3	EN	Enable pin. Active high. Driving EN over 1V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode.
4	1	VIN	Supply input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor. Place the capacitor as close as to the pin as possible.
	4	NC	No connection.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN Pin to GND ---------- -0.3~6.5V
- VOUT, EN Pin to GND ---------- -0.3~VIN
- Maximum Junction Temperature (T_J) ---------- 150℃
- Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃
- Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

- HBM (Human Body Model) ---------- 4kV
- CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions

- Input Voltage ---------- 2.2V to 5.5V
- Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
- Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, unless otherwise noted.)

Symbol	Parameter	Condition		Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT							
V_{IN}	Input Voltage Operation Range			2.2		5.5	V
I_{Inrush}	Inrush Current	C_{OUT}=10μF			400		mA
I_Q	DC Supply Quiescent Current	LP3982S-28B5F, I_{OUT}=0mA			58		μA
I_{SD}	Shutdown Current	LP3982S-28B5F, V_{EN}=0V			0.6		μA
REGULATED OUTPUT							
V_{OUT}	Output Voltage Accuracy	I_{OUT}=1mA		1.18	1.2	1.22	V
				1.78	1.8	1.82	
				2.772	2.8	2.828	
				3.267	3.3	3.333	
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	Output Voltage Line Regulation	V_{IN}=V_{OUT}+0.5V~5.5V I_{OUT}=1mA			0.01		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{OUT} from 1mA to 300mA			16	28	mV
T_{CVOUT}	V_{OUT} Temperature Coefficient	I_{OUT}=1mA			0.01		%/℃
I_{OUT_MAX}	Max Load Current	V_{EN}=V_{IN}		300			mA
I_{LIMIT}	Load Current Limit	V_{EN}=V_{IN}		400	550		mA
I_{SHORT}	Short Current	V_{EN}=V_{IN} V_{OUT} short to GND			110		mA
V_{DROP}	Dropout Voltage	V_{OUT}=1.8V, I_{OUT}=300mA			320		mV
		V_{OUT}=2.8V, I_{OUT}=300mA			200		
		V_{OUT}=3.3V, I_{OUT}=300mA			180		
PSRR	Power Supply Rejection Ratio	V_{IN}=(V_{OUT}+1V)$_{DC}$ +0.2V_{P-P}, I_{OUT}=20mA, V_{OUT}=2.8V	f=100Hz		80		dB
			f=1kHz		75		
			f=10kHz		60		
			f=100kHz		50		
e_N	Output Noise	10Hz~100kHz I_{OUT}=20mA	V_{OUT}=1.2V		29		μV_{RMS}
			V_{OUT}=1.8V		45		
			V_{OUT}=2.8V		42		
			V_{OUT}=3.3V		48		

THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			160		℃
ΔT_{SD}	Thermal Shutdown Hysteresis			20		℃
SOFTSTART AND DISCHARGE						
t_{rise}	V_{OUT} Rise Time	I_{OUT}=0mA		30		μs
R_{DISC}	Auto-discharge On-Resistance			850		Ω
EN PIN						
V_{ENH}	EN Logic High Voltage		1.0			V
V_{ENL}	EN Logic Low Voltage				0.4	V
I_{EN}	EN Input Current	V_{EN}=0 to 5.5V		120		nA

Typical Characteristics

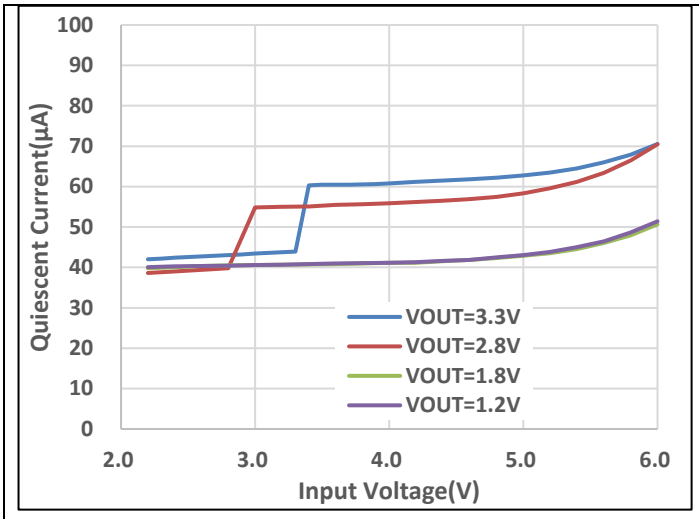


Figure 1. Quiescent current vs input voltage, 25℃

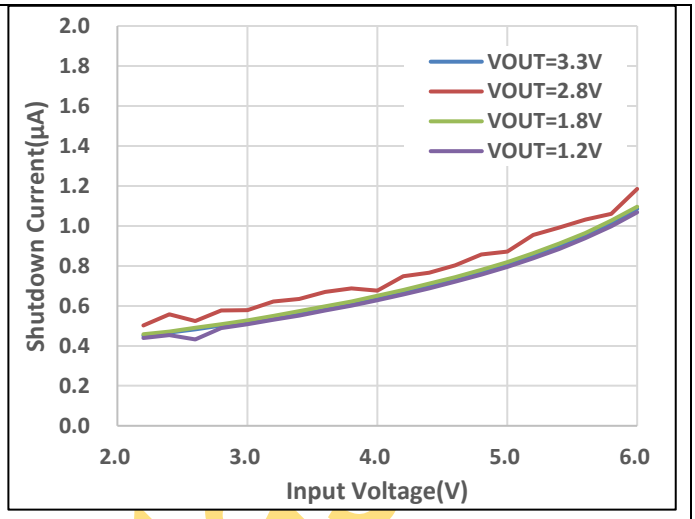


Figure 2. Shutdown current vs input voltage, 25℃

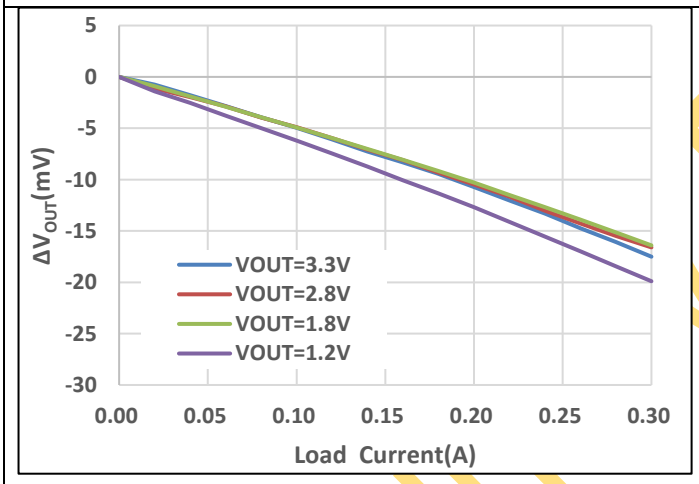


Figure 3. ΔV_{OUT} vs load current, $V_{IN}=V_{OUT}+1V$, 25℃

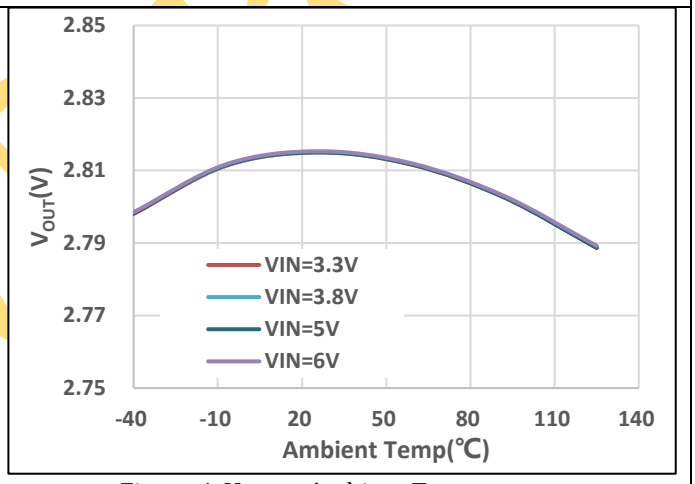


Figure 4. V_{OUT} vs Ambient Temperature, LP3982S-28B5F, I_{OUT}=1mA

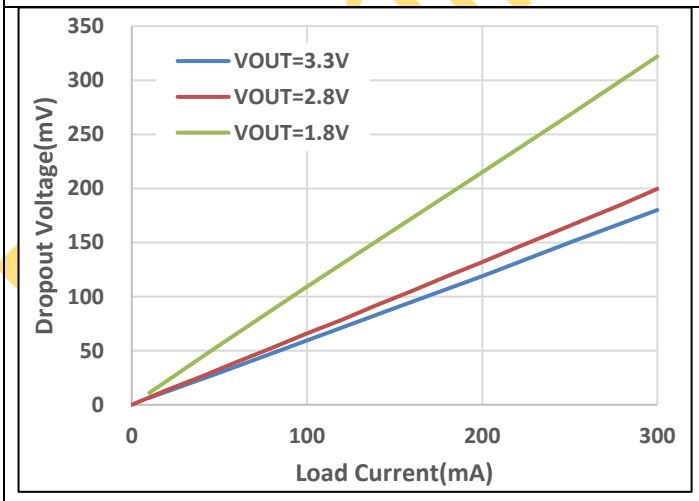


Figure 5. Dropout Voltage vs Load Current, 25℃

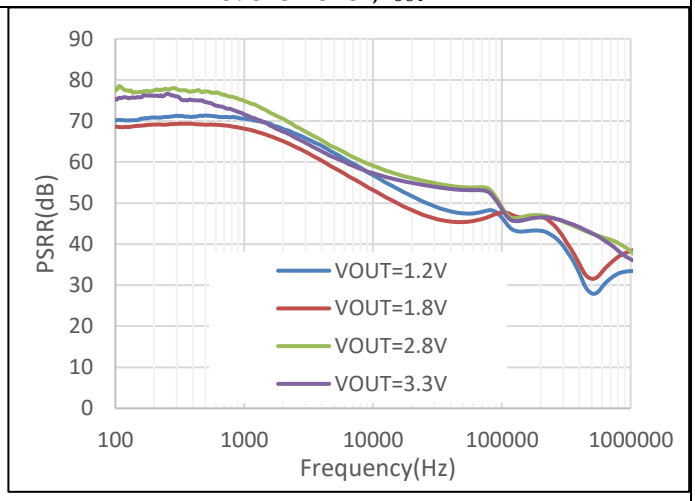


Figure 6. PSRR vs Frequency, I_{OUT}=20mA, $V_{IN}=V_{OUT}+1V$, 25℃

Load Transient: I_{OUT}=1mA <->300mA in 1µs

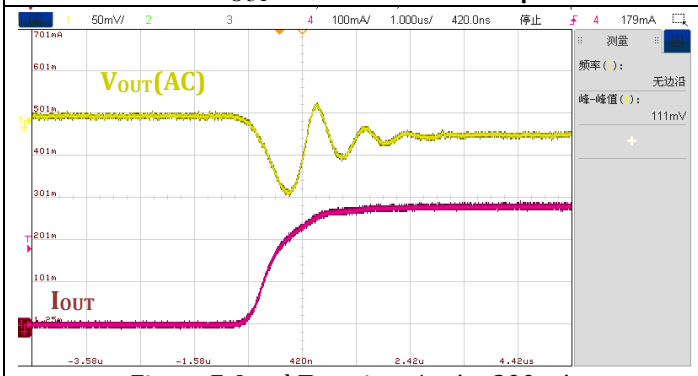


Figure 7. Load Transient 1mA->300mA, V_{IN}=3.3V, V_{OUT}=1.2V

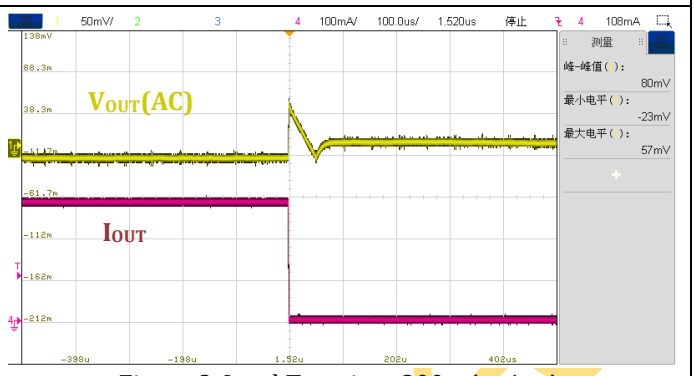


Figure 8. Load Transient 300mA->1mA, V_{IN}=3.3V, V_{OUT}=1.2V

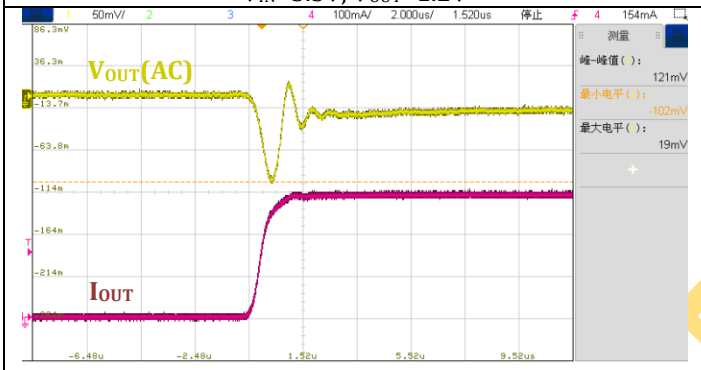


Figure 9. Load Transient 1mA->300mA, V_{IN}=3.3V, V_{OUT}=1.8V

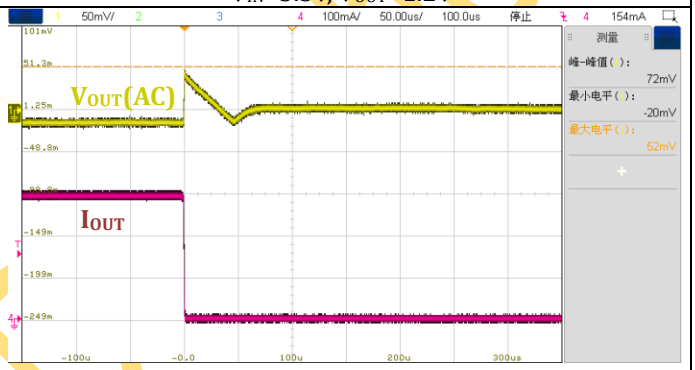


Figure 10. Load Transient 300mA->1mA, V_{IN}=3.3V, V_{OUT}=1.8V

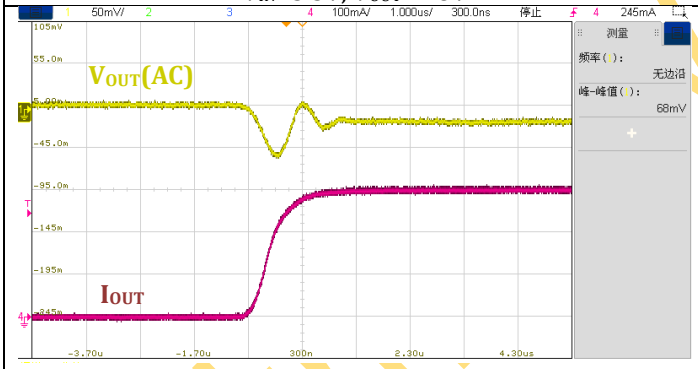


Figure 11. Load Transient 1mA->300mA, V_{IN}=3.8V, V_{OUT}=2.8V

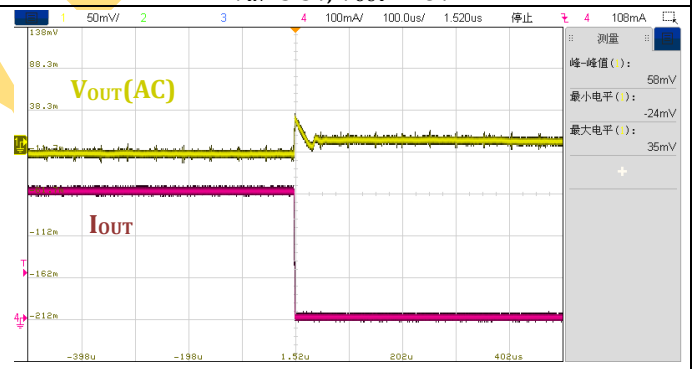


Figure 12. Load Transient 300mA->1mA, V_{IN}=3.8V, V_{OUT}=2.8V

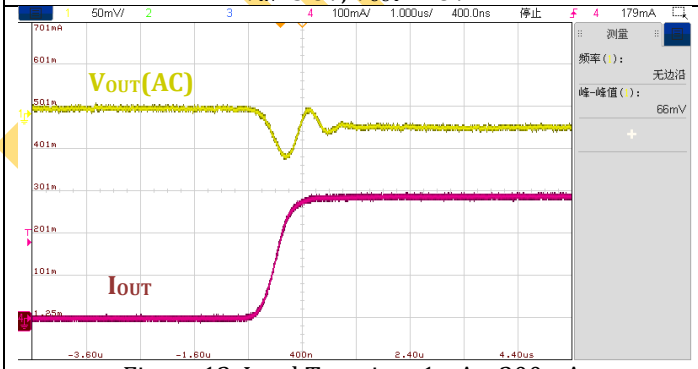


Figure 13. Load Transient 1mA->300mA, V_{IN}=4.3V, V_{OUT}=3.3V

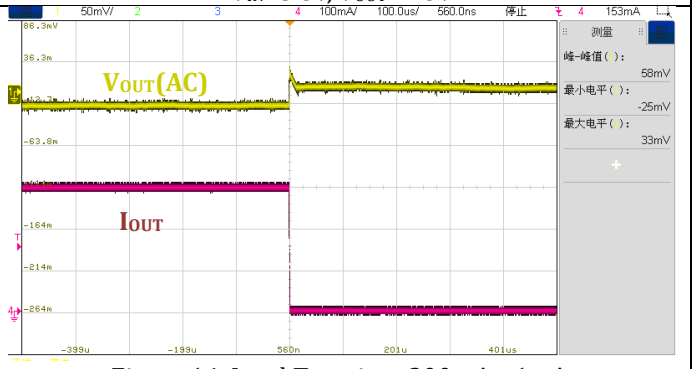


Figure 14. Load Transient 300mA->1mA, V_{IN}=4.3V, V_{OUT}=3.3V

Line Transient: V_{IN}=V_{OUT}+1V<->V_{OUT}+2V in 10μs

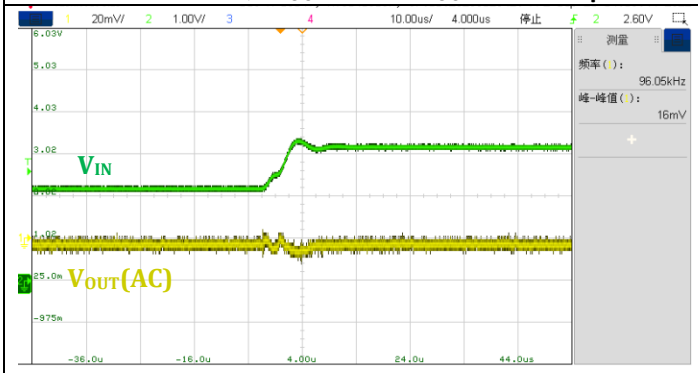


Figure 15. Line Transient V_{IN}=2.2V->3.2V, V_{OUT}=1.2V, I_{OUT}=100mA

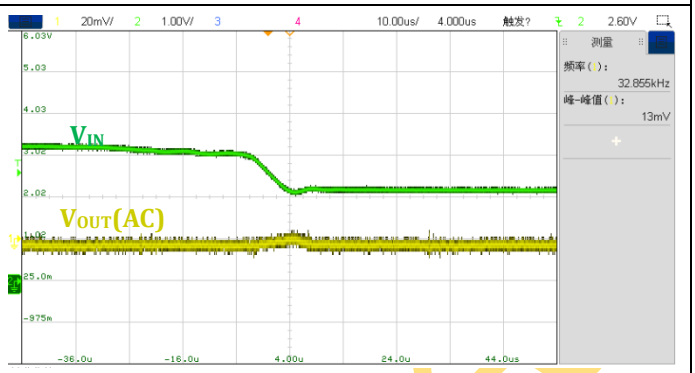


Figure 16. Line Transient V_{IN}=3.2V->2.2V, V_{OUT}=1.2V, I_{OUT}=100mA

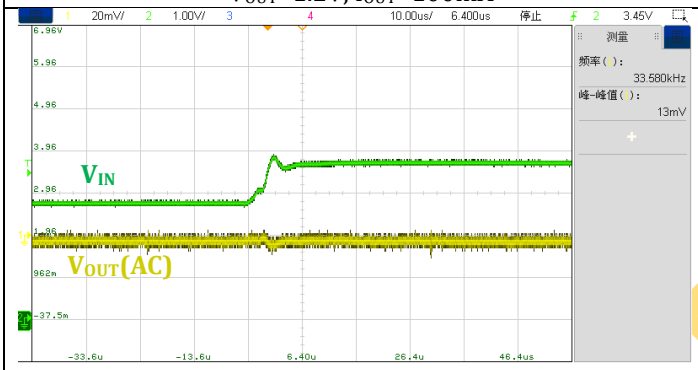


Figure 17. Line Transient V_{IN}=2.8V->3.8V, V_{OUT}=1.8V, I_{OUT}=100mA

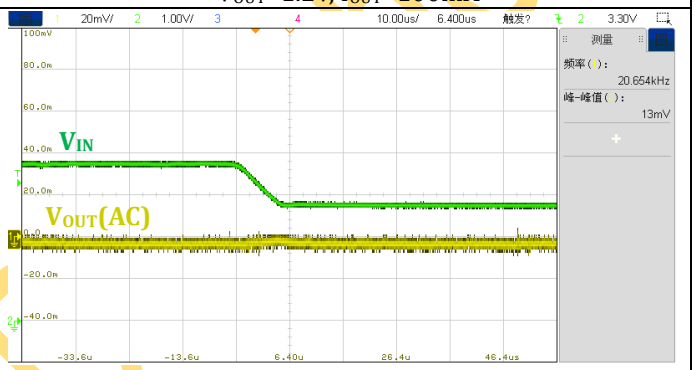


Figure 18. Line Transient V_{IN}=3.8V->2.8V, V_{OUT}=1.8V, I_{OUT}=100mA

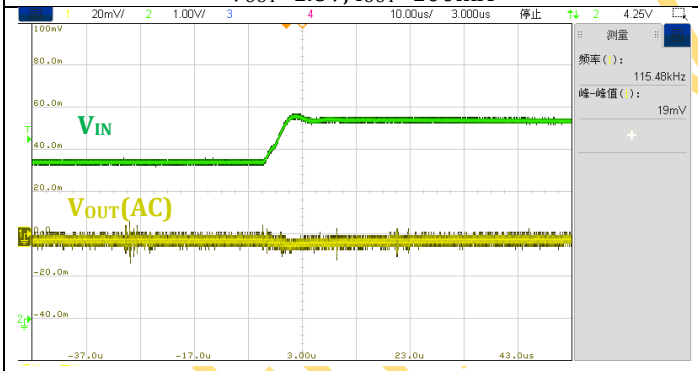


Figure 19. Line Transient V_{IN}=3.8V->4.8V, V_{OUT}=2.8V, I_{OUT}=100mA

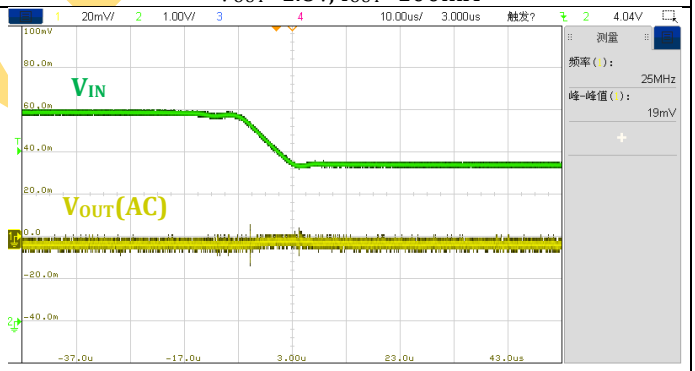


Figure 20. Line Transient V_{IN}=4.8V->3.8V, V_{OUT}=2.8V, I_{OUT}=100mA

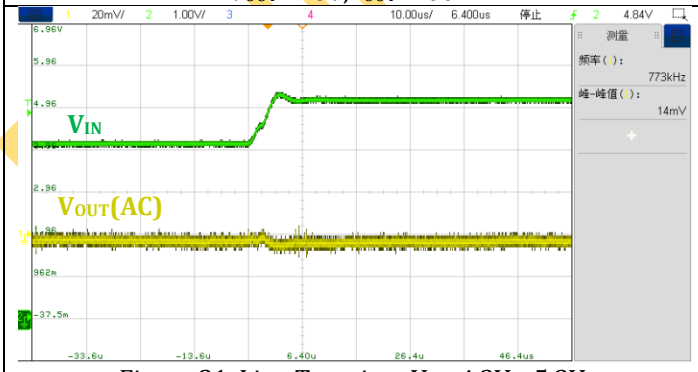


Figure 21. Line Transient V_{IN}=4.3V->5.3V, V_{OUT}=3.3V, I_{OUT}=100mA

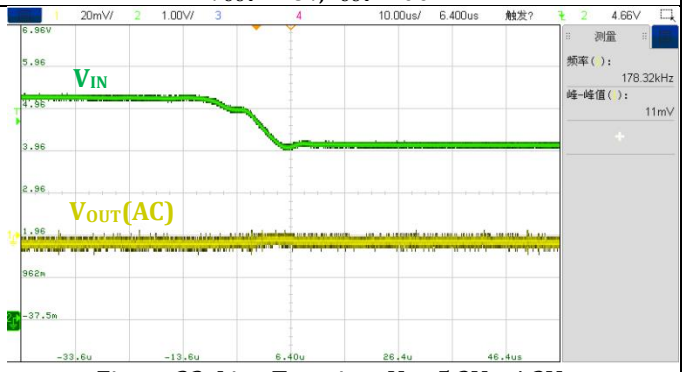


Figure 22. Line Transient V_{IN}=5.3V->4.3V, V_{OUT}=3.3V, I_{OUT}=100mA

Detailed Description

Overview

The LP3982S family are high performance, low dropout linear regulators with fixed 1.2V, 1.8V, 2.8V, and 3.3V output voltages. The family with low output noise and high PSRR are suited for high performance applications. Optimized for using with ceramic capacitors, the device provides excellent transient performance.

Internally, the devices consist of a voltage reference, an enable control logic, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares a reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

Enable Function

The EN pin is an active high logic input pin. The internal power element is turned off when EN pin is tied low. When the EN pin is pulled high, the LP3982S will be activated and output voltage according to the setting.

Auto Discharge

The LP3982S family have a quick discharge function. When the device is disabled by the pulled-down EN pin, a discharge resistor is connected between OUT and GND. The resistance is 850Ω typically.

Short Current Limit Protection

When the output current at the VOUT pin is higher than current limit threshold or the VOUT pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 110mA to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

When the internal junction temperature of LP3982 family devices exceed the junction thermal shutdown threshold (160℃ typical), the devices will shut down the output, after the junction temperature falls below 140℃ , the VOUT voltage will resume.

Application Description

Thermal Consideration

The reason that causes thermal shutdown protection of an LP3982S device is the power dissipation. Nearly all of the power dissipation is generated by the internal PMOS pass device. The power dissipation can be calculated approximately as,

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

where P_D is the power dissipation.

The worst-case situation is when the device has the maximum input voltage of 5.5V and the maximum load current of 300mA. In this situation, the device dissipates the maximum power,

$$P_{Dmax} = (5.5V - 1.2V) \times 300mA = 1.29W$$

This power dissipation of the LDO device in the SOT23-5 or DFN-4 package will trigger thermal shutdown protection at high ambient temperature. Then a trade-off must be made between the output current, cost, and thermal requirements of the application.

Input Capacitor

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. A 1μF-10uF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitches and noise. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

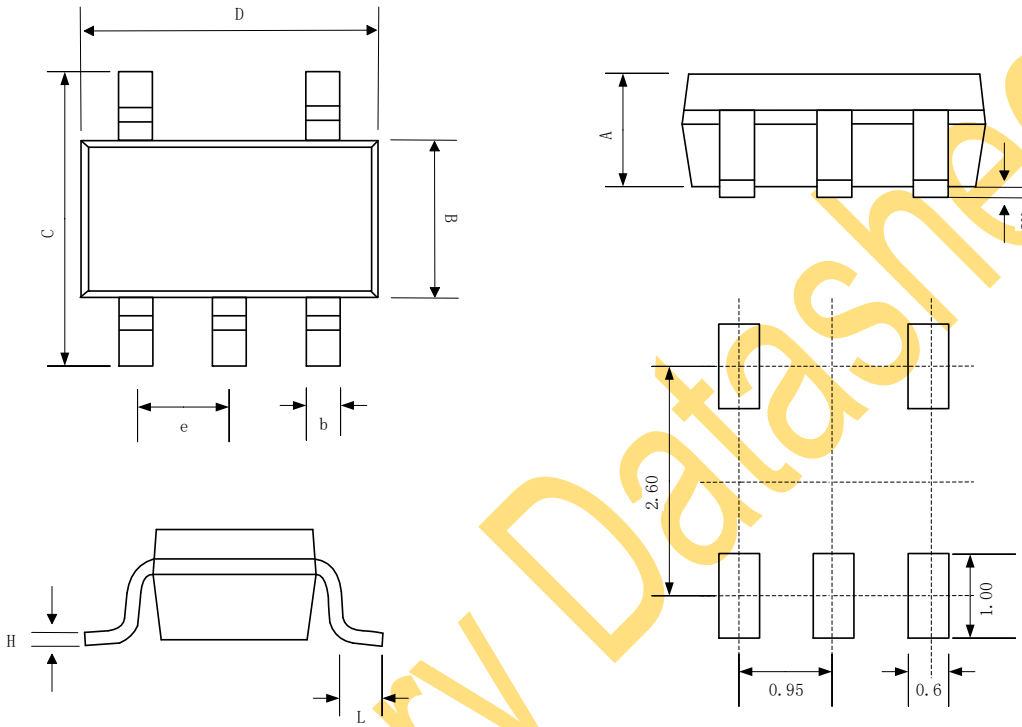
The LP3982S devices require a minimum output capacitance of 1 μF for output voltage stability. The recommended output capacitance is from 1μF to 10μF, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as practically possible.

Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practically possible to the respective LDO pins. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible with a wide and component-side copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device.

Packaging Information

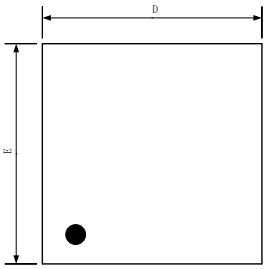
SOT23-5



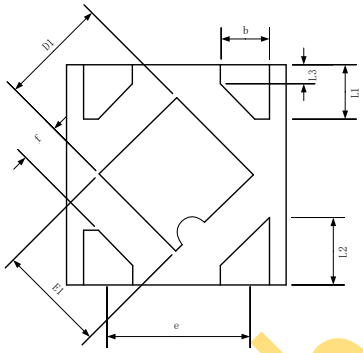
Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

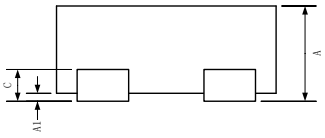
DFN-4



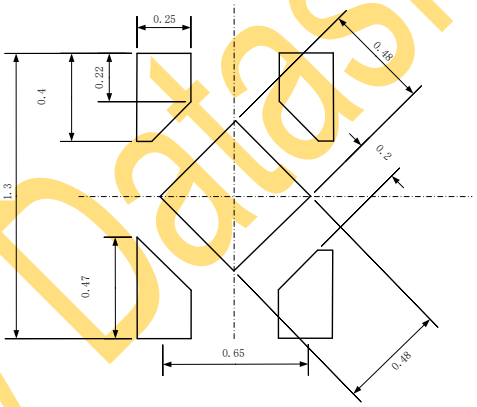
TOP VIEW



BOTTOM VIEW



SIDE VIEW



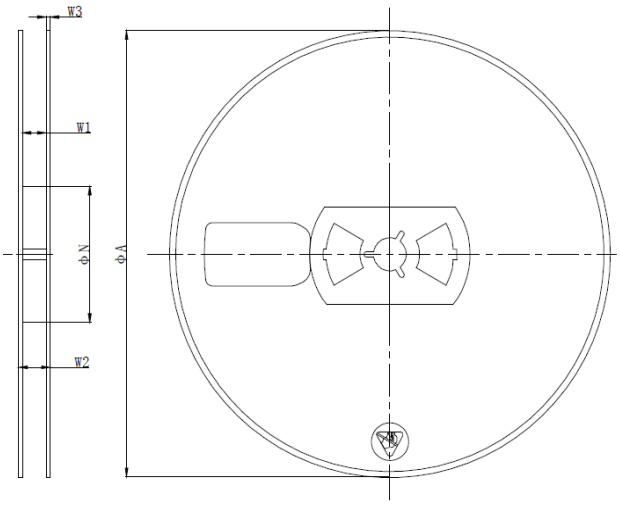
Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.07	0.12	0.17
D	0.95	1.00	1.05
D1	0.43	0.48	0.55
E	0.95	1.00	1.05
E1	0.43	0.48	0.55
e	0.65BSC		
L1	0.2	0.25	0.30
L2	0.27	0.32	0.37
L3	0.09REF		
f	0.18REF		

Tape and Reel Information

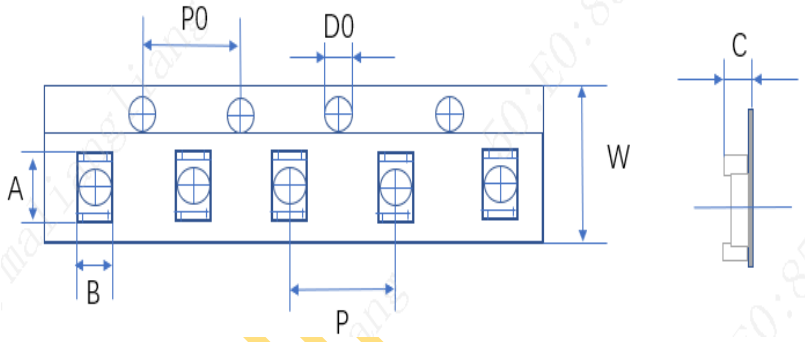
SOT23-5

REEL DIMENSIONS



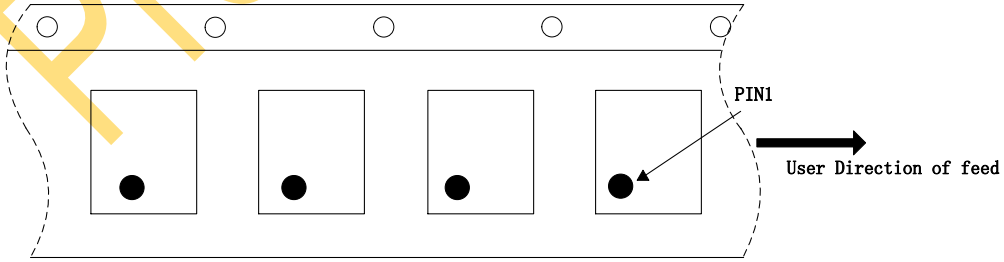
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



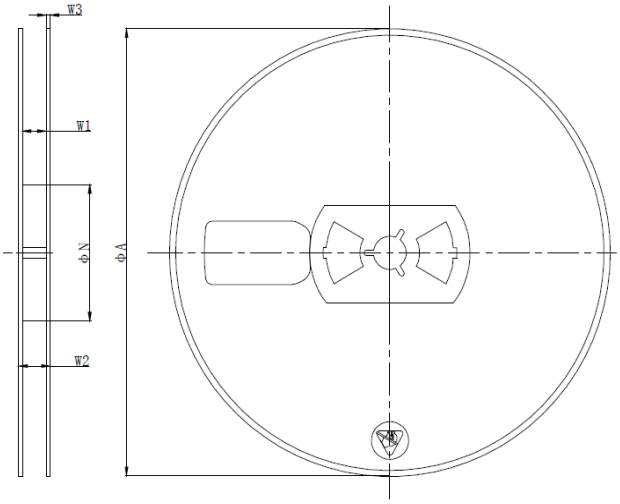
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	3.06	3.26	3.46
P0	3.90	4.00	4.10
P	3.90	4.00	4.10
D0	1.35	1.50	1.65
W	7.70	8.00	8.30
C	1.20	1.40	1.60

PIN1 AND TAPE FEEDING DIRECTION



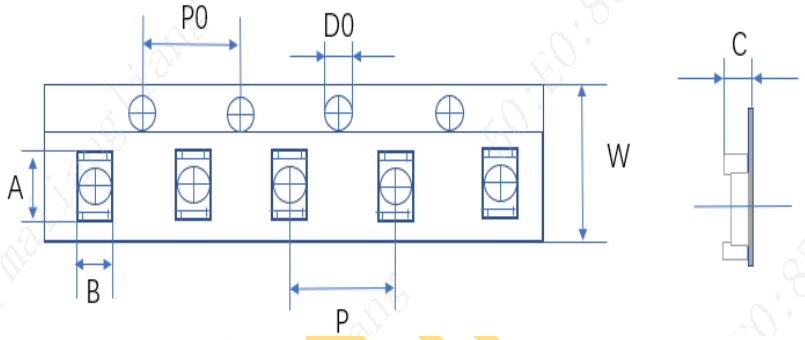
DFN-4

REEL DIMENSIONS



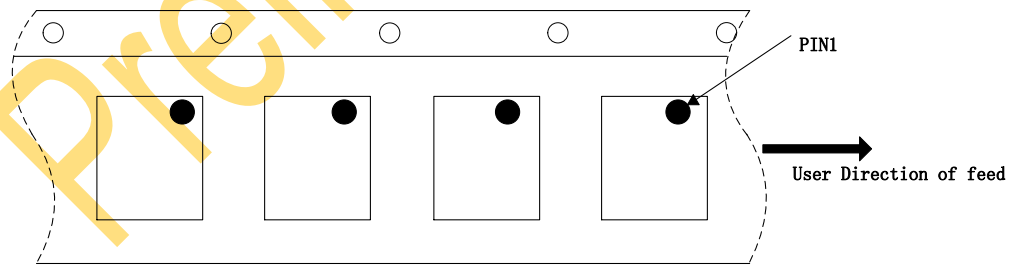
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.96	1.16	1.36
B	0.96	1.16	1.36
P0	3.80	4.00	4.20
P	1.80	2.00	2.20
D0	1.30	1.50	1.70
W	7.90	8.00	8.30
C	0.30	0.50	0.70

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

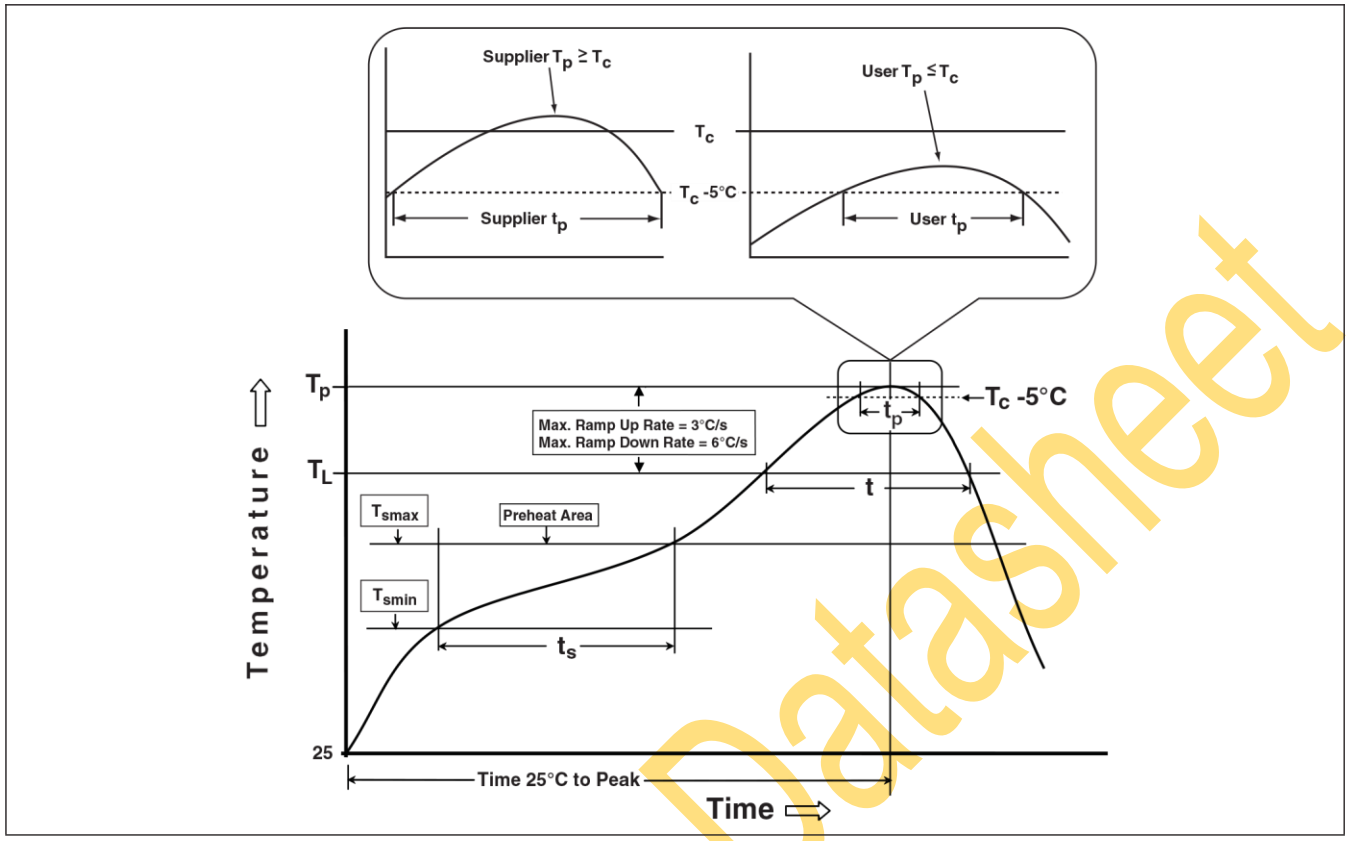


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;