10-Channel Level-Shift with Charge Sharing for GOP Panel

General Description

The LP6297B is a 10-CH high voltage level shifter for TV and monitor LCD applications. It converts logic level signals from Timing Controller (T-CON) to high level signals used by the LCD panel.

The outputs are switching from VGL to VGH, with capacitive loads up to 5nF.

Other features include thermal shutdown protection and under-voltage lockout (UVLO).The LP6297B is available in QFN-32 (0.4mm pitch) package.

Order Information

LP6297B □□□
- F: Green
- Package Type
  - QV: QFN-32

Features

- -20V to 40V High Output Level
- Support Two Kinds of TCON Input Signals
  - TCON Mode 0
  - TCON Mode 1
- High Output Slew Rate to Drive Up to 5nF Load
- Over Temperature Protection
- Available in QFN-32 (4x4mm)
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT for NB Using GOP/IPS Technology
- TFT for Monitors Using GOP/IPS Technology
- TFT for TV Using GOP/IPS Technology

Marking Information

Device	Marking	Package	Shipping
LP6297B	LPS LP6297B YWXXX	QFN-32	3K/REEL
Y: Year code. **W:** Week code. **XXX** : Series number.			

Typical Application Circuit

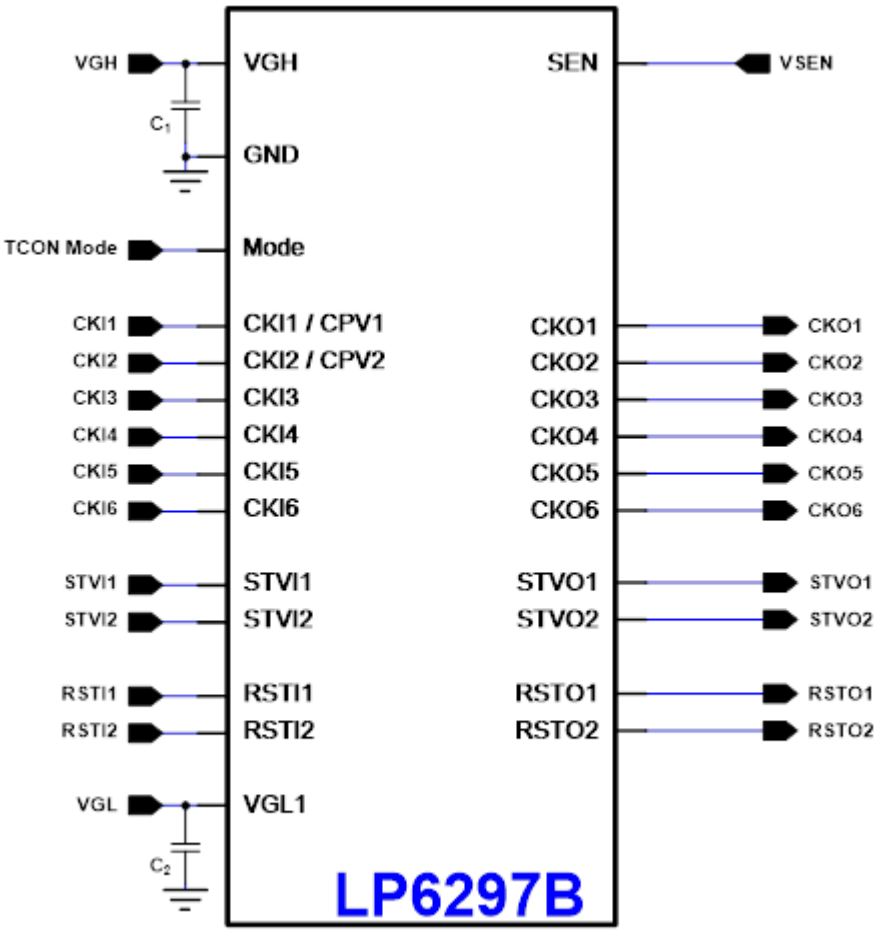


Figure 1. Typical Application Circuit of LP6297B

Pin Configuration

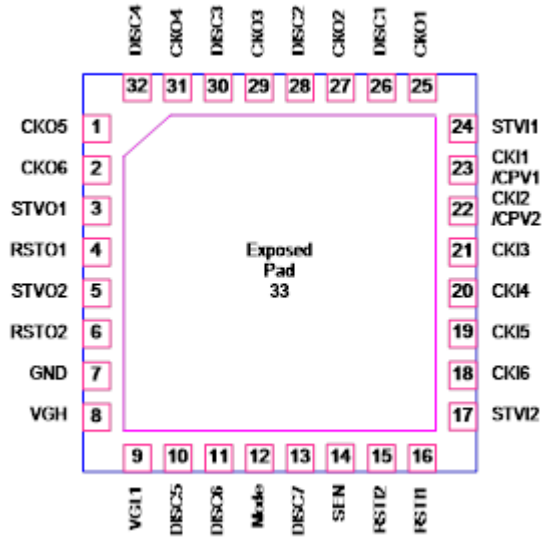


Figure 2. QFN-32 Package (4mm x 4mm)

Function Block Diagram

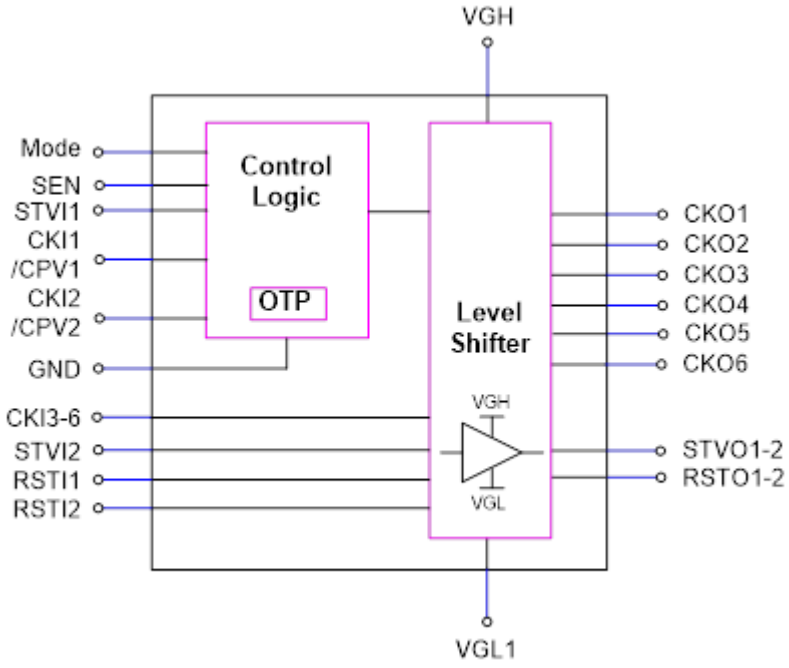


Figure3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	CKO5	Level shifter output.
2	CKO6	Level shifter output.
3	STVO1	Level shifter output.
4	RSTO1	Level shifter output.
5	STVO2	Level shifter output.
6	RSTO2	Level shifter output.
7	GND	Ground.
8	VGH	Positive high supply. Connect this pin with 2.2uF Ceramic capacitor to GND.
9	VGL1	Negative low supply 1. Connect this pin with 2.2uF Ceramic capacitor to GND.
10	DISC5	Disconnected pin.
11	DISC6	Disconnected pin.
12	Mode	TCON mode selection pin. Internal pull-down resistance.
13	DISC7	Disconnected pin.
14	SEN	Sense Voltage pin.
15	RSTI2	Level shifter input. Internal pull-down resistance.
16	RSTI1	Level shifter input. Internal pull-down resistance.
17	STVI2	Level shifter input. Internal pull-down resistance.
18	CKI6	Level shifter input. Internal pull-down resistance.
19	CKI5	Level shifter input. Internal pull-down resistance.
20	CKI4	Level shifter input. Internal pull-down resistance.
21	CKI3	Level shifter input. Internal pull-down resistance.
22	CKI2/CPV2	Level shifter input. Internal pull-down resistance.
23	CKI1/CPV1	Level shifter input. Internal pull-down resistance.
24	STVI1	Level shifter input. Internal pull-down resistance.
25	CKO1	Level shifter output.
26	DISC1	Disconnected pin.
27	CKO2	Level shifter output.
28	DISC2	Disconnected pin.
29	CKO3	Level shifter output.
30	DISC3	Disconnected pin.
31	CKO4	Level shifter output.
32	DISC4	Disconnected pin.
EP		Connect to VGL1. The copper area of the ground plane must be large enough to ensure adequate thermal performance.

Absolute Maximum Ratings Note 1

- ✧ STVI1, STVI2, RSTI1, RSTI2, SEN, Mode, to GND ---------- −0.3V to +7V
- ✧ CKI1/CPV1, CKI2/CPV2, CKI3, CKI4, CKI5, CKI6 to GND ---------- −0.3V to +7V
- ✧ VGH to GND ---------- −0.3V to +45V
- ✧ VGL1 to GND ---------- −20V to +0.3V
- ✧ CKO1, CKO2, CKO3, CKO4, CKO5, CKO6 to VGL1 ---------- −0.3V to +60V
- ✧ STVO1, STVO2, RSTO1, RSTO2 to VGL1 ---------- −0.3V to +60V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40°C to +150°C
- ✧ Operation Ambient Temperature Range ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings only. The functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  QFN-32 4x4, θ_{JA} ---------- 46.8°C/W

  QFN-32 4x4, θ_{JC} ---------- 19.5°C/W

Electrical Characteristics

V_{GH}=25V, V_{GL1}=-10V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
VGH Input Range	V_{GH}		16		45	V
VGL1 Input Range	V_{GL1}		-20		-3	V
Supply Current	I_{GH}	STVIx=RSTIx=CKIx=0V			1	mA
	I_{GL1}	STVIx=RSTIx=CKIx=0V	-0.5			mA
UVLO High Threshold	$V_{UVLO(H)}$	V_{GH} High Level	14	15	16	V
UVLO Low Threshold	$V_{UVLO(L)}$	V_{GH} Low Level	2	3.5	5	V
Thermal Shutdown Threshold	T_{SD}	Temperature Rising	130	150	170	°C
Thermal Shutdown Threshold Hysteresis	T_{SD_Hys}	Temperature Falling		20		°C
Control Signals (SEN, Mode)						
SEN Threshold Voltage	V_{SEN}	V_{SEN} Falling	1.14	1.2	1.26	V
SEN Hysteresis	V_{SEN_HYS}	V_{SEN} Rising		50		mV
Mode Threshold Voltage	V_{Mode}	TCON Mode 0			0.8	V
		TCON Mode 1	2			
Mode Pull Down Resistor	R_{PD_Mode}		50	100	200	kΩ
Level Shifters (STVx, RSTx)						
Level Shifter Input Threshold	V_{IL}	STVIx, RSTIx Falling			0.8	V
	V_{IH}	STVIx, RSTIx Rising	2			
Pull Down Resistor	R_{PD}	STVIx, RSTIx	50	100	200	kΩ
High Side On Resistance	R_{DS_H}			30	60	Ω
Low Side On Resistance	R_{DS_L}			15	30	
Slew Rate	T_R	C_{OUT}=4.7nF, From 20% to 80%	20			V/us
	T_F	C_{OUT}=4.7nF, From 80% to 20%	30			
Propagation Delay	T_{R_dly}	C_{OUT}=150pF, V_{OUT} Rising		40	100	ns
	T_{F_dly}	C_{OUT}=150pF, V_{OUT} Falling		50	100	

Electrical Characteristics(Continued)

V_{GH}=25V, V_{GL1}=-10V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Level Shifters (CKx)						
Operating Frequency	Freq	CPV1, CPV2			500	kHz
Level Shifter Input Threshold	V_{IL_CK}	CKIx Falling			0.8	V
	V_{IH_CK}	CKIx Rising	2			
Pull Down Resistor	R_{PD_CK}	CKIx	50	100	200	kΩ
High Side On Resistance	$R_{DS\_H\_CK}$			11	25	Ω
Low Side On Resistance	$R_{DS\_L\_CK}$			7	15	Ω
Slew Rate	T_{R_CK}	C_{OUT}=4.7nF, From 20% to 80%	50			V/us
	T_{F_CK}	C_{OUT}=4.7nF, From 80% to 20%	50			
Propagation Delay	$T_{R\_dly\_CK}$	C_{OUT}=150pF, V_{OUT} Rising		40	100	ns
	$T_{F\_dly\_CK}$	C_{OUT}=150pF, V_{OUT} Falling		50	100	

Timing Diagram - Power On/ Off Sequence

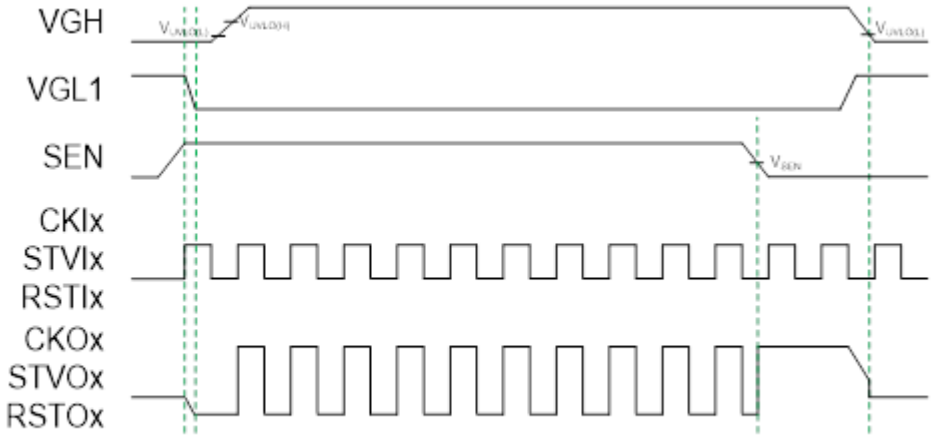


Figure 4. Power Sequence with TCON Mode0

Timing Diagram - TCON Mode0

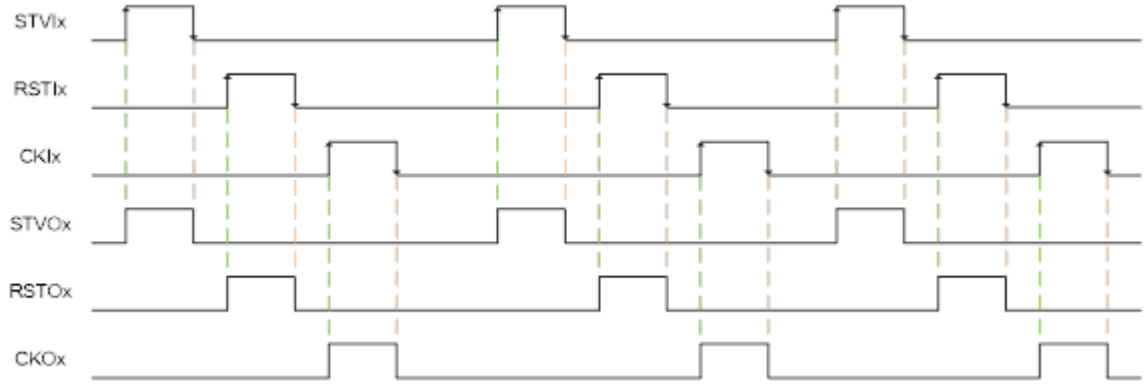


Figure 5. TCON Mode0

TCON Mode0 Description:

1.STVIx↑/RSTIx↑ / CKIx↑ @ STVOx↑ /RSTOx↑ / CKOx↑;

2.STVIx↓ /RSTIx↓ / CKIx↓ @ STVOx↓ /RSTOx↓ / CKOx↓;

Timing Diagram - TCON Mode1

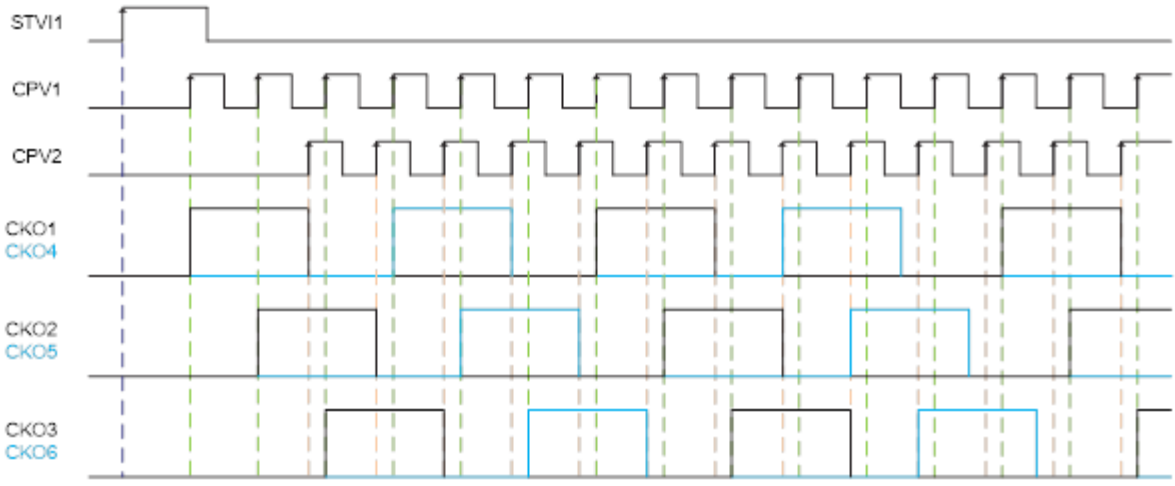


Figure 6. TCON Mode1

TCON Mode1 Description:

1. TCON input signals are STVI1, CPV1, CPV2.

2. When STVI1 is rising, all CKOx must be pull low; until CPV1 is rising edge, CKOx could active.

3. CPV1 rising edge will decide six CKOx rising location, and CPV2 rising edge will decide six CKOx falling location.

Application Information

The LP6297B is level shifter for TFT LCD panel in GOP application. The device has six clock outputs, two STV outputs, two RST outputs. The clock output supports normal TCON application and CPV input application which can save TCON output value.

Under Voltage Lockout (UVLO)

The LP6297B had an UVLO internal circuit that VGH is lower than UVLO(L), the device function is shutdown and all output are followed VGL value. Enable the device that output follow input once the voltage on the VGH voltage exceeds the UVLO(H) threshold voltage if VSEN high level. In the case where UVLO(H) > VGH > UVLO(L), the outputs are all at VGL level.

TCON Mode Selection

The device supports two TCON modes.

TCON mode 0	Level shifter follows STVIx / RSTIx / CKIx. It converts signal to higher / lower level signal.
TCON mode 1	Decode CPV1 and CPV2 signal to generate the higher / lower level output. The rising edge of CPV1 decides CKOx rising location, and the rising edge of CPV2 decides CKOx falling location.

Refer to figure 5 and figure 6 for TCON mode timing.

Over Temperature Protection

If LP6297B junction temperature reaches 150°C (typ.) an over thermal protection block disables all the outputs and lets the part cool down. After its junction temperature drops by 20°C (typ.), a new Soft-Start cycle will be initiated.

Layout Guideline

The output stages of the LP6297B are capable of sinking and sourcing high peak currents and care must be taken during PCB layout to ensure that this performance. In particular, the change of current at the rising and falling edges of each output require stray inductance to be minimized. It is easily solved by routing the output signals using short, wide PCB trace and a low impedance ground plane on the opposite side of PCB to conduct return currents. Trace between the decoupling capacitors and the corresponding power supply pins should also be keeping short and wide as possible.

1. The input capacitor should be located as closed as possible to the VGH, VGL and ground plane.

2. Minimize the distance of all traces connected to the Output node, which the traces short and wide route to obtain optimum performance.

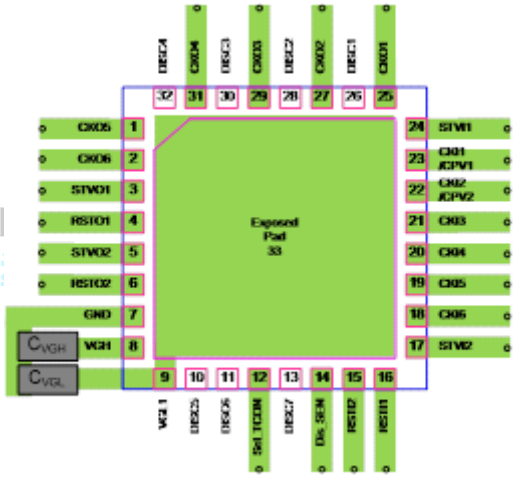
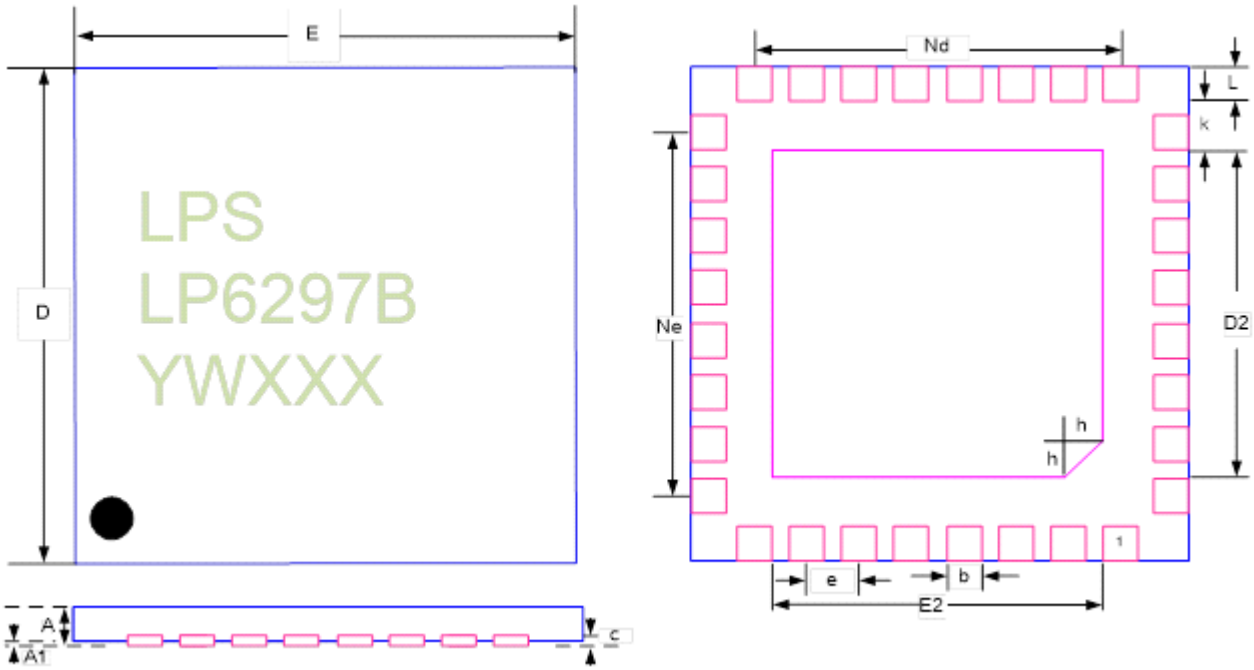


Figure 7. Recommended LP6297B PCB Layout

Outline Information

QFN-32 Package (4x4) pitch 0.4 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.600	---	2.900
E	3.900	4.000	4.100
E2	2.600	---	2.900
K	0.300	---	---
e	0.400 BSC		
Nd	2.800 BSC		
Ne	2.800 BSC		
L	0.200	0.400	0.450
h	0.300	0.350	0.400