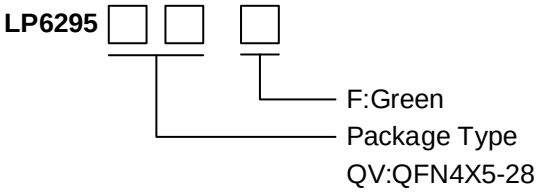
Features

- **Input Supply Voltage Range**
  - VGH1/VGH2: 20V to 40V
  - VGL1/VGL2: -18V to -3.0V
- 14 Channel Level Shifter
- High Output Slew Rate to Drive Up to 4.7nF Load
- 55V Maximum Input for VGH - VGL
- Phase Options: 4-Phase, 6-Phase or 8-Phase
- Selectable 1-line/ 2-line mode
- Over Current Protection
- VGH Input Under Voltage Lockout
- Over Temperature Protection
- RoHS Compliant and 100% Lead(Pb)-Free
- Compact Package: QFN4×5-28

Applications

- LCD Panels Using GIP / GOA / ASG Technology

Order Information

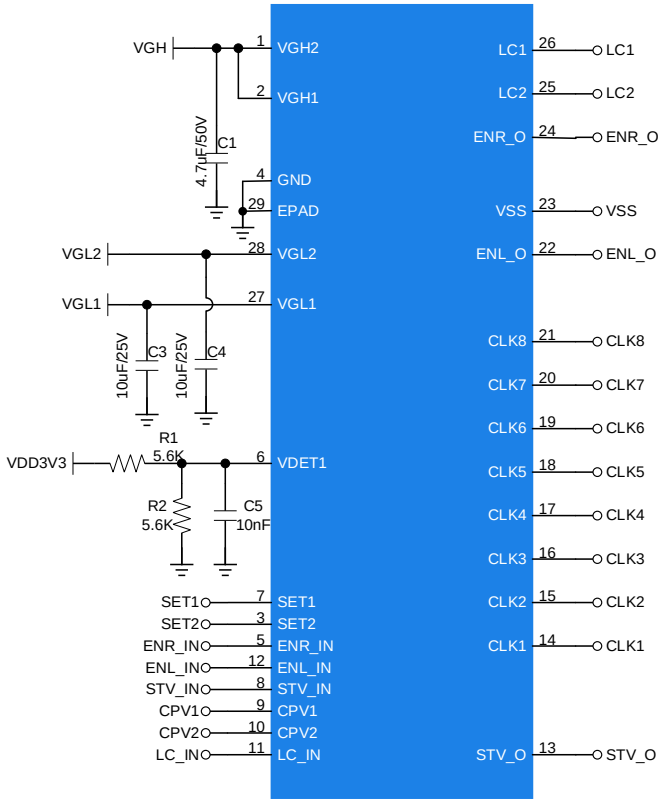


General Description

The LP6295 is a 14-CH high voltage level shifter for TV and monitor LCD applications. It converts logic level signals from Timing Control (TCON) to high level signals used by the LCD panel. It provides 14 outputs (CLK1~8, STV_O, LC1, LC2, ENR_O, ENL_O, and VSS). The outputs can drive capacitive loads up to 4.7nF.

The LP6295 has a reset function. Once VDET1 reaches reset level, output channels will be pulled to VGH1 and VGH2. the LP6295 also has an OCP function. Once the current level reaches fault conditions, output channels will be Hi-Z.

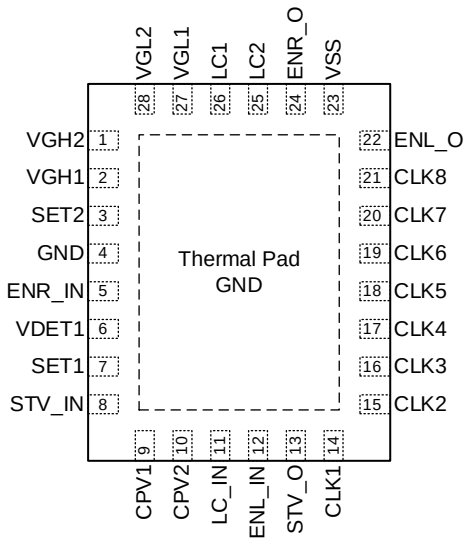
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6295QVF	LPS LP6295 YWXA1	MSL3	QFN4X5-28	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



LP6295QVF

Pin Description

Pin#	Name	Description
1	VGH2	Positive Power Supply for ENR_O, LC1 and LC2. Decouple this pin to GND with a 1μF to 10μF Ceramic Capacitor.
2	VGH1	Positive Power Supply for GSPOUT, CLK1 to CLK8, VSS and ENL_O. Decouple this pin to GND with a 1μF to 10μF Ceramic Capacitor.
3	SET2	Level Shift Input for 1-line/2-line Mode Selection High: 2-line Mode Open/Low: 1-line Mode
4	GND	Ground pin.
5	ENR_IN	Level Shift Input for ENR_O
6	VDET1	Level Shift Input Discharge Sensing Voltage. When VDET1 from High to Low. All Output Channels Pull High to VGH1 or VGH2.
7	SET1	Level Shift Input for Clock Mode Selection. High: 8 CLK outputs Open: 4 CLK outputs Low: 6 CLK outputs
8	STV_IN	Level Shift Input for Start Pulse.
9	CPV1	Level Shift Input for CLKx Start. CLKx Rising Depends on CPV1 Falling Edge.
10	CPV2	Level Shift Input for CLKx End. CLKx Falling Depends on CPV2 Falling Edge.
11	LC_IN	Level Shifter Input for LC1 and LC2.
12	ENL_IN	Level Shifter Input for ENL_O.
13	STV_O	Level Shift Output for Start Pulse. Synchronized with STV_IN
14	CLK1	Level Shift Output.
15	CLK2	Level Shift Output.
16	CLK3	Level Shift Output.
17	CLK4	Level Shift Output.
18	CLK5	Level Shift Output.
19	CLK6	Level Shift Output.
20	CLK7	Level Shift Output.
21	CLK8	Level Shift Output.
22	ENL_O	Level Shifter Output for ENL_IN Clock.
23	VSS	Level Shifter High Voltage Output for Discharging.
24	ENR_O	Level Shifter Output for ENR_IN Clock.
25	LC2	Level Shifter Output LC2 is asynchronous with LC_IN.
26	LC1	Level Shifter Output LC1 is asynchronous with LC_IN.
27	VGL1	Negative Power Supply.
28	VGL2	Negative Power Supply. VGL2 is always higher than VGL1.
29	EPAD	GND

Absolute Maximum Ratings (Note1)

VGH1,VGH2 to GND ---------- -0.3V to +45V
VGL1,VGL2 Voltage to GND ---------- -20V to +0.3V
VGH1/VGH2 to VGL1/VGL2 ---------- -0.3V to +60V
STV_IN,CPV1,CPV2,ENR_IN,ENL_IN to GND ---------- -0.3V to 6V
VDET1 to GND ---------- +0.3V to 16V
STV_O,CLKx,ENR_O,ENL_O,VSS,LC1,LC2 to GND ---------- (-0.3V+VGL) to VGH1/VGH2

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2kV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ---------- 150℃
Operating Junction Temperature Range (TJ) ---------- -40℃ to 150℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- TBD℃/W

Electrical Characteristics

(VGH1/2 = 30V, VGL1/VGL2 = -10V, GND= 0V, VDET1=3.3V TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{GH1},V_{GH2}	VGH1, VGH2 Input Voltage Range		20	---	40	V
V_{GL1},V_{GL2}	VGL, VGL2 Input Voltage Range		-18	---	-3	V
$V_{GH1/2}$-$V_{GL1/2}$	Voltage difference between VGH1/2 & VGL1/2		---	---	55	V
I_{VGH1}	VGH1 Quiescent Current	Channels pull to VGL1/2	---	300	---	μA
I_{VGH2}	VGH2 Quiescent Current	Channels pull to VGL1/2	---	1.5	---	mA
I_{VGL}/I_{VSS}	VGL+VSS Quiescent Current	Channels pull to VGL1/2	---	300	---	μA
$V_{UVLO(H)}$	VGH2 Under Voltage Lockout Threshold	VGH2 Rising	17	18	19	V
$V_{UVLO(L)}$	VGH2 Under Voltage Lockout Threshold	VGH2 Falling	3.0	4.0	5.0	V
V_{DETL}	VDET1 Threshold Voltage	VDET Falling	0.85	0.95	1.05	V
V_{DETH}	VDET1 Threshold Voltage	VDET Rising	1.10	1.20	1.30	V
T_{SD}	Thermal Shutdown Temperature	Rising, Hys.=30℃	---	150	---	°C
T_{HYS}	Thermal Shutdown Hysteresis		---	30	---	°C
INPUT SIGNALS (STV_IN, CPV1/2, SET2, LC_IN, ENR_IN, ENL_IN)						
V_{IH}	STV_IN, CPV1, CPV2, LC, ENR_IN, SET2, ENL_IN Input Voltage		1.4	---	---	V
V_{IL}			---	---	0.6	V
$R_{PULL.DOWN}$	Internal Pull Down Resistor		---	400	---	kΩ
F_{CPV1}, F_{CPV2}	CPV1, CPV2 Maximum Input Operating Frequency		200	---	---	kHz
T_{CPV1}, T_{CPV2}	CPV1, CPV2 Minimum Pulse Width		100	---	---	ns
INPUT SIGNALS (SET1)						
$V_{IH.SET1}$	SET1 High Level Voltage Threshold		1.08	1.20	1.32	V
$V_{IL.SET1}$	SET1 Low Level Voltage Threshold		0.72	0.80	0.88	V
Level Shifter Output (CLK1 to CLK8, VSS, ENR_O,ENL_O, STV_O, LC1, LC2)						
$R_{DS(ON).HS}$	High-Side Output Resistance		---	15	30	Ω
$R_{DS(ON).LS}$	Low-Side Output Resistance		---	10	20	Ω
	Output Voltage Rising Time	RL=51Ω,CL=4.7nF 20% to 80%	---	300	600	ns
	Output Voltage Falling Time	RL=51Ω,CL=4.7nF 80% to 20%	---	300	600	ns
T_{PR}	Rising Edge Propagation Delay	RL=51Ω,CL=4.7nF	---	60	200	ns
T_{PF}	Falling Edge Propagation Delay	RL=51Ω,CL=4.7nF	---	60	200	ns
V_{SL}	Output Voltage Swing Low	Iout=-10mA	VGL	VGL+0.2	VGL+0.5	V
V_{SH}	Output Voltage Swing High	Iout=10mA	VGH-0.5	VGH-0.2	VGH	V

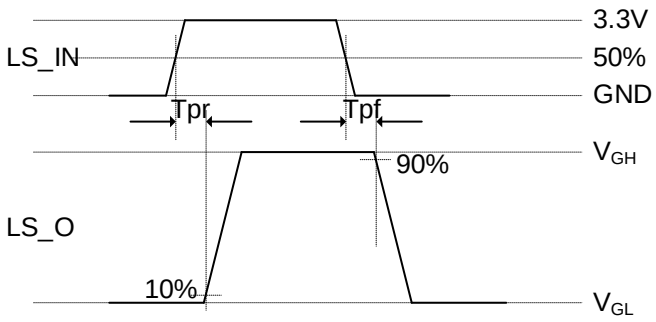
Electrical Characteristics

(VGH1/2 = 30V, VGL1/VGL2 = -10V, GND= 0V, VDET1=3.3V TA= 25℃)

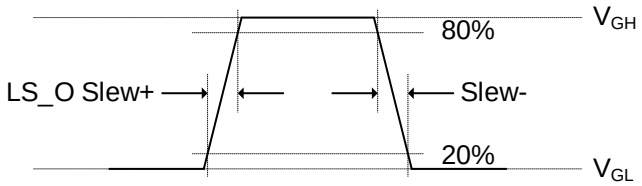
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over Current Protection(CLK1 to CLK8)						
	OCP Level (P-MOSFET)		80	---	---	mA
	OCP Level (N-MOSFET)		80	---	---	mA
$T_{OCP.DET}$	High-Side Delay Time		8	---	---	uS
$T_{OCP.DET}$	Low-Side Delay Time		8	---	---	μS
Over Current Protection (STV_O,ENR_O,ENL_O)						
	OCP Level (P-MOSFET)		80	---	---	mA
	OCP Level (N-MOSFET)		80	---	---	mA
$T_{OCP.DET}$	High-Side Delay Time		8	---	---	uS
$T_{OCP.DET}$	Low-Side Delay Time		30	---	---	μS
Over Current Protection (LC1,LC2,VSS)						
	OCP Level (P-MOSFET)		80	---	---	mA
	OCP Level (N-MOSFET)		80	---	---	mA
$T_{OCP.DET}$	High-Side Delay Time		30	---	---	uS
$T_{OCP.DET}$	Low-Side Delay Time		30	---	---	μS

Note：Rising/Falling time measure point is before RC

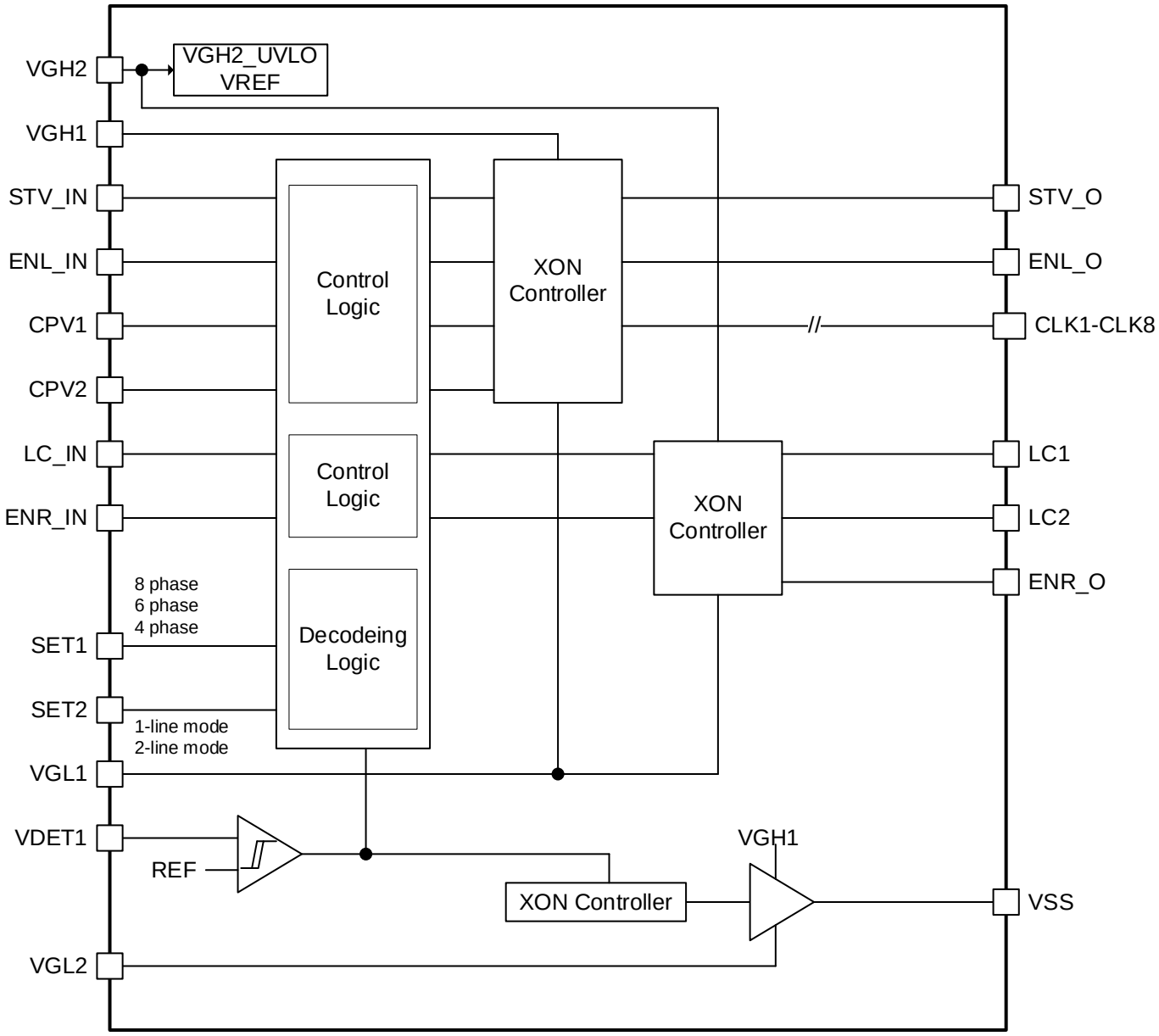


Propagation Delay

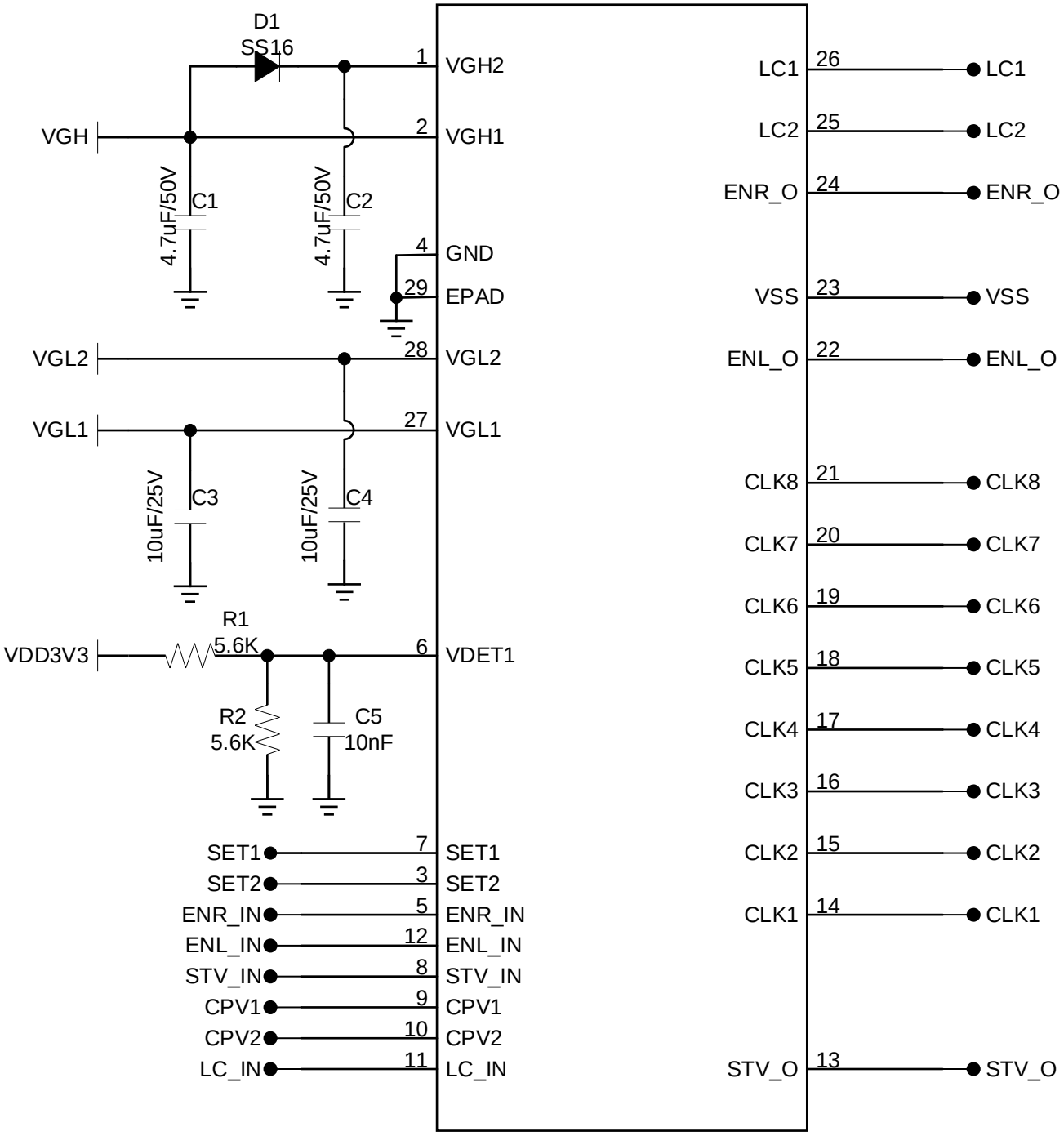


Rising and Falling Time

Functional Block Diagram



Typical Application Circuit



Timing Diagram

Power On/Off Sequence

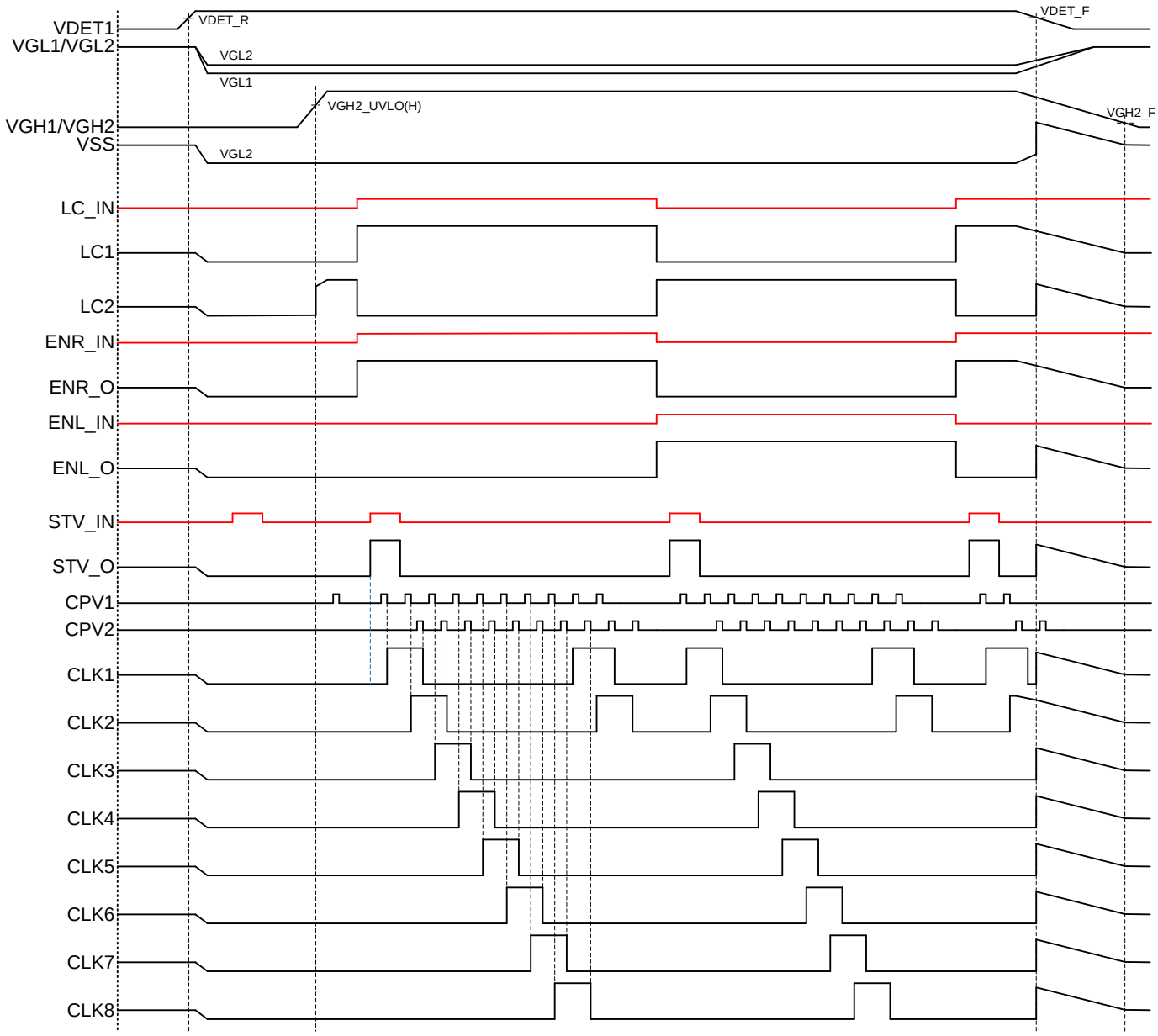


Figure 1 SET1=High:8CLK output; SET2=Open/Floating:1-line Mode

SET1

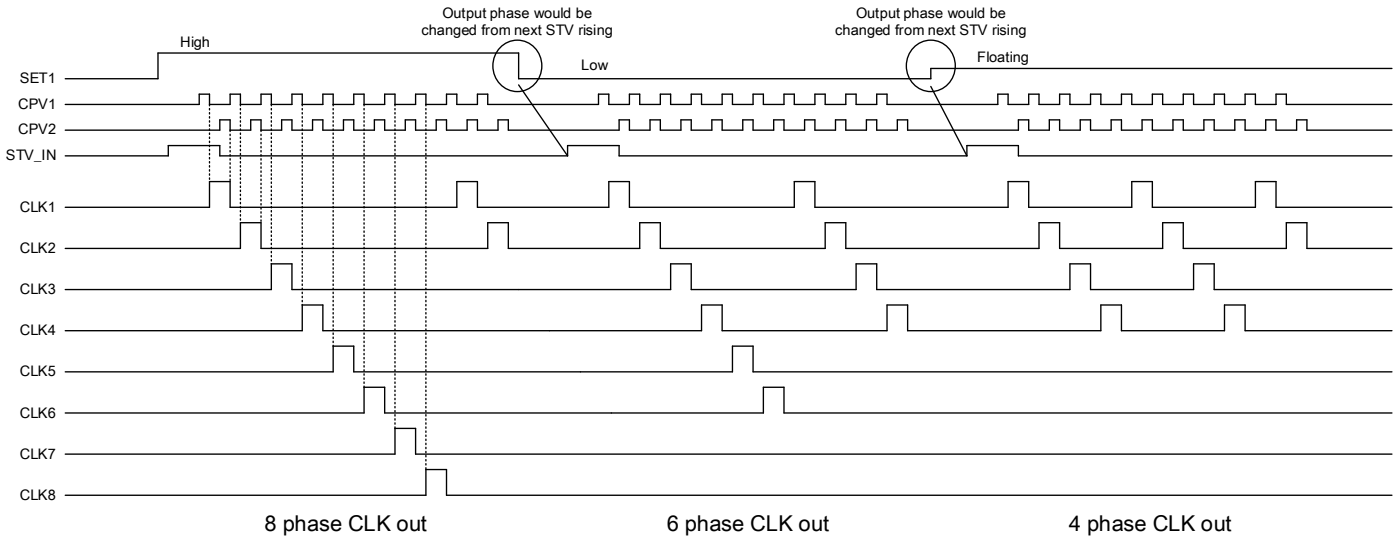


Figure 2 SET1 Function

SET2

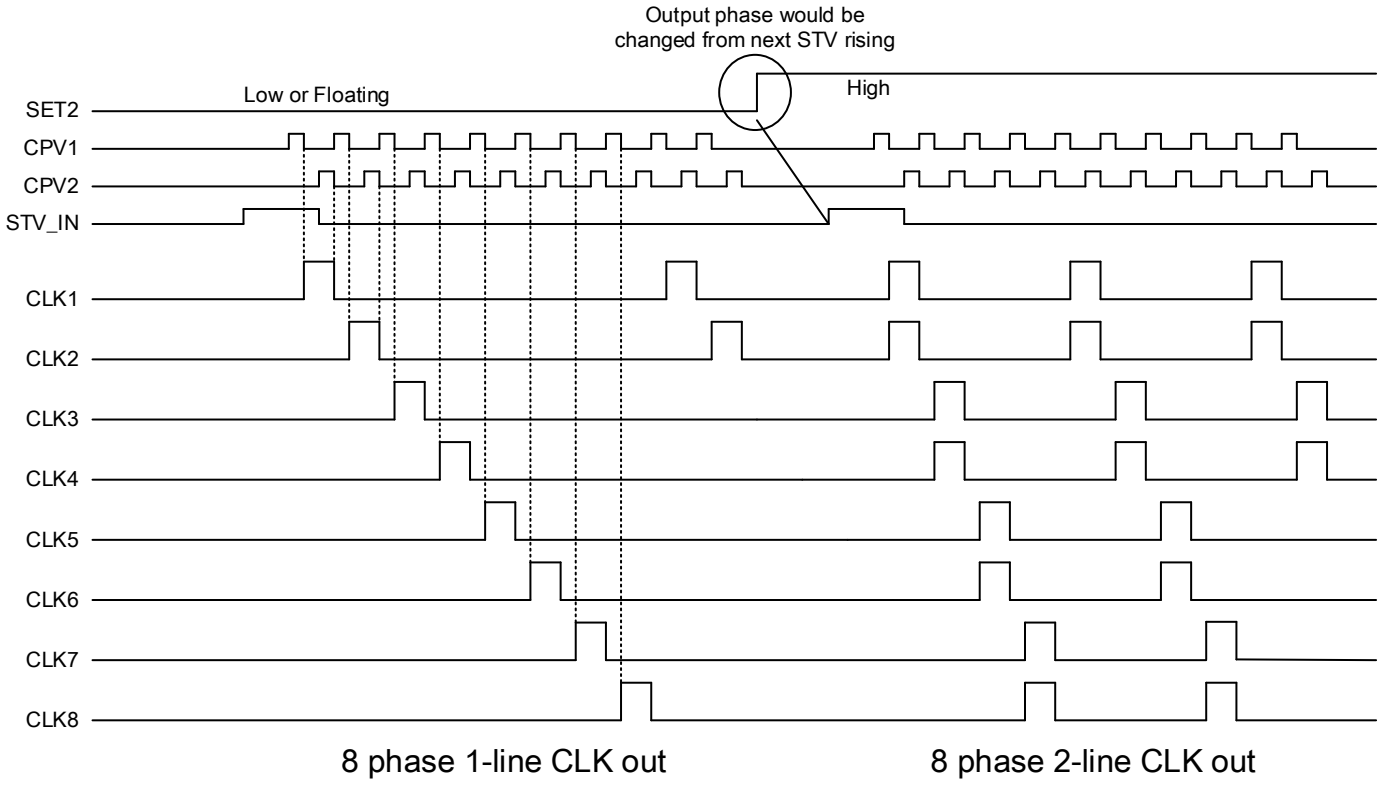


Figure 3 SET2 Function

Level Shift Logic Function Control (Timing Setting)

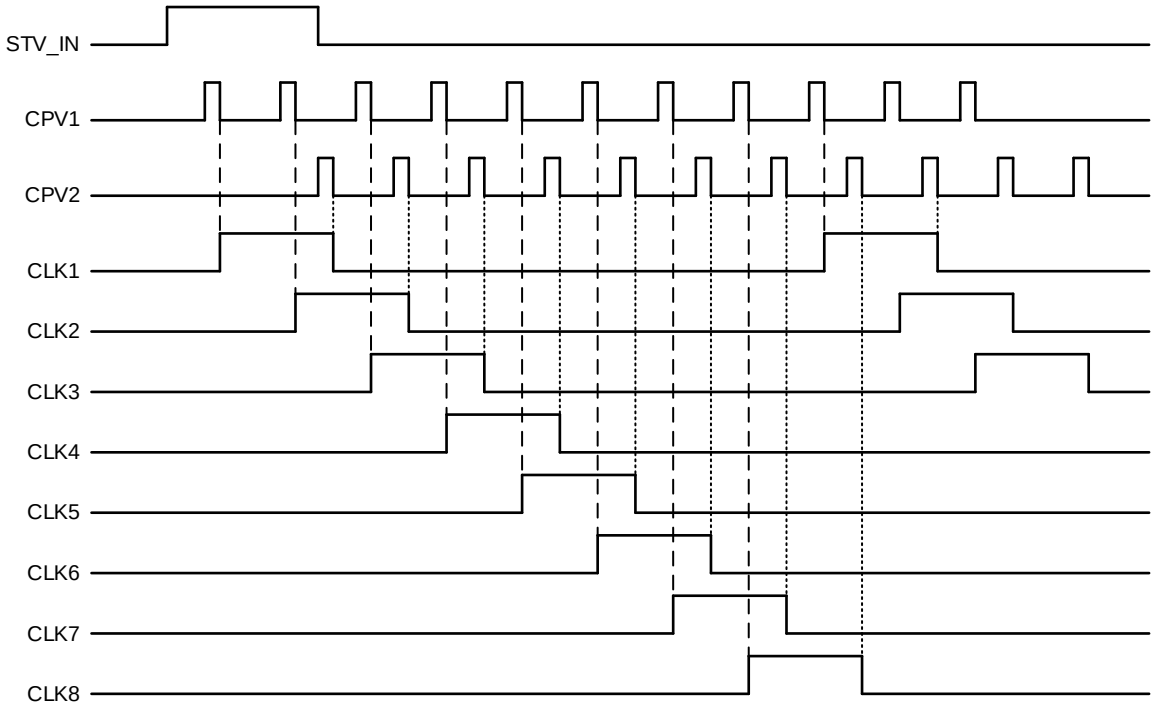


Figure 4 SET1=High Level(8 phase); SET2=Low or Floating(1 line)

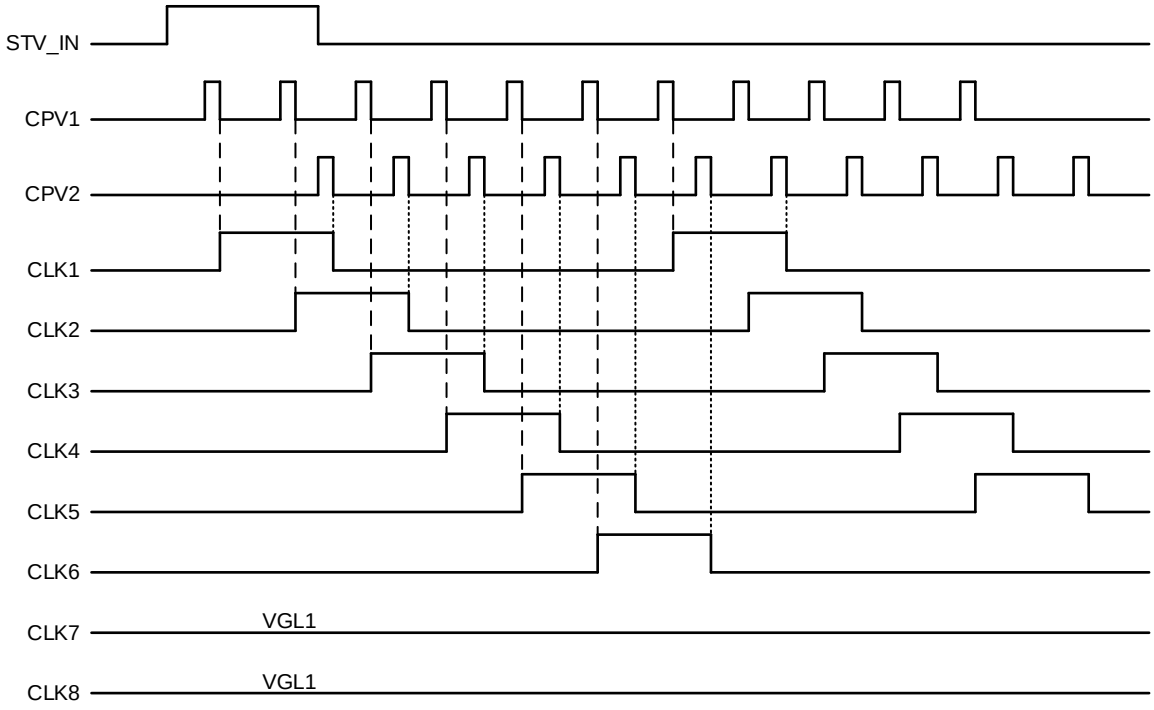


Figure 5 SET1=Low Level(6 phase); SET2=Low or Floating(1 line)

Level Shift Logic Function Control (Timing Setting)

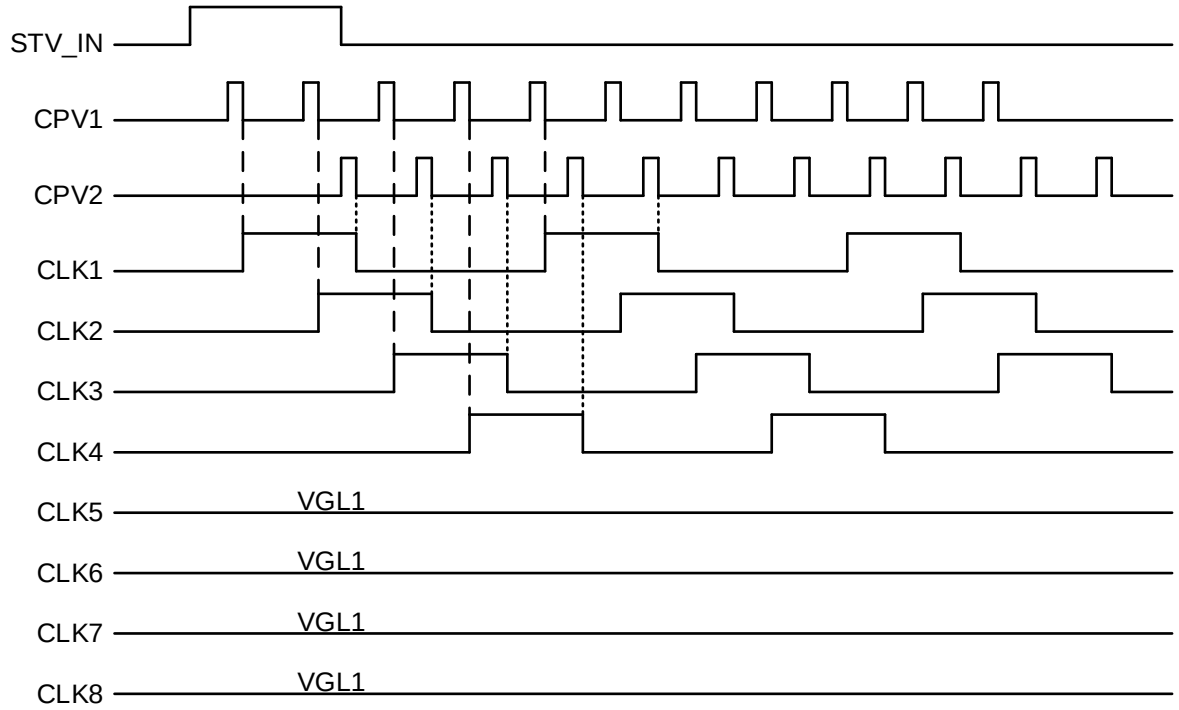


Figure 6 SET1=Floating Level(4 phase); SET2=Low or Floating(1 line)

PIN NAME	STATUS	FUNCTION
SET1	High level	8 Phase CLK Output
	Low level	6 Phase CLK Output
	Floating	4 Phase CLK Output

Level Shift Logic Function Control (Timing Setting)

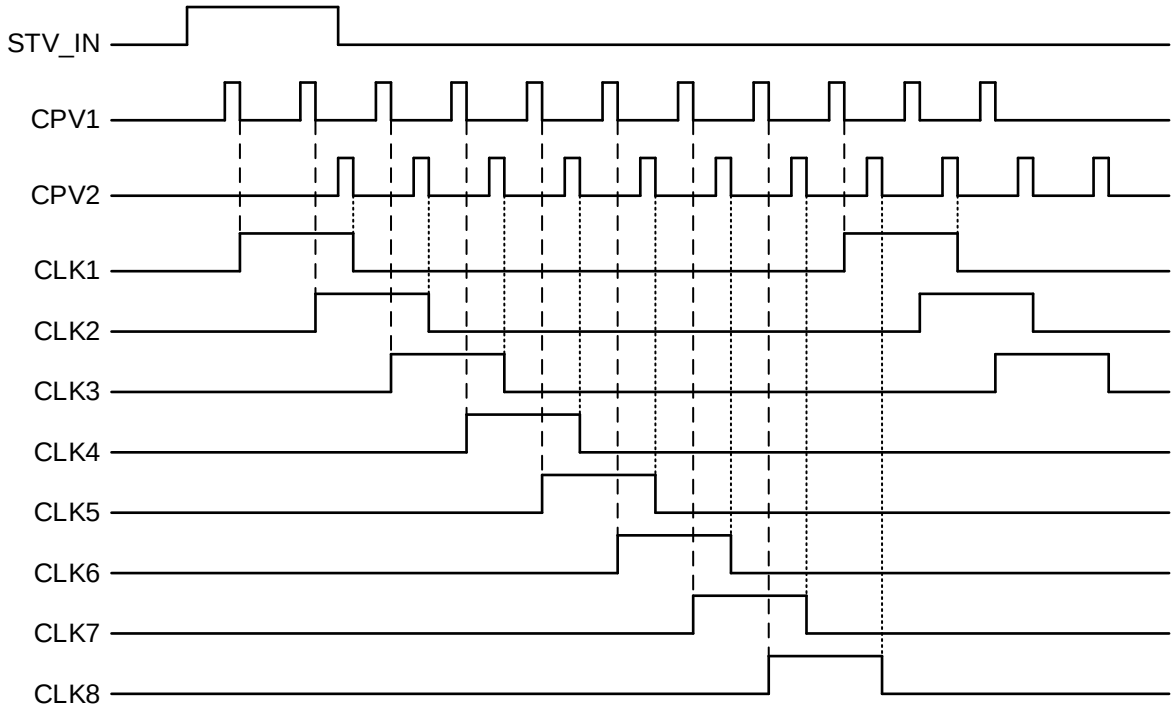


Figure 7 SET1=High Level(8 phase); SET2=Low or Floating(1 line)

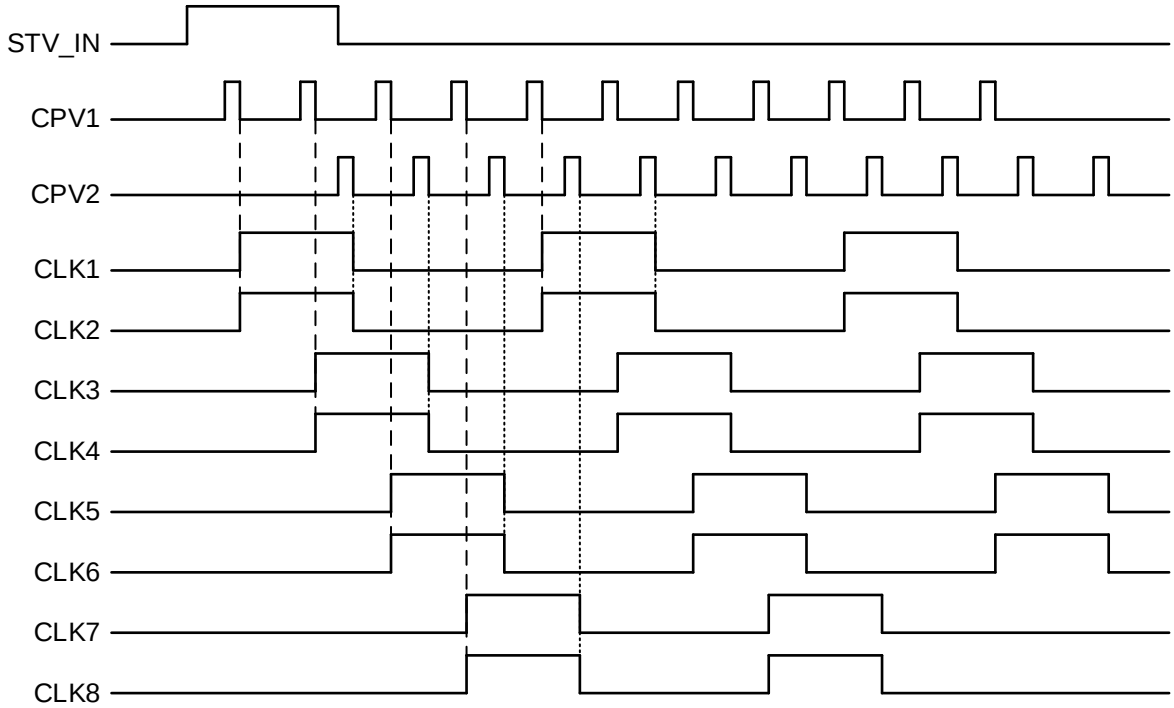


Figure 8 SET1=High Level(8 phase); SET2=High Level(2 line)

PIN NAME	STATUS	FUNCTION
SET2	High level	2-line Mode
	Low level/Floating	1-line Mode

Power on logic Table:

Case	Power Input			Logic Input				Level Shifter Output				
	VDET1	VGH2	VGL	STV_IN	CPV1 CPV2	ENR_IN ENL_IN	LC_IN	STV_O	CLK1~8	ENR_O ENL_O	LC1/LC2	VSS
1	>VDET 1(R)	>UVLO (R)	Don't Care	w/ Signal	w/ Signal	w/ Signal	w/ Signal	Normal Operation	Normal Operation	Normal Operation	Normal Operation	VGL
2	>VDET 1(R)	>UVLO (R)	Don't Care	w/ Signal	w/ Signal	w/ Signal	w/o Signal	Normal Operation	Normal Operation	Normal Operation	LC1=VGL LC2=VGH	VGL
3	>VDET 1(R)	>UVLO (R)	Don't Care	w/ Signal	w/ Signal	w/o Signal	w/ Signal	Normal Operation	Normal Operation	VGL	Normal Operation	VGL
4	>VDET 1(R)	>UVLO (R)	Don't Care	w/ Signal	w/o Signal	w/ Signal	w/ Signal	Normal Operation	VGL	Normal Operation	Normal Operation	VGL
5	>VDET 1(R)	>UVLO (R)	Don't Care	w/o Signal	w/ or w/o Signal	w/ Signal	w/ Signal	VGL	VGL	Normal Operation	Normal Operation	VGL
6	>VDET 1(R)	>UVLO (R)	Don't Care	w/ Signal	w/o Signal	w/o Signal	w/ Signal	VGL	VGL	VGL	Normal Operation	VGL
7	>VDET 1(R)	>UVLO (R)	Don't Care	w/o Signal	w/o Signal	w/o Signal	w/o Signal	VGL	VGL	VGL	LC1=VGL LC2=VGH	VGL
8	<VDET 1(R)	>UVLO (R)	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGH1	VGH1	VGH2 VGH1	VGH2	VGH1
9	>VDET 1(R)	<UVLO (R)	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL	VGL	VGL	VGL	VGL2
10	<VDET 1(R)	<UVLO (R)	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL	VGL	VGL	VGL	VGL2

Power off logic Table:

Case	Power Input			Logic Input				Level Shifter Output				
	VDET1	VGH2	VGL	STV_IN	CPV1 CPV2	ENR_IN ENL_IN	LC_IN	STV_O	CLK1~8	ENR_O ENL_O	LC1/LC2	VSS
1	<VDET 1(F)	>UVLO (F)	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGH1	VGH1	VGH2 VGH1	VGH2	VGH1
2	<VDET 1(F)	<UVLO (F)	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGH1	VGH1	VGH2 VGH1	VGH2	VGH1
3	>VDET 1(F)	<UVLO (F)	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL	VGL	VGL	VGL	VGL2

PCB Layout Guidelines

PCB layout is very important for designing power converter circuits. The following layout guidelines should be strictly followed for best performance of the LP6295. Place the power components as close to the IC as possible. The VGL1/VGL2 VGH1/VGH2 input Capacitor should be closed the chip The traces should be wide and short, especially for the high current loop. The exposed pad of the chip should be connected to a large PCB plane for maximum thermal consideration.

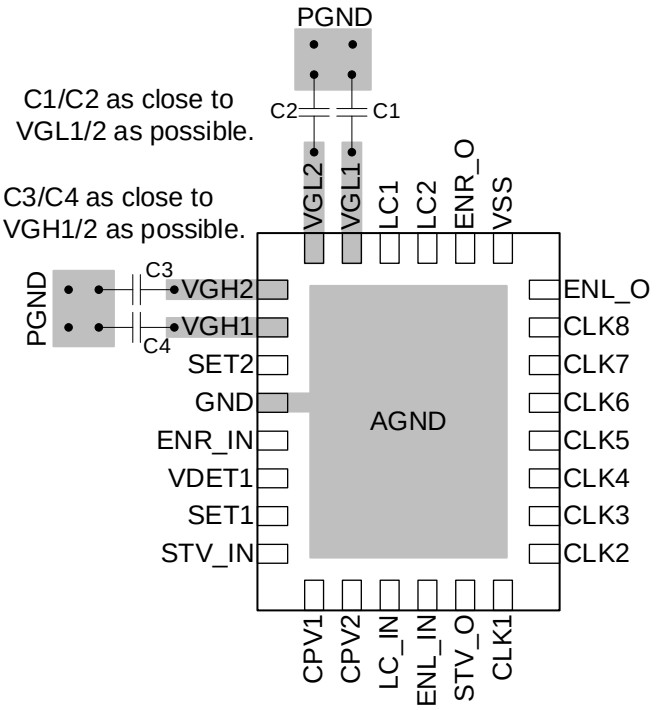
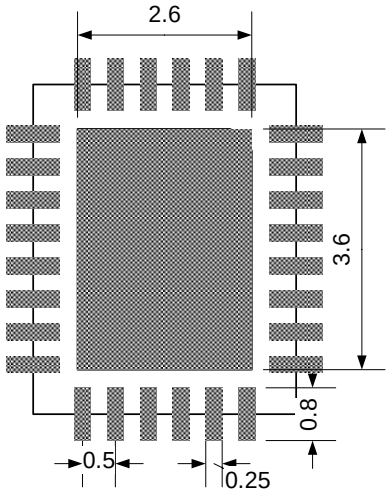


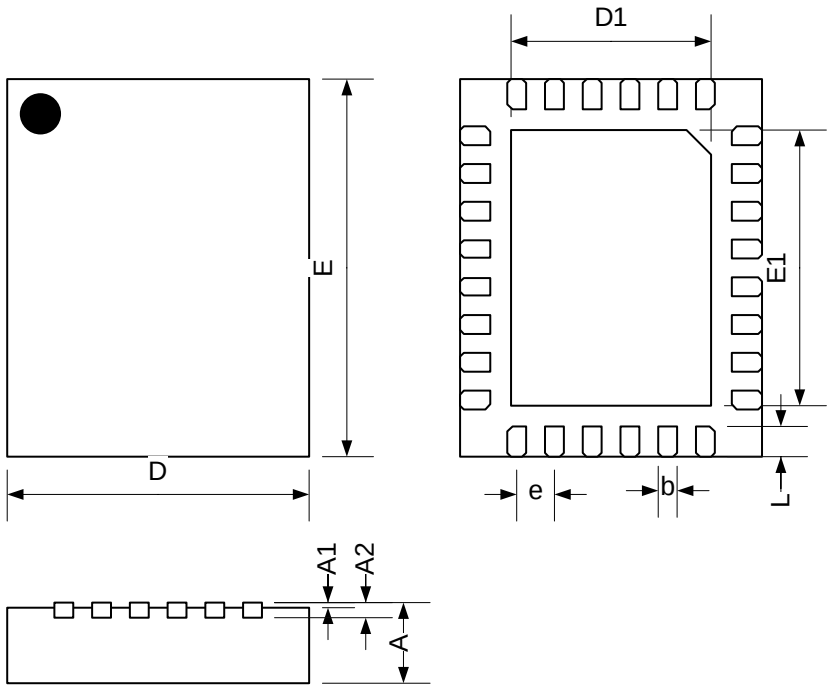
Figure 9 PCB Layout Guide

Minimum Footprint PCB Layout Section



Packaging Information

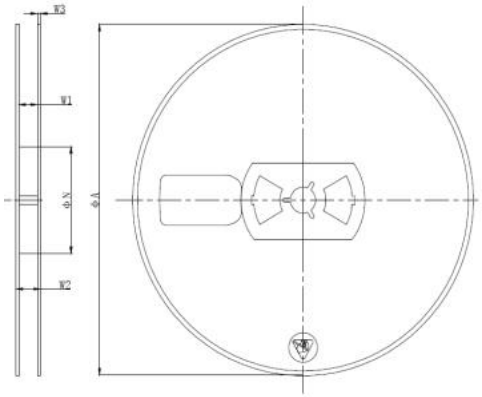
QFN4X5-28



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
D1	2.60	2.65	2.70	0.1024	0.1043	0.1063
E1	3.60	3.65	3.70	0.1417	0.1437	0.1457
b	0.20	0.25	0.30	0.0079	0.0098	0.0118
e	0.5 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

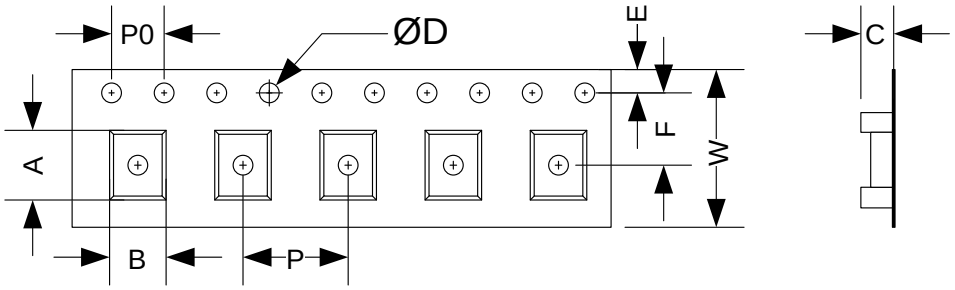
QFN28 0504 Tape and Reel information

REEL DIMENSIONS（Unit:mm）



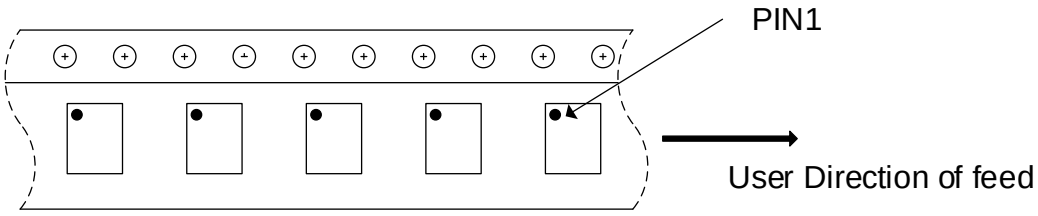
ΦA	W2
329±2	12.4±2

TAPE DIMENSIONS（Unit:mm）



A	B	P0	P	D0	W	C	E	F
5.30±0.10	4.30±0.10	4.00±0.10	8.00±0.10	1.50±0.10	12.00±0.30	1.10±0.15	1.75±0.10	5.50±0.05

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min(T_{SMIN}) Temperature Max(T_{SMAX}) Time(T_S) from (T_{SMIN} to T_{SMAX})	 100℃ 150℃ 60~120 seconds	 150℃ 200℃ 60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L) Time(t_L) maintained above T_L	183℃ 60~150 seconds	217℃ 60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed theClassification temp in Table 1. For suppliers T_P must equal or exceedthe Classification temp in Table 1.	For users T_P must not exceed theClassification temp in Table 2. For suppliers T_P must equal or exceedthe Classification temp in Table 2.
Time(t_P)* within 5 ℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

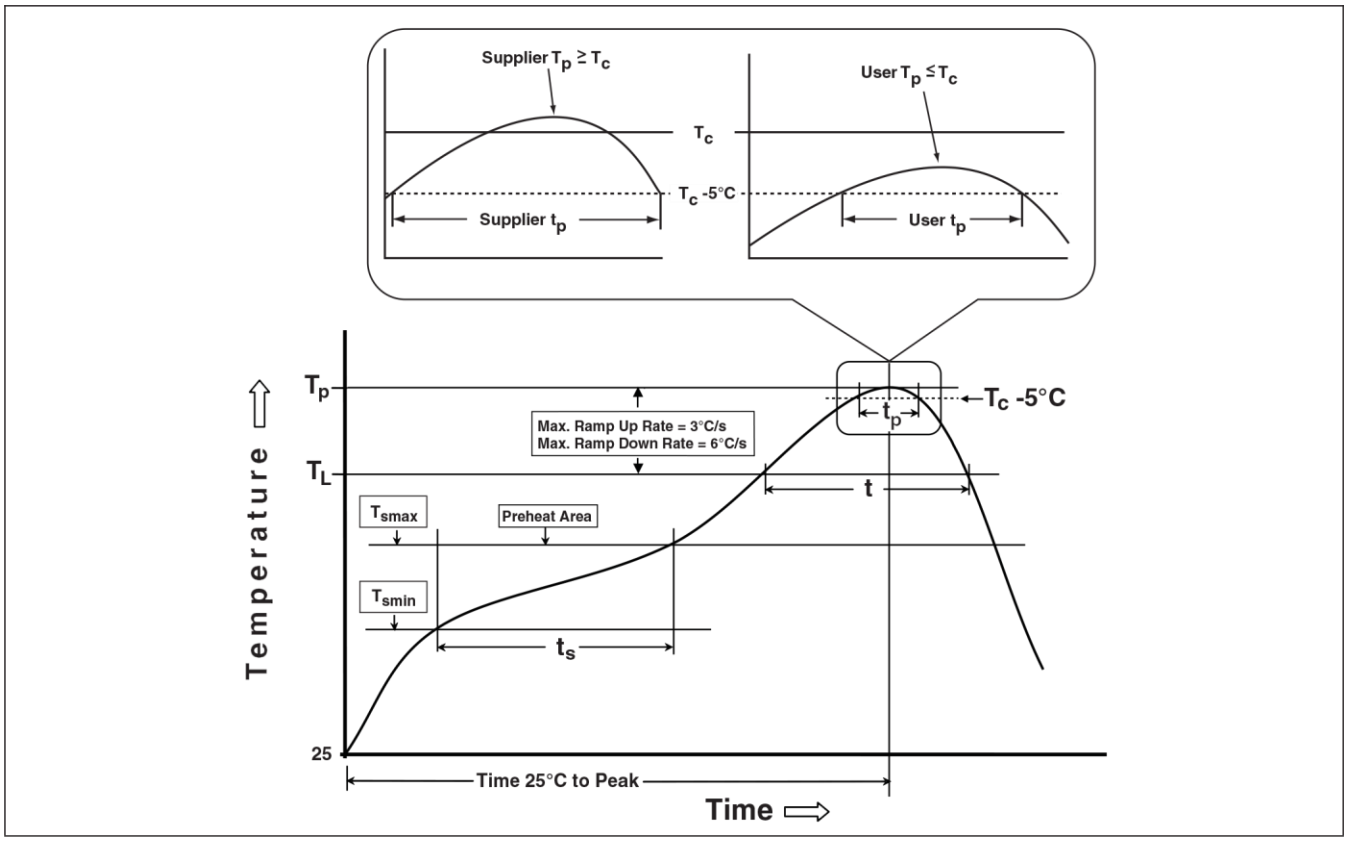


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C"standards;

Products shipped conform to "Rohs"standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;

Revision History

Revision	Date	Change Description
Rev 0.1p0	06/05/2022	Product Brief