LP4033

30V, I²C Controlled, Buck Mode Charger

Features

- Input over-voltage protected up to 30V
- Charge management
  - Programmable charge current up to 3-A with up to 95% switching efficiency
  - Programmable floating voltage with 0.35% accuracy
  - Programmable trickle charge and termination current with minimum 30-mA termination current
- Automatic re-charge and thermal foldback
- I²C bus to the MCU with an interrupt pin
- Power path management
- Boost converter with up to 1.5-A output
- Two independent load switches with up to 600-mA output for each channel
- Load insertion and removal detection
- Ultra-low quiescent current linear regulator
- NTC management
- Rich protections: UVLO, OVP, SCP
- Minimum 5-μA ultra-low iq in normal operation
- 4mm X 4mm QFN-24 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Wireless Microphone
- Smart Glasses
- Electrical Tool
- Bluetooth Speaker

General Description

The LP4033 is a fully integrated switch mode charger solution with power path management targeting single-cell Li-ion battery powered portable applications. A low on-resistance BUS-FET is integrated to manage the input power from the VIN pin. A bidirectional buck or boost converter is integrated to manage charging and discharging of the battery. The buck charger supports up to 3-A charging current with up to 95% efficiency. The ultra-low quiescent current boost converter consumes less than 2-μA and supports up to 1.5-A output current. Two independent load switches provide power from the PMID pin to the LDSW1 pin and LDSW2 pin with high accuracy current limit. An NTC circuit is offered to manage the temperature range that charging or discharging is allowed. A LDO pin delivers power to the system that contains an MCU typically. The LP4033 offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the VIN input and the battery to meet the system loading needs. An I²C interface enables programming various parameters of charging, discharging, and multiple protection functions. An interrupt output (IRQb) sends a signal to the MCU when an interrupt event happens so the MCU can take actions accordingly.

Multiple features are offered for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), etc. When powered by a battery, LP4033 can operate with only 5-μA current.

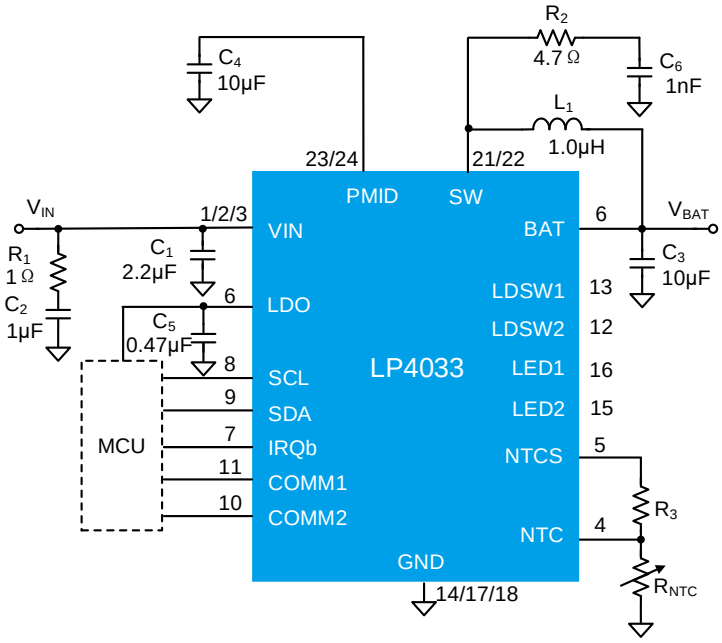
The whole System is in a 24-pin 4 X 4 QFN package.

Order Information

LP4033 □□ □

- F：Green/Pb-Free
- Package Type
  - QV : QFN

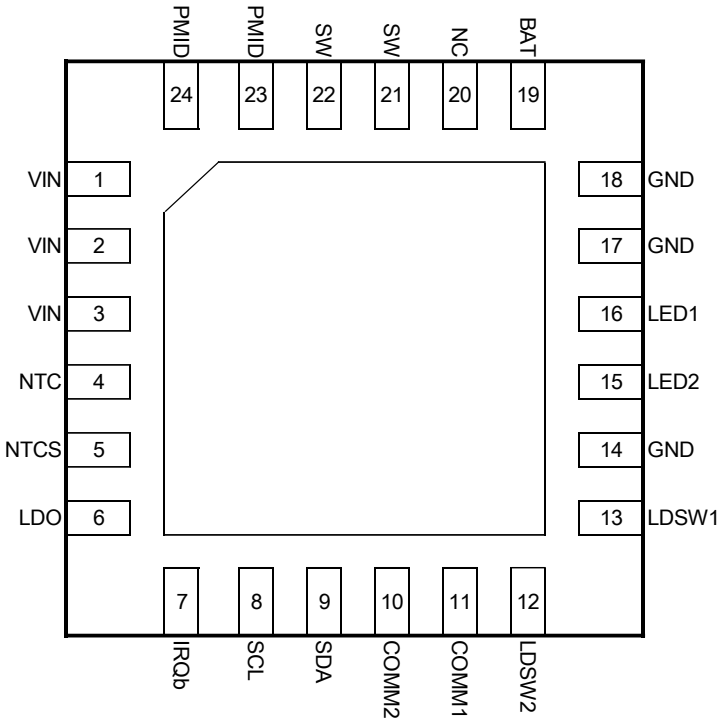
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	MSL
LP4033QVF	LPS LP4033 YWX	24-pin 4 X 4 QFN	3K/REEL	LEVEL 3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. **MSL: Moisture Sensitivity Level, according to JEDEC Standard.**				

Pin Diagram



LP4033 Pinout

Pin Description

Pin #	Name	Description
1/2/3	VIN	Input voltage that is connected to the positive input of the USB port. 30-V maximum voltage rating. A 1-µF or higher value input decoupling capacitor must be connected to this pin and the GND pins.
4	NTC	NTC pin. Connect the NTC resistor divider between this pin, NTCS and GND pin.
5	NTCS	This pin is the bias power supply for the NTC circuits. This NTCS is power down in standby status (STD=1).
6	LDO	Ultra-low quiescent current LDO output to power an external MCU or sensors.
7	IRQb	Interrupt output to the external MCU. This pin is pulled-up to LDO pin with a 1-MΩ resistor.
8	SCL	Clock line of the I²C bus. This pin is pulled-up to LDO pin with a 5.1-kΩ resistor.
9	SDA	Data line of the I²C bus. This pin is pulled-up to LDO pin with a 5.1-kΩ resistor.
10	COMM2	Load switch2 communication pin. This pin is bi-directional.
11	COMM1	Load switch1 communication pin. This pin is bi-directional.
12	LDSW2	Load switch channel 2 output pin.
13	LDSW1	Load switch channel 1 output pin.
14	GND	Ground. Connect to the pin17,18 on PCB.
15	LED2	Open-drain LED output.
16	LED1	Open-drain LED output.
17/18	GND	Ground. Connect to the pin14 on PCB.
19	BAT	Battery voltage sense pin of the buck charger.
20	NC	No connection inside. Connect to GND for good PCB layout.
21/22	SW	Switch node of the boost converter/ buck charger.

23/24	PMID	Power input for the buck charger and power output for the load switches. A 10-µF or higher ceramic capacitor is required between this pin and the GND pins.
Thermal PAD		Connect to GND for good PCB and thermal dissipation.

Absolute Maximum Ratings (Note 1)

VIN to GND ---------- -0.3V to 30V
All other pins to GND ---------- -0.3V to 6.5V
SW to GND (5ns transient) ---------- -1V to 8V
Junction Temperature (T_J) ---------- -40℃ to 125℃
Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec)---------- 260℃

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 45℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.1		5.7	V
I_{IN}	Input current			4	A
T_A	Ambient temperature range	-40		85	°C
C_{IN}	Input decoupling capacitor, 25-V rating or higher	0.1	1		μF
C_{pmid}	System capacitor, 10-V rating or higher	1	10		μF
C_{bat}	Battery capacitor, 10-V rating or higher	1	10		μF

Electrical Characteristics

(The specifications are at $V_{UVLO\_IN} < V_{IN} < V_{OVP\_IN}$, V_{BAT} =3.6V, T_A = -40°C to +85°C and T_A = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{UVLO_IN}	VIN UVLO	V_{IN} falling	3.7	3.8	3.9	V
	Hysteresis			150		mV
V_{OVP_IN}	VIN OVP threshold	V_{IN} rising	5.7	5.85	6.0	V
	Hysteresis			150		mV
I_{q_IN}	Input quiescent current	V_{IN} =5.0V , V_{BAT} =4.3V EN_CHG=1		250		μA
R_{DSON_IN}	BUS-FET on- resistance	V_{IN} =5.0V, VIN to PMID pin		0.11		Ω
$V_{FWD-BUS}$	BUS-FET forward regulation			50		mV
I_{IN_LIM}	Input current limit	ILIM[1:0]= 00		2.1		A
		ILIM[1:0]= 01		3.0		A
		ILIM[1:0]= 10		4.5		A
		ILIM[1:0]= 11		5.7		A
V_{SCP_PMID}	PMID short circuit protection threshold	PMID falling edge		2.5		V
	Hiccup work time[Note 2]			1.2		ms
	Hiccup wait time[Note 2]			36		ms
BATTERY SECTION						
V_{BAT_POR}	BAT Power-on-reset	V_{BAT} rising			2.6	V
	Hysteresis			180		mV
I_{BAT}	Quiescent current from BAT	Discharge mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=01, EN_BST=1, STD=0		25		μA
		Standby mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=01, EN_BST=1, STD=1		8		μA
		Standby mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=00, EN_BST=0, STD=1		5		μA
		Standby mode, V_{IN} =5V, V_{BAT} =4.5V, EN_CHG=0		0.3		μA
		Charge mode, V_{IN} =5V, V_{BAT} =4.5V, EN_CHG=1		3		μA
CHARGE MANAGEMENT						
V_{TRI}	Trickle charge voltage threshold	V_{BAT} rising, V_{TRI}=2.8V	2.75	2.8	2.85	V
		V_{BAT} rising, V_{TRI}=3.0V	2.95	3.0	3.05	V
	Hysteresis	Reference to V_{TRI}		100		mV
I_{TRI}	Trickle charge current	ITERM[2:0]=000, I_{TRI} =30mA	27	30	33	mA
		ITERM[2:0]=101, I_{TRI} =180mA	162	180	198	mA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	CC current	25°C, I_{CC}=880mA, 01010	-5		+5	%
		From -10°C to 85°C, I_{CC}=880mA	-10		+10	%
		25°C, I_{CC}=1960mA, 10110	-5		+5	%
		25°C, I_{CC}=445mA, 00101	-10		+10	%
V_{CV}	CV voltage	25°C, I_{CC}=880mA, V_{CV}=4.2V	-0.35		0.35	%
		From -10°C to 85°C, I_{CC}=880mA, V_{CV}=4.2V	-0.6		0.6	%
		25°C, I_{CC}=880mA, V_{CV}=4.35V	-0.35		0.35	%
		25°C, I_{CC}=880mA, V_{CV}=4.4V	-0.35		0.35	%
V_{RECHG}	Re-charge threshold	V_{BAT} falling, Reference to CV voltage		-150		mV
t_{drechg}	Recharge deglitch time[Note 2]			100		us
I_{TERM}	Charge termination current	ITERM[2:0]=000, I_{TRI} =30mA	27	30	33	mA
		ITERM[2:0]=101, I_{TRI} =180mA	162	180	198	mA
t_{dterm}	termination deglitch time[Note 2]			100		us
$I_{swtolinear}$	Switch charge to linear charge current threshold in CV[Note 2]	V_{IN} =5.0, CV=4.2V, V_{BAT} =4.2V, I_{CC}=880mA, I_{TERM}=180mA,		200		mA
$t_{dswtolinear}$	Switch mode to linear mode deglitch time[Note 2]			30		us
t_{dterm}	Charge cycle termination deglitch time[Note 2]			100		us
V_{PMID_DPM}	PMID dynamic power management threshold	V_{PMID} falling, DPM[1:0]= 10		4.65		V
T_{therm}	Thermal foldback threshold[Note 2]		100	120	140	°C
f_{SW1}	Buck switching frequency	V_{IN} =5.0V , V_{BAT} =3.6V, ICC=880mA		1.4		MHz
R_{DSON_HS}	HS-FET on resistance	V_{BAT} =3.6V, V_{PMID}=5.1V		0.07		Ω
R_{DSON_LS}	LS-FET on resistance	V_{BAT} =3.6V, V_{PMID}=5.1V		0.07		Ω
I_{BUCK_LIM}	Buck HS-FET peak current limit		4	5.5	7	A
BOOST CONVERTER						
V_{PMID}	Boost output voltage accuracy	VBST[2:0]=111 , EN_BST=1, 100mA load at PMID pin	5.05	5.1	5.15	V
I_{BST_LIM}	Boost LS-FET peak current limit		3	4	5	A
I_{BYP_LIM}	Boost HS-FET bypass mode current limit	V_{BAT} =4.2V, V_{PMID}=3.5V		1.6		A
f_{SW2}	Boost switching frequency	V_{BAT} =3.6V, V_{PMID}=5.1V, 500mA		1.0		MHz
V_{BAT_UV}	Battery UVLO	V_{BAT} falling, BAT_UV[2:0]=011, 3.1V		3.1		V
	Hysteresis	V_{BAT} rising		0.2		V
t_{d_BATUV}	BAT_UV deglitch time[Note 2]			30		us

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
NTC MANAGEMENT						
T_{-10}	-10°C threshold	V_{NTC} rising, in % of NTCS	80.4	81.2	81.9	%
	Hysteresis	in % of NTCS		1.5		%
T_0	0°C threshold	V_{NTC} rising, in % of NTCS	72.4	73.3	74.2	%
	Hysteresis	in % of NTCS		1.5		%
T_{10}	10°C threshold	V_{NTC} rising, in % of NTCS	63.3	64.3	65.3	%
	Hysteresis	in % of NTCS		1.5		%
T_{45}	45°C threshold	V_{NTC} falling, in % of NTCS	32.1	32.9	33.7	%
	Hysteresis	in % of NTCS		2		%
T_{60}	60°C threshold	V_{NTC} falling, in % of NTCS	22.5	23.2	23.8	
	Hysteresis	in % of NTCS		2		
ULTRA-LOW QUIESCNET CURRENT LDO						
V_{LDO}	LDO output voltage accuracy	V_{BAT} =3.6V, V_LDO[1:0]=00, 50mA load	2.65	2.68	2.72	V
I_{LDO}	LDO output current capability	V_{BAT} =3.6V, V_LDO[1:0]=00	75	90		mA
LOAD SWITCH (LDSW1, LDSW2)						
I_{PUP}	Load insert detection current	PUP[1:0]=01, 1-μA pull up current, V_{BAT} =3.6V	0.7	1	1.3	uA
V_{INSERT}	Load insert detection threshold	V_{BAT} =3.6V, V_{PMID} =5.1V, No VIN reference to PMID voltage		-0.7		V
t_{dins}	Load insert deglitch time[Note 2]			30		ms
$R_{on,LDSW}$	Rds,on of Load Switch1,2	V_{PMID}=5.1V		350		mΩ
I_{LS_LIM}	Load switch current limit	0℃ to 125℃, EICC=300mA	270	300	330	mA
		0℃ to 125℃, EICC=50mA	45	50	55	mA
I_{LS_LL}	Load switch light load current threshold	EEOC=4m	3	4	5	mA
		EEOC=20mA	15	20	25	mA
t_{dLL}	Load switch light load deglitch time[Note 2]			30		ms
SCL, SDA and IRQb						
V_H	Logic High	in % of LDO	75			%
V_L	Logic Low	in % of LDO			25	%
I_{sink1}	SDA, SCL sink current capability	V_{BAT} =3.6V, V_{PIN}=0.4V	10			mA
I_{sink2}	IRQb sink current capability	V_{BAT} =3.6V, V_{IRQb}=0.4V	0.5			mA
LED1, LED2						
I_{sink3}	LED1, LED2 sink current capability	V_{BAT} =3.6V, V_{PIN}=0.4V	10			mA

Note 2: Not production tested. Guaranteed by design.

Typical Characteristics

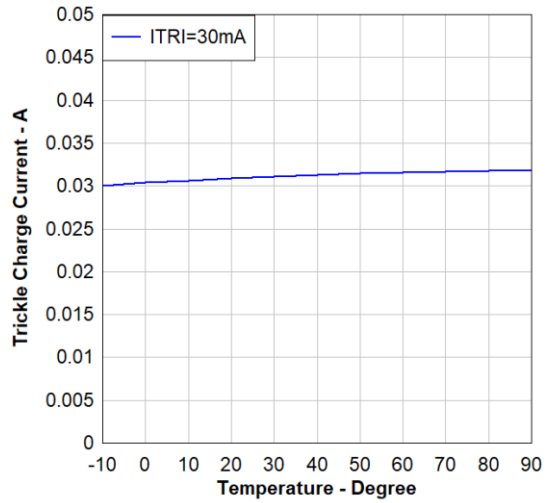


Figure 1. I_{TRI} vs. Ambient Temperature, V_{BAT}=2.5V.

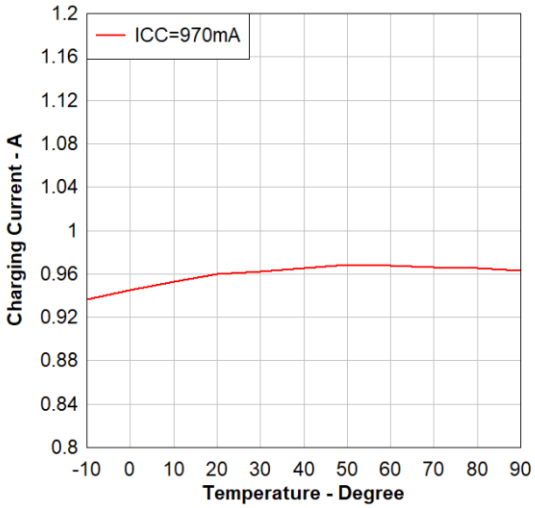


Figure 2. I_{CC} vs. Ambient Temperature, V_{BAT}=3.6V.

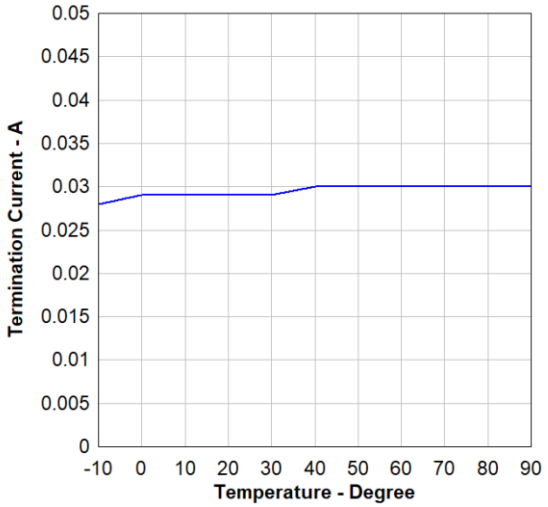


Figure 3. I_{TERM} vs. Ambient Temperature.

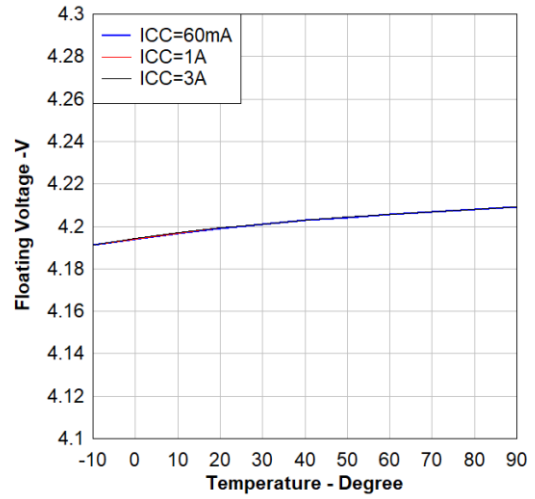


Figure 4. V_{CV} vs. Ambient Temperature, CV=4.2V.

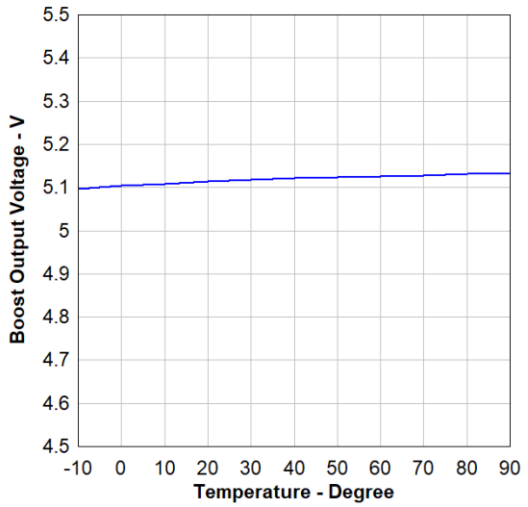


Figure 5. V_{PMID} vs. Ambient Temperature, ENBST=1.

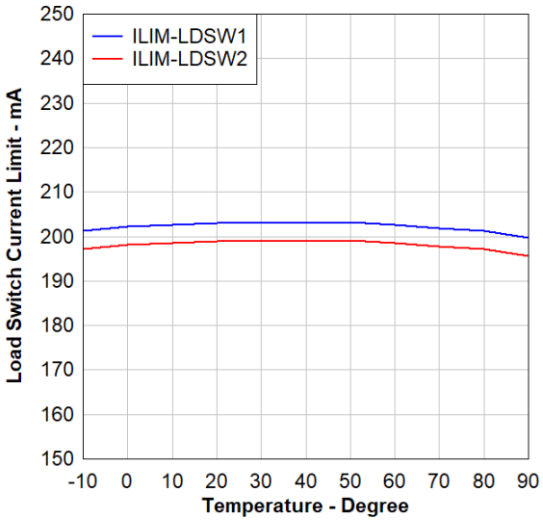


Figure 6. I_{LS_LIM} vs. Ambient Temperature, 200mA.

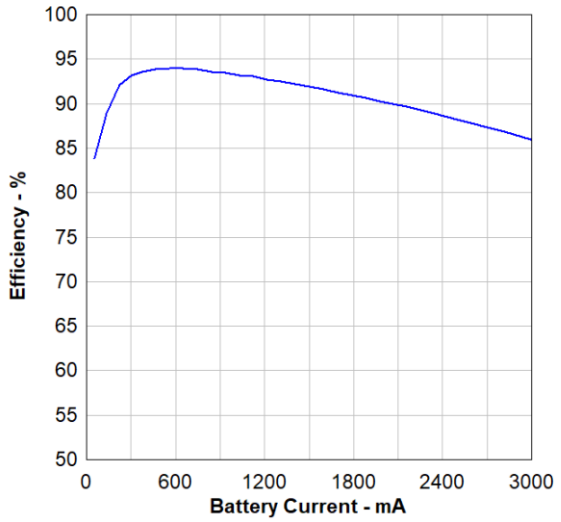


Figure 7. Charger Efficiency. V_{BAT}=3.6V, 1-μH.

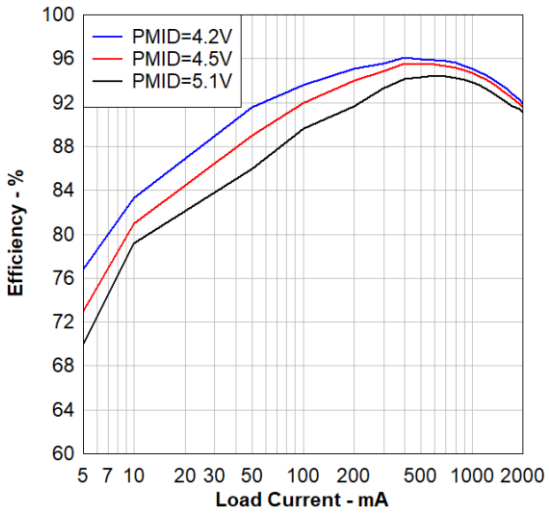


Figure 8. Boost Efficiency. V_{BAT}=3.6V, 1-μH.

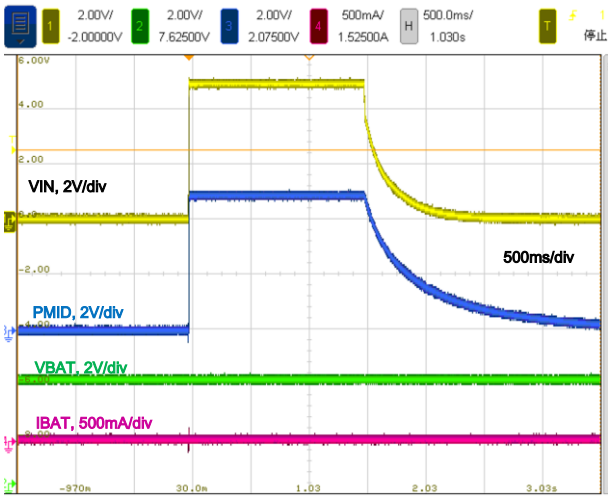


Figure 9. VIN plugged in and unplugged with EN_BST=EN_CHG=0, V_{BAT}=3.6V.

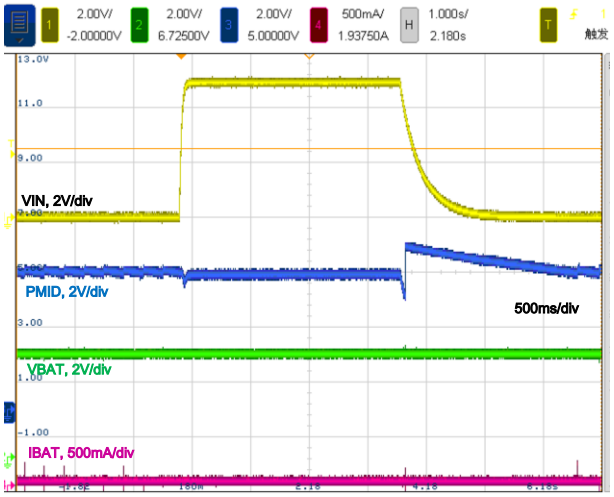


Figure 10. VIN plugged in and unplugged with EN_BST=1, EN_CHG=0, V_{BAT}=3.6V.

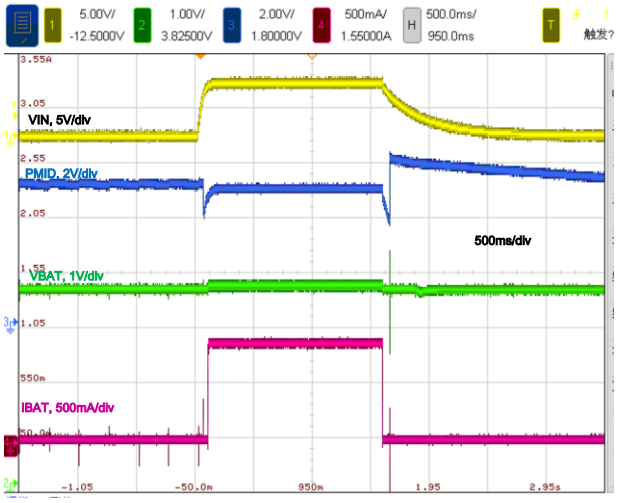


Figure 11. VIN plugged in and unplugged with I_{CC}=880mA, V_{BAT}=3.6V.

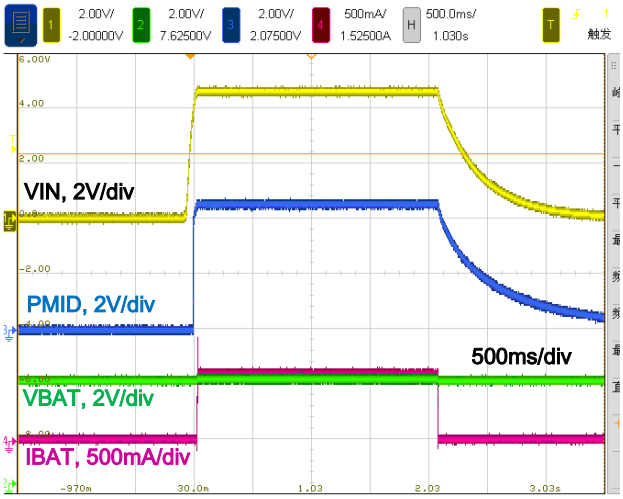


Figure 12. VIN plugged in and unplugged with VIN DPM, I_{CC}=880mA, V_{BAT}=3.6V.

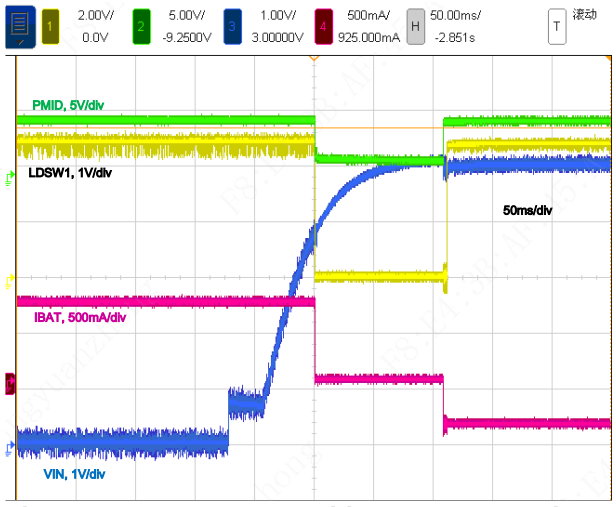


Figure 13. VIN powerup with I_{CC}=370mA and I_{LS}= 500mA, V_{BAT}=3.6V.

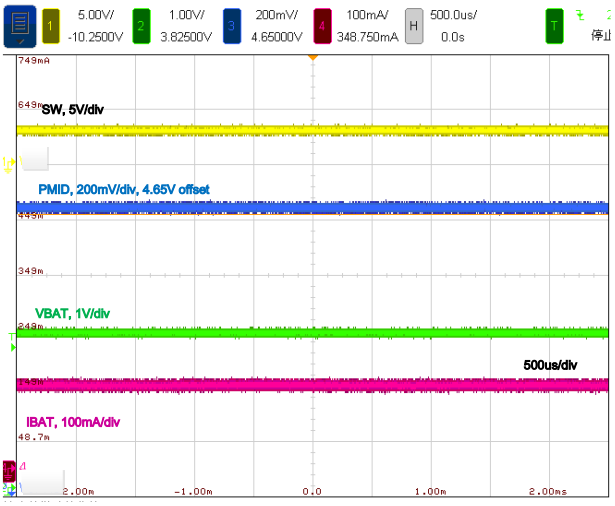


Figure 14. Trickle charge, I_{TRI}=150mA, V_{BAT}=2.8V.

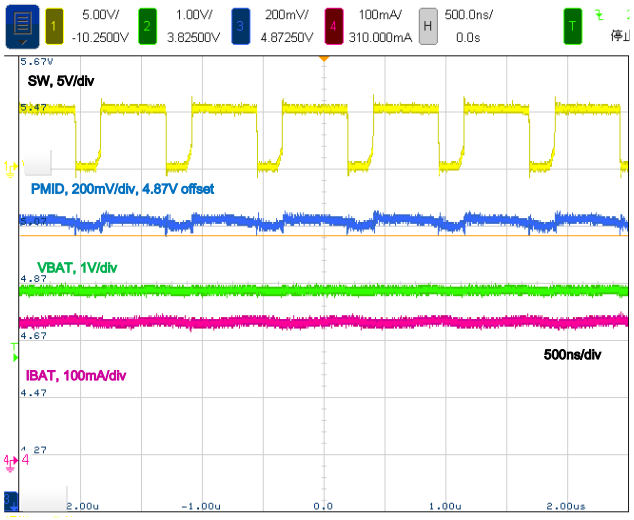


Figure 15. Switch charge, I_{CC}=220mA, V_{BAT}=3.6V.

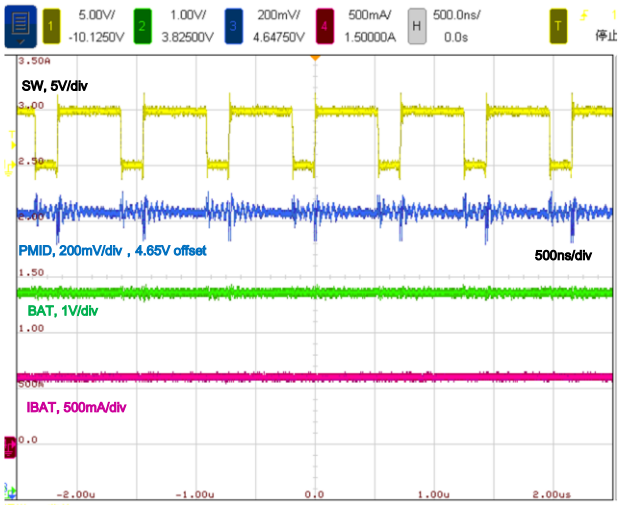


Figure 16. Switch charge, I_{CC}=610mA, VBAT=3.6V.

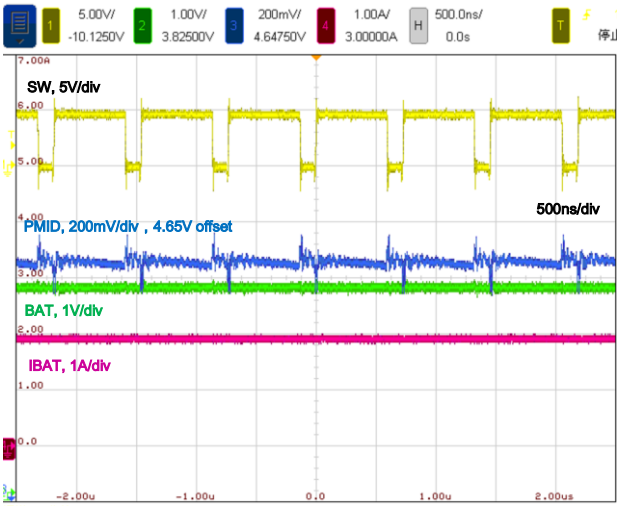


Figure 17. Switch charge, I_{CC}=1870mA, V_{BAT}=3.6V.

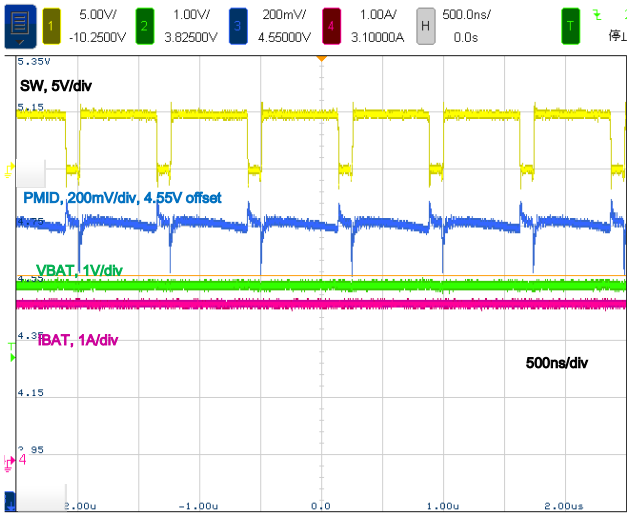


Figure 18. Switch charge, I_{CC}=2680mA, V_{BAT}=3.6V.

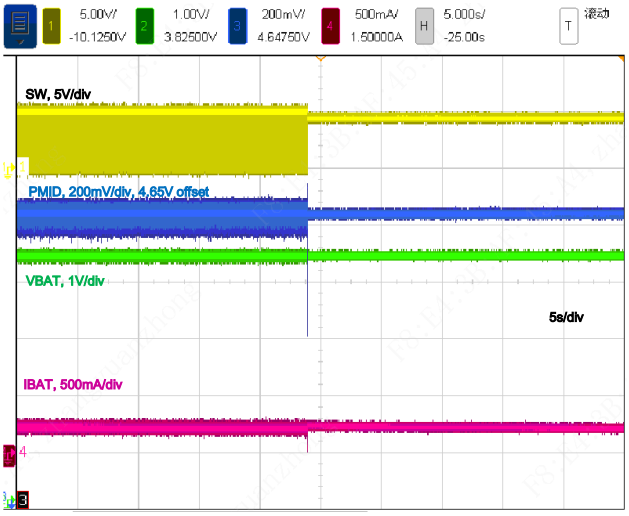


Figure 19. Switch Mode enters linear Mode in CV mode, I_{TERM}=180mA, CV=4.3V.

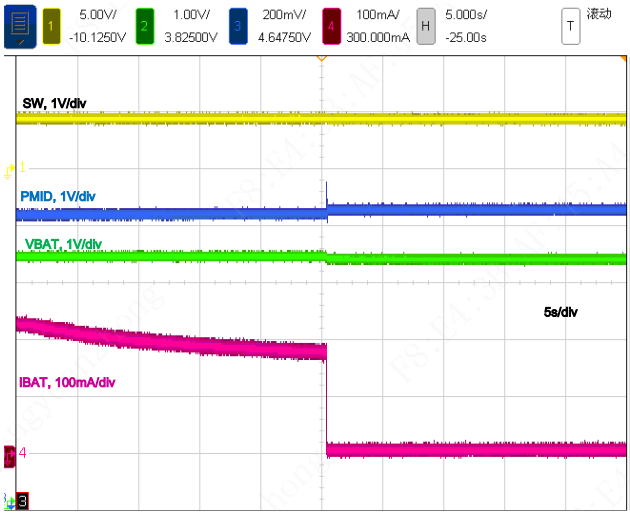


Figure 20. Charge cycle termination, I_{TERM}=180mA, CV=4.3V.

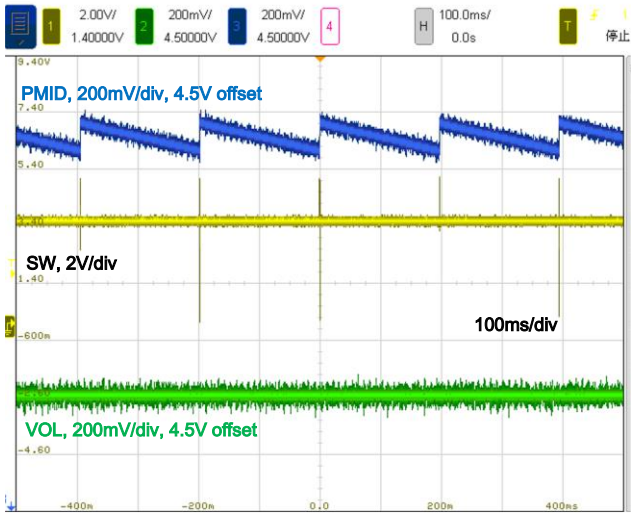


Figure 21. BOOST operation, no load, V_{BAT}=3.8V, V_{PMID}=4.5V.

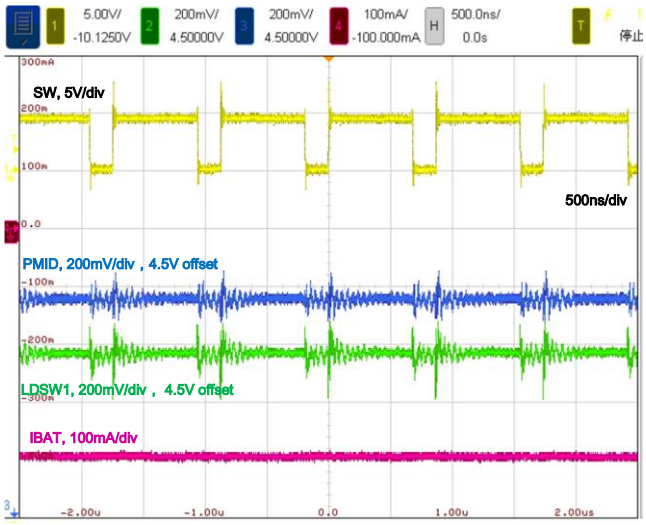


Figure 22. BOOST operation, 300mA load, V_{BAT}=3.8V, V_{PMID}=4.5V.

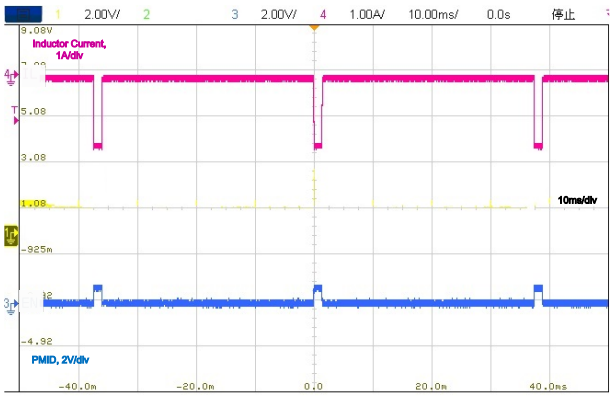
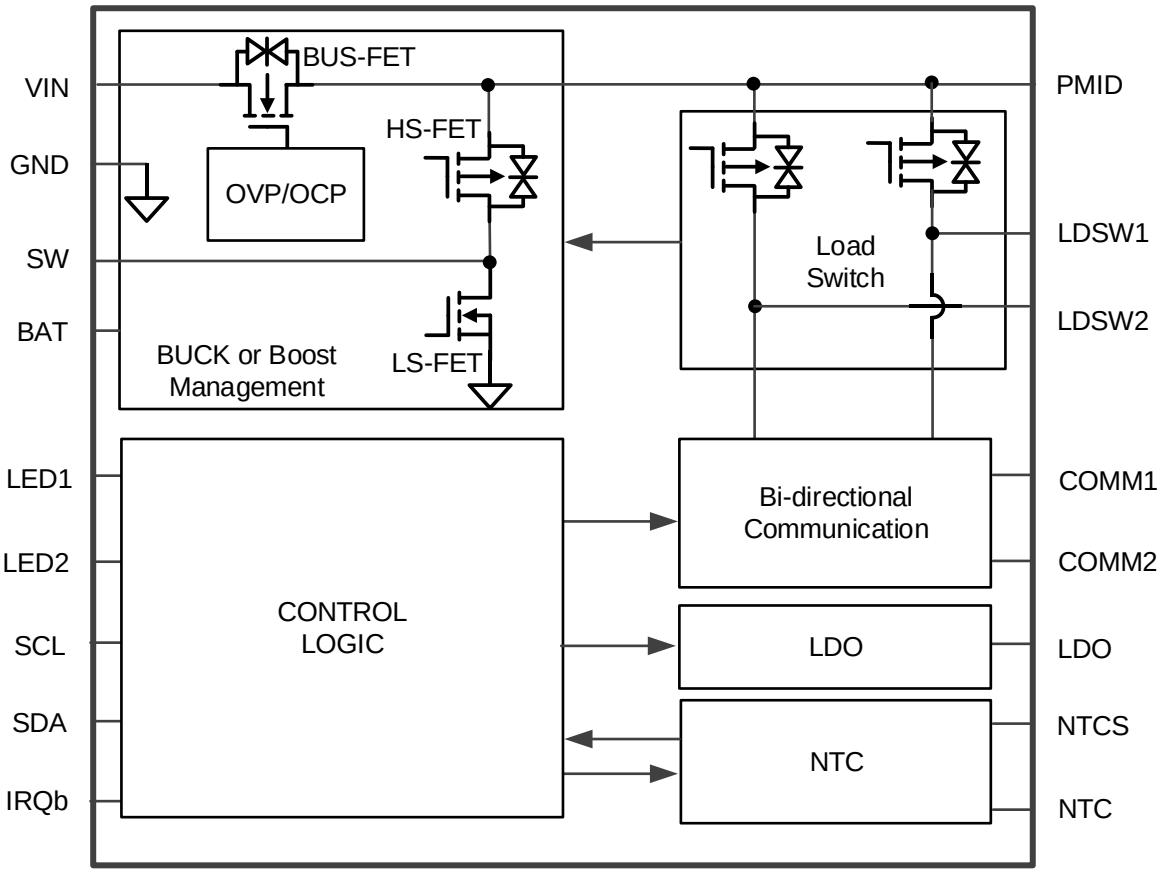


Figure 23. PMID SCP, V_{BAT}=3.8V.

Functional Block Diagram



Detailed Description

Overview

The LP4033 is a fully integrated switch mode charger solution with power path management targeting single-cell Li-ion battery powered portable applications. A low on-resistance BUS-FET is integrated to manage the input power from the VIN pin. The LP4033 offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the VIN input and the battery to meet the system loading needs. A bidirectional buck or boost converter is integrated to manage charging and discharging of the battery. The buck charger supports up to 3-A charging current with up to 95% efficiency. The ultra-low quiescent current boost converter consumes less than 2-μA and supports up to 1.5-A output current. An NTC circuit is offered to manage the temperature range that charging and discharging is allowed. An ultra-low quiescent current LDO is integrated to delivers power to the system that contains an MCU typically. Two load switches provide power from the PMID to the LDSW1 and LDSW2 pins with high accuracy current limit. The load switches support bi-directional communication with the MCU. An I^2C interface enables programming various parameters of charging, discharging, and multiple protection functions. An interrupt output (IRQb) sends a signal to the MCU when an interrupt event happens so the MCU can take actions accordingly.

Multiple features are offered for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), etc. When powered by a battery, LP4033 can operate with only 5-μA current.

Power-on Reset (POR)

The LP4033 performs a POR when either the VIN input voltage or the BAT pin voltage is higher than the $V_{BAT\ POR}$ rising threshold. All registers will be set to default values when performing the POR. Refer to the Register Map section for more register information. The MCU can access all registers after POR.

Input Section

The input section contains the BUS-FET and its control circuitry to realize UVLO, OVP, RCP, ideal diode, current limit, and short-circuit protection functions.

UVLO and OVP

The input section control circuit monitors the VIN-pin voltage to determine when to turn on or off the BUS-FET. The LP4033 detects an over-voltage event when the input voltage is higher than OVP threshold and turns off the BUS-FET immediately. The LP4033 detects an under voltage (UV) event when the input voltage is lower than V_{UVLO_IN} falling threshold.

VIN Power Good (PGD)

When it is between the UVLO and the OVP threshold, the input voltage is in a power-good (PGD) range. The BUS-FET is turned on with a typical 1-ms startup time and the PGD bit of the Status Register 0 is set after a 30-ms deglitch time. If the VIN voltage falls off the PGD range, the BUS-FET is turned off.

Ideal Diode Function with Current Limit

The BUS-FET is controlled as an ideal diode with a 50mV forward regulation and a current limit. When the BUS-FET is turned on, the forward voltage across the BUS-FET will be dependent on the forward current passing through. The BUS-FET is firstly turned on fully so the voltage is the product of the forward current and the R_{DSON_IN} (which is 110mΩ typically). As the forward current reduces, the forward voltage reduces accordingly. As the forward voltage drops to 50mV, a forward-voltage regulation control loop will start to increase the R_{DSON_IN} so the forward voltage remains regulated at 50mV. On the other hand, if it reaches a current limit (programmable with the ILIM[1:0] bits of the Control Register 1, default 5.7A), the forward current will be regulated at the current limit. If the BUS-FET is reversely biased, i.e. the PMID-pin voltage is higher than the VIN-pin voltage, the reverse current is fully blocked.

System SCP

The LP4033 has a system short-circuit protection (SCP) function. When the PMID-pin voltage is pulled lower than 2.5V for 1-ms when PGD bit is 1, the LP4033 enters hiccup mode. Both the BUS-FET, HS-FET and the LS-FET are turned off for 36ms and then the device will try to restart powering up the PMID pin for 1-ms. If the PMID-pin voltage rises above the 2.5V threshold within 1-ms, the hiccup will stop; otherwise, the BUS-FET, HS-FET and the LS-FET will be turned off for 36-ms again and repeat the restart-up.

Charge Management

The LP4033 will charge the battery through the BUCK charger when the PMID-pin voltage is 150mV higher than the battery voltage. The charger operates with three charging modes, i.e., trickle, CC, and CV modes. During trickle charge mode, the LP4033 is a linear charger to achieve high current accuracy. The LP4033 automatically changes from linear charge mode to switch charge mode when the LP4033 exits the trickle charge mode and enters the CC mode. The LP4033 enters linear mode again when the battery is close to be fully charged. A typical charging cycle is shown in Figure 24. The charging currents and CV are programmable by I²C. The EN_CHG bit of Control Register 3 can enable the charger. The following describes the details of the charging operation.

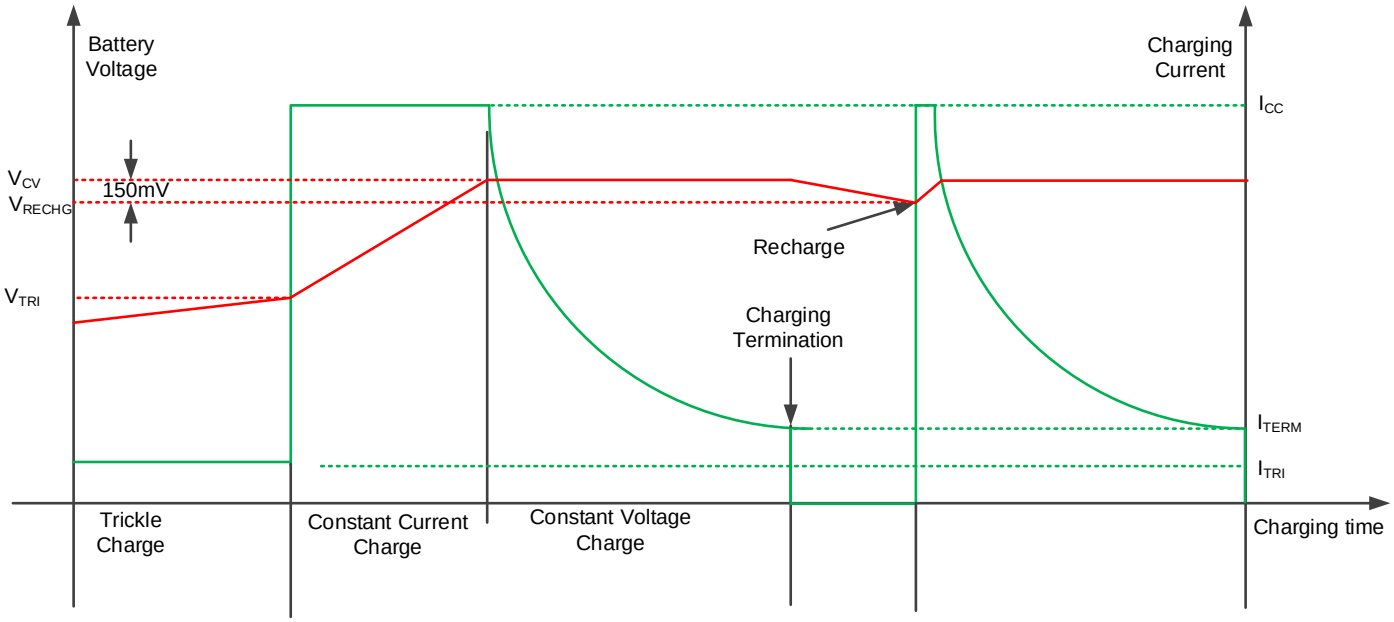


Figure 24. 5V normal charging profile

Start of a Charge Cycle

The charger can be in a charge cycle when all the conditions below are valid,

- PGD = 1
- EN_CHG = 1
- The NTC-pin voltage is in the range of T_0 and T_{45} given in the Electrical Characteristics table.

A new charge cycle will start when the last of the above conditions change from invalid to valid. For example, when the NTC-pin voltage and the PGD are valid when the EN-CHG bit is set.

Trickle Mode

The charger enters the trickle mode at the beginning of a charge cycle if the battery voltage is below the trickle-charge voltage threshold (V_{TRI}) that is programmable via the VTRI bit of the Control Register 2. The default value is 3.0V. The trickle-charge current is programmable with the ITRI[1:0] bits of the Control Register 1. The LP4033 is a linear mode charger when the battery voltage is below the V_{TRI}.

CC Mode

The LP4033 starts the CC mode when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The charging current is determined by the ICC[4:0] bits of the Control Register 0. The CC current is programmable from 55~2910mA and the LP4033 works in switch mode all the time. The default charging current is 370mA.

CV Mode

The LP4033 starts the CV mode when the battery voltage reaches the CV threshold. The charging current decreases gradually until the charging termination is triggered in this mode. The CV voltage is programmable via the BAT_CV[2:0] bits of the Control Register 0. The default value is 4.2V.

The LP4033 still operates in switch mode at the beginning of CV mode, when the charging current decreases to less

than 200mA for 32-μs deglitch time, determined by the ITERM[1:0] bits of the Control Register 1, the LP4033 changes to linear charge mode again. LP4033 stays in linear charge mode until the charge cycle termination is triggered.

Charge Cycle Termination

When the BAT voltage is higher than the recharge voltage and the charging current drops to the termination current threshold, the charging termination is triggered. The charging is terminated immediately and the CHG bit of the Status Register0 is set to 0.

Recharge

A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage while the VIN voltage is still present after a typical 100-μs deglitch time. The LP4033 works in switch mode again at the beginning of recharge cycle.

Charge Current Thermal Foldback

When the die temperature reaches 120 ºC, the charging current decreases to prevent further temperature rise.

NTC Management

An NTC resistor with 1% accuracy and a beta of 3435 is recommended for LP4033. The NTC resistor is enabled by the STD bit with its default value of 0. The NTCS and the internal NTC detection circuitry are disabled when STD is set to 1 to reduce the quiescent current.

Three temperature detecting thresholds are provided when charging, i.e., T_0, T_{10}, and T_{45}. An NTC interrupt pulse will be sent when the temperature is crossing these thresholds. The charging is terminated when the temperature range is out of T_0 - T_{45}.

The NTC [2:0] bits are used to indicate the temperature range in the Status Register 0. The MCU can change the charging parameters or disable the charging operation by using the control registers.

The NTC[2:0] will be set to 011 when STD is set to 1.

Battery Voltage Monitor

A 4-bit ADC to monitor the battery voltage is offered in the LP4033. The ADC samples the battery voltage every 100-ms and the battery voltage range is shown in the V_BATM[3:0] bits of the Status Register 1. The V_BATM[3:0] can be used in a software gauge. The ADC is always-on until both the VIN and BAT falls below the POR thresholds.

EN_CHG Bit

EN-CHG bit can enable the charger. When EN_CHG is set to 0, the charging cycle is terminated immediately. When EN_CHG is set to 1 from 0, a new charging cycle starts again. The default value of EN_CHG bit is 0.

As a recommendation, the EN_CHG should be written to 0 after every termination and only written to 1 with a typical 1-s delay time after the PGD changes from 0 to 1.

Power Path Management

The LP4033 integrates the power path management function. The PMID pin can be powered from the input voltage, the battery under different scenarios.

Dynamic Power Management

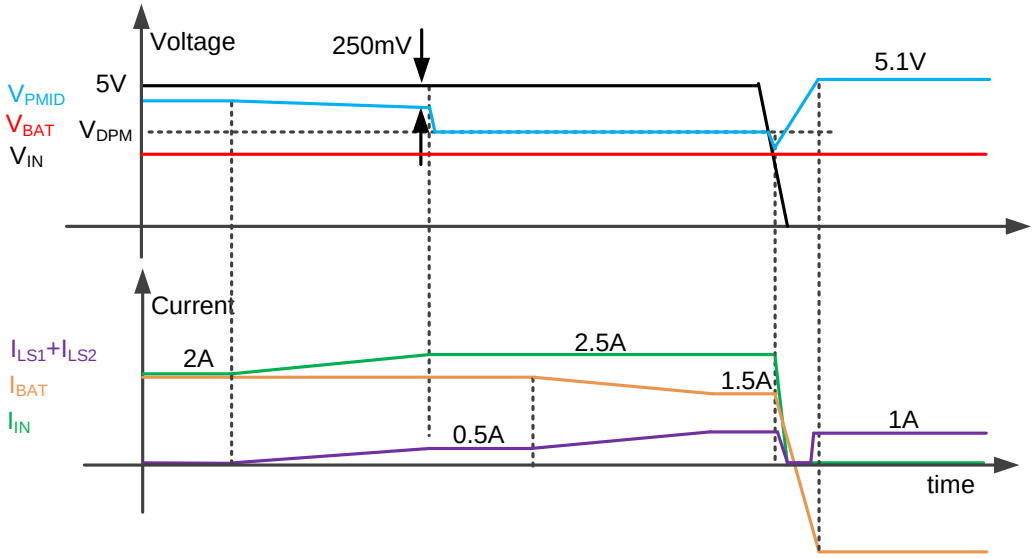


Figure 25. Dynamic power management

The voltage at the PMID pin and currents through the BUS-FET is monitored continuously when the LP4033 is powered. The minimum PMID-pin voltage is set by the DPM[1:0] bits of the Control Register 6. When the PMID-pin voltage drops (due to the load increase at load switches' pins) to the voltage set by the DPM[1:0] bits , the charging current is reduced to prevent the PMID-pin voltage from dropping further until a new balance is reached.

The battery will start providing current if the VIN drops to the V_{UVLO_IN} falling threshold, in which case the HS-FET and LS-FET are controlled as a boost converter. The Figure 25 shows the operation of the dynamic power management. When the input power is removed, the system is powered from the battery only.

Boost converter

When the input power is removed, the HS-FET and LS-FET are controlled as a boost converter with up to 1.5A output current capability. The quiescent current of the boost converter is only 2-μA from the battery when there is no load sink by the load switches.

Boost Converter Operation

The boost regulator has two operation modes. It operates in the voltage step-up mode when the PMID voltage is required to be higher than the battery voltage. It operates in a by-pass mode when the PMID voltage is required to be lower or equal to the battery voltage. The maximum output voltage of the boost converter is programmable by the VBST[2:0] bits of the Control Register 2. The range is between 4.2V- 5.1V.

Feedback selection

The higher voltage of the LDSW1 and LDSW2 will be selected to set the reference for the PMID output, however, when either LDSW1 or LDSW2 channel is not needed, that channel of feedback can be disconnected. The disconnection can be performed by setting FBK_L1 or FBK_L2 bit to 0. The PMID is regulated at a voltage setting by the VBST[2:0] when both the FBK_L1 and FBK_L2 bit are set to 0.

Current Limit and Hiccup Operation

The current flow the HS-FET of the boost regulator is limited to 3A when the PMID is overloaded or short to ground. The LP7810A shuts down the boost converter if the overload condition lasts 1.2-ms typical time and the PMID_OL bit will be set when 1.2-ms expires. After a 36-ms hiccup time, the boost converter will perform a new startup with typical 200-μs soft-start time.

The boost converter can be enabled by the EN_BST bit of the Control Register 3.

LDO

The LP4033 integrates an ultra-low quiescent current linear regulator that is powered by either the VIN or the BAT pin. This output is to power the external MCU, the NTC circuit, the internal logic circuit, and the communication circuit. A 0.1~0.47-μF external ceramic capacitor is required. The LDO output voltage is programmable by the V_LDO[1:0] bits of the Control Register 3 from 1.8V to 3.3V.

The LDO is always on.

Load switches

The LP4033 offers two independent load switches LDSW1 and LDSW2 with 300mΩ on-resistance power FETs. Both the load switches are powered by the PMID and the current limit is programmable from 10mA to 600mA with minimum 10mA/step by the EICC[4:0] bits of the Control Register 5.

Device insert and removal

The load switches support device insert and removal detection. Both the LDSW1 and LDSW2 are pulled to the PMID or BAT with a weak current source, which is programmable by the PUP[1:0] bits of the Control Register 5. The LDSW1 and LDSW2 has the same voltage level of PMID or BAT when there is nothing connected to the LDSW1 and LDSW2. When the LDSW1/2 pin is pulled 0.7-V lower than the maximum voltage of PMID and BAT pin because of the device insert, the L1_INS or the L2_INS bit is set to 1 and an interrupt is sent and the MCU can enable the load switches to power the loads. When the load current at each switch is reduced to less than 4mA or 20mA which is set via the register EEOC bit as well, the EOC_L1 bit or EOC_L2 bit is set to 1 and the interrupt is sent to MCU and the MCU can decide whether to cutoff the power to the load. When the peripheral device is removed from the LDSW1 or the LDSW2 pin, the LDSW1 or the LDSW2 voltage recovers to the level same as the PMID voltage, the L1_INS bit or the L2_INS is set to 0 and the interrupt is sent to the MCU again.

Load switch current limit

The load switches support current limit by configuring the EICC[4:0] bits of the Control Register 6. The LP4033 supports two modes, the low-voltage dropout mode and the normal mode.

When the FBK_L1 is enabled, the voltage drop between the PMID and LDSW1 is only 150mV and the system efficiency is improved compared with the traditional 5.1V constant output at the PMID pin. This is the low-voltage dropout mode. The maximum current for the each peripheral device connected at LDSW1 and LDSW2 is 400mA in this mode.

In normal mode, the boost converter output is fixed at 5.1V or 4.8V and set the FBK_L1 and FBK_L2 to 0 at the same time. The load switches support up to 600mA current capability when the voltage drop between the PMID and LDSW1/2 are higher than 250mV.

Battery under-voltage lockout (BAT_UV)

The LP4033 integrates battery over discharge protection as well. Discharge will stop when the battery voltage drops below the BAT_UV[2:0] bits of the Control register 2, which is programmable between 2.8V - 3.5V. Both the LDSW1 and LDSW2 are turned off to prevent the battery voltage from further decrease.

Bi-directional Communication

Another two communication interfaces (COMM1/COMM2) are combined with the load switches (LDSW1/LDSW2) and the MCU can send to or receive the signals from the peripheral devices independently as shown in the Figure 26. The L1_TX bit enables the signal transfer from the COMM1 to the LDSW1 while the L1_RX bit enables the signal transfer reversely. The L1_PUP bit enables the pull-up resistor when communication is needed. All these 3 bits should be set to 0 to save quiescent current when no communication is on-going.

The capacitance at the LDSW1/2 nodes is critical for communication speed. For a typical 115200bps UART communication, 1-nF capacitor is allowed. The capacitor can be higher than 1-μF if no communication at LDSW1/2 pins.

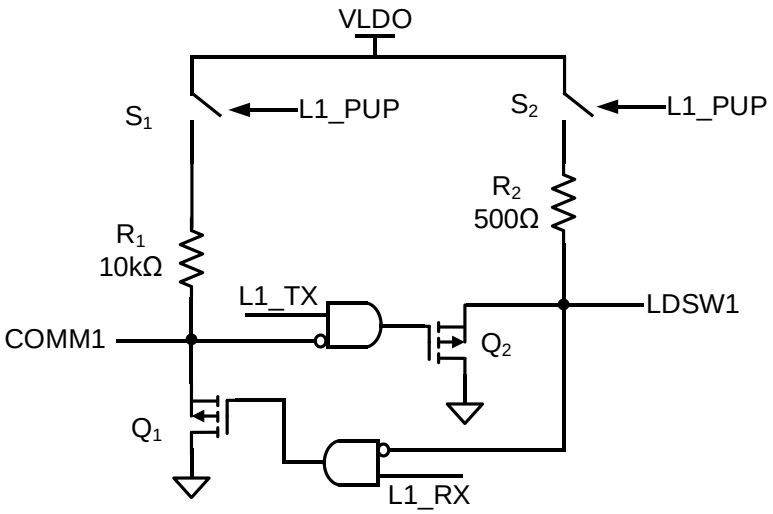


Figure 26. Communication Diagram (LDSW1 channel)

Load switch SCP

The LP4033 integrates short circuit protection as well. The L1_SCP bit and the L2_SCP bit of the Status Register 1 is set to 1 and the interrupt is sent to the MCU when the LDSW1 or LDSW2 voltage falls below 1V. The MCU can take actions accordingly.

NTC Management

Two temperature detecting thresholds are provided when the battery is discharging, i.e., T_{-10} and T_{60}. An NTC interrupt pulse will be sent when the temperature is crossing these thresholds. The load switches are terminated when the temperature range is out of T_{-10} - T_{60}.

LED Outputs

Two LED outputs are offered that can be controlled by the I2C bus. Each pin has 10mA current capability.

The LED1/2 outputs support breathing mode when the LED1[1:0] or the LED2[1:0] in the register 0CH is set to 10. The breathing frequency is fixed at 0.5Hz with 100Hz resolution.

The LED outputs support flash mode as well with a typical 2Hz flash when the LED1/2 register is set to 11.

Minimum Operating Current

When powered by the battery alone, the LP4033 can minimize its operating current by setting the LP4033 in the standby mode (STD = 1) and disabling the charger, the boost converter and the load switches (EN_BST =EN_CHG=EN_L1=EN_L2= 0, PUP[1:0]=00) at the same time. The LP4033 only consumes 5-μA quiescent current with such configuration. The ADC monitoring the battery voltage, the LDO and the I2C registers are still active.

Thermal Shutdown

When the internal junction temperature of LP4033 exceeds the thermal shutdown threshold of 150 ºC, the LP4033 disables all the power paths. The LP4033 will not reset the registers and recovers to the default setting after the junction temperature falls to the 130 ºC .

I²C Bus and Interrupt

The LP4033 has an I²C bus and the interrupt IRQb pin. The LP4033 operates as a slave device with an address of 6BH (7bit, 1101011). A 1 or 0 should be placed at the end of the address that represents read or write operation. The LDO is the power supply of the internal I2C circuits. The SDA and SCL are both pulled up to the LDO with 5.1-kΩ resistor. The IRQb is pulled up to the LDO with 1-MΩ resistor.

Interrupt

The interrupt pin IRQb pulls to low when an interrupt event happens in the chip. Those events include,

- Input power attaching or removal
- PMID pin shorting to GND
- LP4033 starting to charge the battery
- The charging is terminated
- Battery voltage falling below the UVLO threshold
- Temperature sensed by the NTC circuit crossing thresholds
- Peripheral device is connected to LDSW1/LDSW2
- Peripheral device is removed
- Peripheral device current is less than EEOC
- LDSW1 or LDSW2 pin shorting to GND
- Any one channel of the LDSW1/2 is short circuit.
- Thermal shutdown

The interrupt events can be masked by the control bits in the Interrupt Mask Register 0 and 1. The IRQb pin recovers to high when the MCU read the interrupt registers.

I²C DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

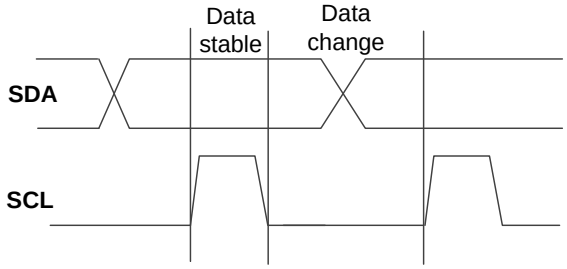


Figure 27. I²C Data validity

I²C Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the SDA line while the SCL is high means a Start condition. A rising edge on the SDA line while the SCL is at high means a Stop condition.

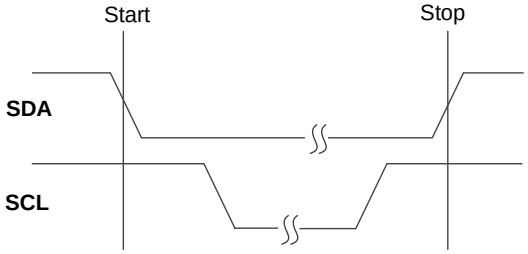


Figure 28. I²C Start and Stop Conditions

I²C Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

Single Byte Read and Write

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 29. Single-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK
							8 bit	1bit	1bit
							Data from Address	NACK	STOP

Figure 30. Single-byte Read

Multi-Read and Multi-Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit							
START	Slave address	0	ACK	Register address	ACK	START							
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit		
				Data to Address	ACK	Data to Address	ACK	.....	Data to Address	ACK	stop		

Figure 31. Multi-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit					
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1					
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit		
				Data from Address	ACK	Data from Address	ACK	.....	Data from Address	NACK	stop		

Figure 32. Multi-byte Read

Register Map

Table 1. Device Registers

Register Name	Address	Read/ Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status rgister 0	00H	RO	NTC	NTC	NTC	PMID_OL	EOC_L2	EOC_L1	CHG	PGD
Status register 1	01H	RO	L1_SCP	L2_SCP	L1_INS	L2_INS	V_BATM	V_BATM	V_BATM	V_BATM
Interrupt register 0	02H	RC	Reserve	Reserve	iRem_L2	iRem_L1	iSCP_L2	iSCP_L1	iBAT_UV	iTSD
Interrupt register 1	03H	RC	iINS_L2	iINS_L1	iEOC_L2	iEOC_L1	iPMID_OL	iNTC	iCHG	iPGD
Mask register 0	04H	RW	Reserve	Reserve	mRem_L2	mRem_L1	mSCP_L2	mSCP_L1	mBAT_UV	mTSD
Mask register 1	05H	RW	mINS_L2	mINS_L1	mEOC_L2	mEOC_L1	mPMID_OL	mNTC	mCHG	mPGD
Control register 0	06H	RW	BAT_CV	BAT_CV	BAT_CV	ICC	ICC	ICC	ICC	ICC
Control register 1	07H	RW	ILIM	ILIM	ITERM	ITERM	ITERM	ITRI	ITRI	ITRI
Control register 2	08H	RW	BYP	BAT_UV	BAT_UV	BAT_UV	VBST	VBST	VBST	VTRI
Control register 3	09H	RW	V_LDO	V_LDO	FBK_L2	FBK_L1	EN_L2	EN_L1	EN_BST	EN_CHG
Control register 4	0AH	RW	Reserve	L2_PUP	L1_PUP	VSEL	L2_RX	L1_RX	L1_TX	L1_TX
Control register 5	0BH	RW	PUP	PUP	EEOC	EICC	EICC	EICC	EICC	EICC
Control register 6	0C	RW	STD	DPM	DPM	LED2	LED2	LED1	LED1	POR

Note: **RO**: read only; **RC**: read and clear; **RW**: read and write

Status Register 0 /Address: 00H (default: 0x6C)

Table 2. Status Register 0

Bit	Symbol	Description	Read/Write	Default
7	NTC[2]	000: <-10 ˚C , 001: -10~0 ˚C,	RO	0
6	NTC[1]	010:0-10 ˚C, 011: 10~45 ˚C,	RO	1
5	NTC[0]	100: 45~60 ˚C, 101: >60 ˚C ,110/111: not valid.	RO	1
4	PMID_OL	=1 PMID is over-loaded.	RO	0
3	EOC_L2	=1 LDSW2 current is less than EEOC current threshold.	RO	1
2	EOC_L1	=1 LDSW1 current is less than EEOC current threshold.	RO	1
1	CHG	=1 when charger is in trickle, CC, or CV mode.	RO	0
0	PGD	=1 $V_{UVLO\_IN} < V_{IN} < V_{OVP\_IN}$.	RO	0

Status Register 1 /Address: 01H (default: 0x00)

Table 3. Status Register 1

Bit	Symbol	Description	Read/Write	Default
7	L1_SCP	1: LDSW1short circuit.	RO	0
6	L2_SCP	1: LDSW2short circuit.	RO	0
5	L1_INS	1: LDSW1 load insertion.	RO	0
4	L2_INS	1: LDSW2 load insertion.	RO	0
3	V_BATM[3]	0000:<2.9V, 0001:3.0V, 0010:3.1V, 0011:3.2V,	RO	0
2	V_BATM[2]	0100:3.3V, 0101:3.4V, 0110:3.5V, 0111:3.6V,	RO	0
1	V_BATM[1]	1000:3.7V, 1001:3.8V, 1010:3.9V, 1011:4.0V,	RO	0
0	V_BATM[0]	1100:4.1V, 1101:4.2V, 1110:4.3V, 1111:>4.4V.	RO	0

Interrupt Register 0/Address: 02H (default: 0x00)

Table 4. Interrupt Register 0

Bit	Symbol	Description	Read/Write	Default
5	iREM_L2	LDSW2 load removal interrupt.	RC	0
4	iREM_L1	LDSW1 load removal interrupt.	RC	0
3	iSCP_L2	LDSW2 load short circuit interrupt.	RC	0
2	iSCP_L1	LDSW1 load short circuit interrupt.	RC	0
1	iBAT_UV	Battery UVLO protection interrupt.	RC	0
0	iTSD	Thermal shutdown interrupt.	RC	0

Interrupt Register 1/Address: 03H (default: 0x00)

Table 5. Interrupt Register 0

Bit	Symbol	Description	Read/Write	Default
7	iINS_L2	LDSW2 load insert interrupt.	RW	0
6	iINS_L1	LDSW1 load insert interrupt.	RW	0
5	iEOC_L2	LDSW2 light load interrupt.	RW	0
4	iEOC_L1	LDSW1 light load interrupt.	RW	0
3	iPMID_OL	PMID overload interrupt.	RW	0
2	iNTC	NTC cross range or thermal shutdown.	RW	0
1	iCHG	Charging status change.	RW	0
0	iPGD	Input voltage status change.	RW	0

Interrupt Mask Register 0/Address: 04H (default: 0x00)

Table 6. Interrupt Mask Register 0

Bit	Symbol	Description	Read/Write	Default
5	mREM_L2	Mask Interrupt.	RW	0
4	mREM_L1		RW	0
3	mSCP_L2		RW	0
2	mSCP_L1		RW	0
1	mBAT_UV		RW	0
0	mTSD		RW	0

Interrupt Mask Register 1/Address: 05H (default: 0x00)

Table 7. Interrupt Mask Register 1

Bit	Symbol	Description	Read/Write	Default
7	mINS_L2	Mask interrupt.	RW	0
6	mINS_L1		RW	0
5	mEOC_L2		RW	0
4	mEOC_L1		RW	0
3	mPMID_OL		RW	0
2	mNTC		RW	0
1	mCHG		RW	0
0	mPGD		RW	0

Control Register 0/Address: 06H (default: 0x44)

Table 8. Control Register0

Bit	Symbol	Description	Read/Write	Default
7	BAT_CV[2]	Constant voltage set:	RW	0
6	BAT_CV[1]	000: 4.0V 001:4.1V 010:4.2V 011:4.3V,	RW	1
5	BAT_CV[0]	100: 4.35V 101:4.38V 110:4.4V 111:4.44V.	RW	0
4	ICC[4]	Constant charge current set: 00000:55mA,00001:140mA,00010:220mA,00011:295mA,	RW	0
3	ICC[3]	00100:370mA,00101:445mA,00110:520mA,00111:610mA, 01000:700mA,01001:790mA,01010:880mA,01011:970mA,	RW	0
2	ICC[2]	01100:1060mA,01101:1150mA,01110:1240mA,01111:1330mA, 10000:1420mA,10001:1510mA,10010:1600mA,10011:1690mA,	RW	1
1	ICC[1]	10100:1780mA,10101:1870mA,10110:1960mA, 10111:2050mA,11000:2140mA,11001:2230mA,	RW	0
0	ICC[0]	11010:2320mA, 11011:2410mA, 11100:2500mA, 11101:2590mA,11110:2680mA, 11111:2910mA.	RW	0

Control Register 1/Address: 07H (default: 0XC0)

Table 9. Control Register1

Bit	Symbol	Description	R/W	Default
7	ILIM[1]	Input current limit set:00: 2.1A, 01:3.0A,	RW	1
6	ILIM[0]	10: 4.5A, 11: 5.7A.	RW	1
5	ITERM[2]	Termination current set:	RW	0
4	ITERM[1]	000:30mA, 001:60mA, 010:90mA, 011:120mA,	RW	0
3	ITERM[0]	100:150mA, 101:180mA, 110~111: not valid.	RW	0
2	ITRI[2]	Trickle charge current set:	RW	0
1	ITRI[1]	000:30mA, 001:60mA, 010:90mA, 011:120mA,	RW	0
0	ITRI[0]	100:150mA, 101:180mA, 110~111: not valid.	RW	0

Control Register 2/Address: 08H (default: 0X3F)

Table 10. Control Register2

Bit	Symbol	Description	R/W	Default
7	BYP	1: Load switches(LDSW1/2) enter bypass mode, 0: normal.	RW	0
6	BAT_UV[2]	Boost UVLO set(Falling edge):	RW	0
5	BAT_UV[1]	000:2.8V, 001:2.9V, 010:3.0V, 011:3.1V,	RW	1
4	BAT_UV[0]	100:3.2V,101:3.3V, 110:3.4V, 111:3.5V.	RW	1
3	V_BST[2]	Boost output voltage set:	RW	1
2	V_BST[1]	000:4.2V, 001:4.3V, 010:4.4V, 011:4.5V,	RW	1
1	V_BST[0]	100:4.6V,101:4.7V, 110:4.8V, 111:5.1V.	RW	1
0	VTRI	Trickle charge voltage set: 1: 3.0V, 0:2.8V.	RW	1

Control Register 3/Address: 09H (default: 0X30)

Table 11. Control Register3

Bit	Symbol	Description	R/W	Default
7	V_LDO[1]	Ultra-low quiescent current LDO output voltage set:	RW	0
6	V_LDO[0]	00: 2.7V, 01:1.8V, 10:3.0V, 11:3.3V.	RW	0
5	FBK_L2	1: LDSW2 voltage is sampled for PMID voltage control.	RW	1
4	FBK_L1	1: LDSW1 voltage is sampled for PMID voltage control.	RW	1
3	EN_L2	1: LDSW2 enable.	RW	0
2	EN_L1	1: LDSW1 enable.	RW	0
1	EN_BST	1: Boost regulator enable.	RW	0
0	EN_CHG	1: Charge enable.	RW	0

Control Register 4/Address: 0AH (default: 0X00)

Table 12. Control Register4

Bit	Symbol	Description	R/W	Default
7	Reserve		RW	0
6	L2_PUP	1: LDSW2 communication pull-up enabled.	RW	0
5	L1_PUP	1: LDSW1 communication pull-up enabled.	RW	0
4	VSEL	Pull-up bias voltage when communication: PMID or LDO voltage, 0 = LDO, 1=PMID.	RW	0
3	L2_RX	1: LDSW2 receive data enable.	RW	0
2	L1_RX	1: LDSW1 receive data enable.	RW	0
1	L2_TX	1: LDSW2 transmit data enable.	RW	0
0	L1_TX	1: LDSW1 transmit data enable.	RW	0

Control Register 5/Address: 0BH (default: 0X44)

Table 13. Control Register5

Bit	Symbol	Description	R/W	Default
7	PUP[1]	Pull up current for load insert detection:	RW	0
6	PUP[0]	00: off, 01: 1uA, 10: 7uA, 11: 20Ua.	RW	1
5	EEOC	Load switch light load current threshold set: 0: 4mA or 1:20mA.	RW	0
4	EICC[4]	High accuracy load switch current limit set: 00000:10mA, 00001:20mA, 00010:30mA,	RW	0
3	EICC[3]	00011:40mA, 00100:50mA, 00101:60mA, 00110:70mA, 00111:80mA,01000:90mA,01001:100mA, 01010:110mA,	RW	0
2	EICC[2]	01011:120mA, 01100:130mA, 01101:140mA, 01110:160mA 01111:180mA,10000:200mA, 10001:220mA, 10010:240mA,	RW	1
1	EICC[1]	10011:260mA,10100:280mA,10101:300mA, 10110:320mA, 10111:340mA, 11000:360mA, 11001:380mA, 11010:400mA,	RW	0
0	EICC[0]	11011:420mA,11100:460mA, 11101:500mA, 11110:550mA, 11111:600mA, 00000~11010 is available when FBKL1=FBKL2=1; 00000~11111 is available when FBKL1=FBKL2=0.	RW	0

Control Register 6/Address: 0CH (default: 0X41)

Table 14. Control Register6

Bit	Symbol	Description	R/W	Default
7	STD	1: LP4033 enters standby mode.	RW	0
6	DPM[1]	PMID DPM threshold voltage set:	RW	1
5	DPM[0]	00:4.45V 01:4.55V, 10:4.65V, 11:4.75V.	RW	0
4	LED2[1]	00: LED2=OFF; 01: LED2=ON,	RW	0
3	LED2[0]	10: LED2 breathing 100Hz, 11: LED2 flash.	RW	0
2	LED1[1]	00: LED1=OFF; 01: LED1=ON,	RW	0
1	LED1[0]	10: LED1 breathing 100Hz, 11: LED1 flash.	RW	0
0	POR	1: power on reset indication, MCU should write to 0 after POR. Write 1 to this bit is not valid.	RW	1

Application Information

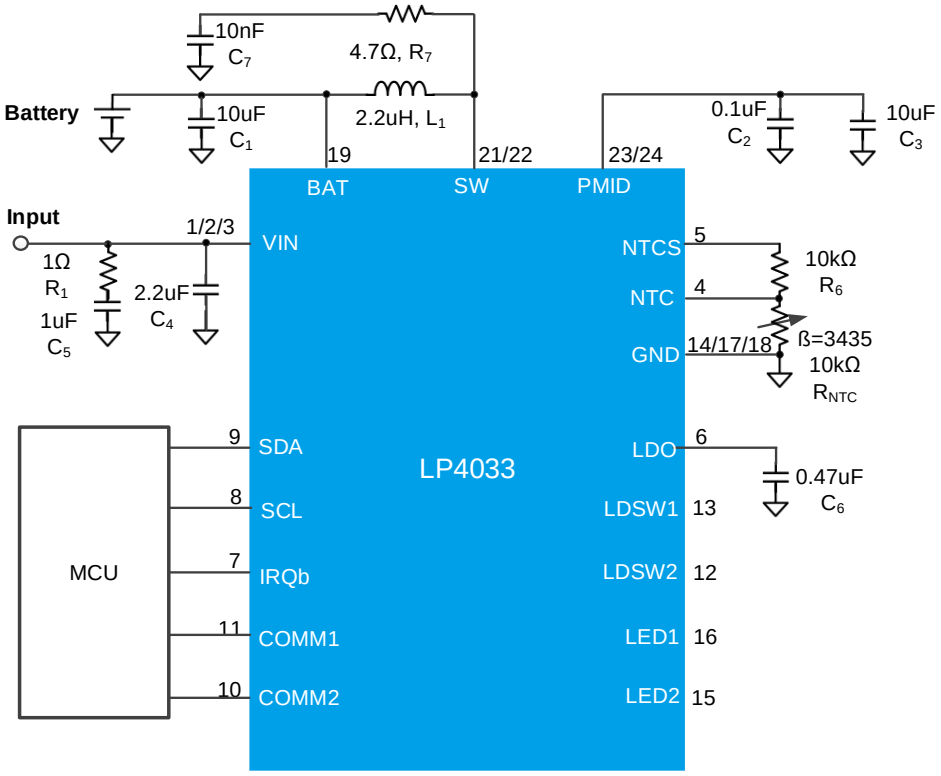


Figure 33. Typical Application Schematic

A typical application consists of the multi-function-in-one power management IC of LP4033 and a host MCU. When powering up in default mode, the battery CV voltage of LP4033 is 4.2V, the constant charging current is 370mA, the termination current and trickle charge current are 30mA. The maximum output voltage of boost converter is 5.1V and the discharge undercharge threshold is 3.1V. The MCU can change all the default values by the I^2C interface.

Inductor and Capacitor Selection

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the IN, BAT and PMID pin to the GND pin. The VIN capacitor C_4 and C_5 should be 25V rating with minimum 1-μF capacitance. The BAT capacitor C_1 should be at least 6.3V rating with minimum 10-μF capacitance. The PMID capacitor C_2 and C_3 should be at least 6.3V rating and the C_2 is used to filter the high frequency noise while the C3 serves as a bulk capacitor with minimum 10-μF capacitance. The LDO capacitor C_5 should be at least 6.3V rating with typical 0.47-μF capacitance.

The LP4033 is optimized to work between 1-μH and 2.2-μH inductance.

The snubber circuit is strongly recommended to be added to absorb the SW spike when boost converter works. A typical resistor of R_7 with 4.7Ω and a typical capacitor of C_7 with 1nF capacitance is a good trade-off between noise and efficiency.

NTC Circuit Design

As all the trigger point thresholds of the internal NTC comparators are well design with a certain type of NTC resistor, an 10-kΩ NTC resistor with 1% accuracy and with a beta of 3435 is recommended. The R_6 should be set to 10-kΩ to cooperate with the 10-kΩ NTC resistor. The following equation helps calculating the trigger point when the NTC resistor changes. All the trigger point thresholds can be found in the electrical characteristics table. The default NTC threshold indicates the temperature of -10 ˚C, 0 ˚C, 10 ˚C, 45 ˚C, 60 ˚C. The NTC pin can't be left float, setting both the R_6 and R_{NTC} to 1MΩ or higher if NTC is not used.

PCB Layout Guidelines

Please follow the rules when designing the PCB layout.

1. The high frequency filtering capacitor C_2 and C_3 should be placed with the highest priority and as close to the PMID pin and the GND pins (the GND pins and the NC pin of pin-20 should be connected to the thermal PAD). 0603 size capacitors are recommended. The loop circumference formed by the capacitors and the pins should under 200 mils to minimize the parasitic inductance. (For example, the enclosed circumference via the C_2, the PMID pin and the GND pins should be controlled to less than 200 mils. This the most critical path.)
2. The R_1 and C_5 is recommended to absorb the input spike when the USB is plugged in. The C_4 should be placed to the VIN pin and the ground plane with less than 300mil loop circumference.
3. The IN, VBAT, LDSW1, LDSW2 and the GND power paths should be wide and short to improve the system efficiency. As a recommendation, the trace path should be at least 40 mils to deliver 1A current with 1oz copper thickness.
4. C_7 and R_7 must be soldered as a snubber circuit to absorb the switching spike caused by the parasitic inductance and the bonding wires of the LP4033. The C_7 and R_7 can greatly reduce the spike.
5. The thermal pad should connected to the ground plane to help dissipating the power from the silicon.

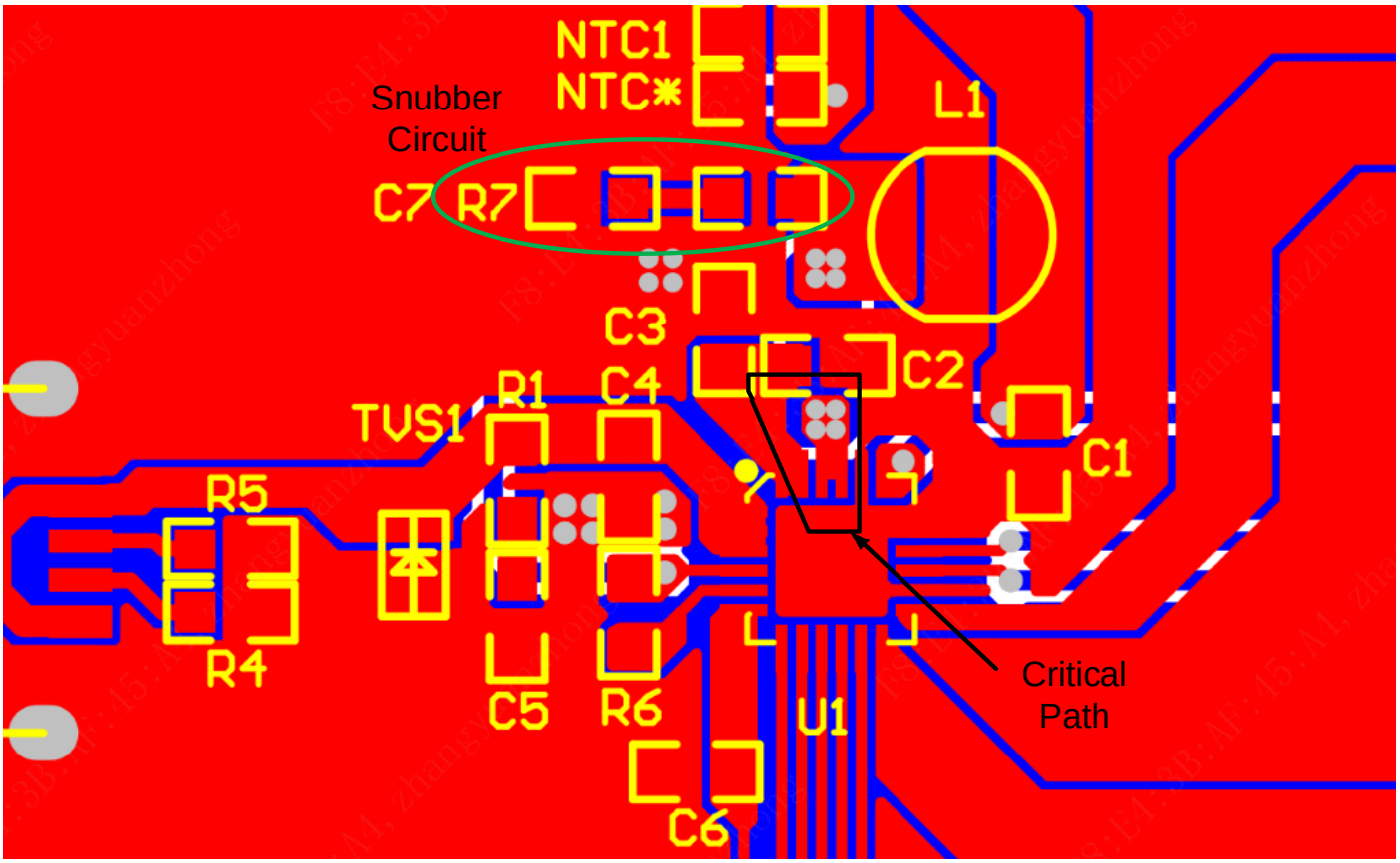
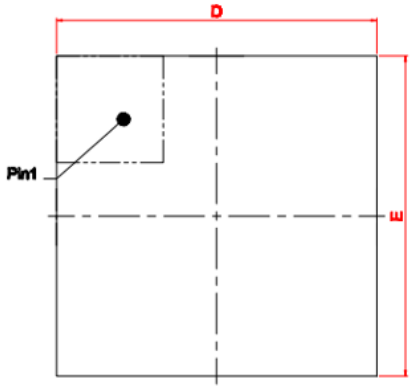


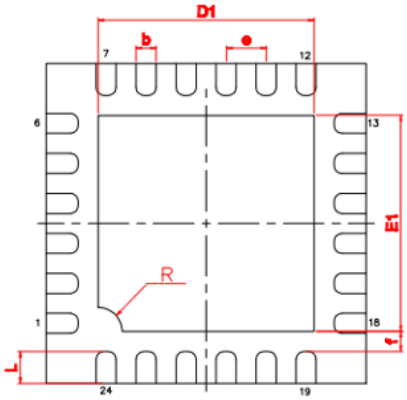
Figure 34. PCB Example (TOP View)

Packaging Information

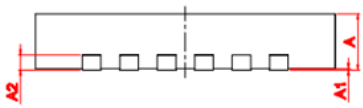
4x4 QFN package



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
* A1	0.00	0.02	0.05
* A2		0.20 REF	
* b	0.20	0.25	0.30
* D	3.90	4.00	4.10
* E	3.90	4.00	4.10
* D1	2.60	2.70	2.80
* E1	2.60	2.70	2.80
* e	0.45	0.50	0.55
R		0.30 REF	
* f	0.20	0.25	0.30
* L	0.30	0.40	0.50

Revision History

Revision	Date	Change Description
Rev 1p0	5/5/2023	Release Version 1.0