Multi-Channel DC-DC Converter for LCD Panels

General Description

The LP6281 is a programmable multi-channel power converter with integrated one channel VCOM buffer and fourteen channel gamma buffers for TFT LCD panel.

The LP6281 contains one VIO buck converter for T-CON power and one AVDD boost converter to provide the voltage of source driver, HAVDD OP, VCOM OP and Gamma buffer. Moreover, one Positive charge pump / boost (VGH) and one negative charge pump / inverting (VGL) are for the level shifter or gate driver.

The AVDD has isolation switch function for AVDD power on sequence. In addition, the VGH, VGL and VCOM have Negative temperature compensation (NTC) function. All output voltage can be programmed by IIC interface and integrated programmable non-volatile memory.

The LP6281 also integrated protection functions including over voltage protection (OVP), under voltage protection (UVP), short circuit protection (SCP), over current protection (OCP), over temperature protection (OTP) and under-voltage lockout (UVLO).

The package of LP6281 is QFN-46 (4.5mm x 6.5mm).

Order Information

LP6281 □□□

- F: Green
- Package Type
  - QV: QFN-46

Features

- Wide V_{IN} Input Range: 7.4V to 18V
- Current-Mode Boost Regulator for V_{AVDD}
  - Isolation Switch
  - Isolation SWG Control
  - 13.5V to 19.8V Programmable Output Voltage
  - 500/750kHz Switch Frequency
  - 5A Peak Current
  - Optional External Switching NMOS Control
- Buck Regulator for V_{IO}
  - 1.8V to 3.35V Programmable Output
  - 500/750kHz Switch Frequency
  - 3A Peak Current
- Operation Amplifier for V_{HAVDD}
  - 7-bits Resolution
  - ±200mA Peak Current
- Positive Charge Pump / Boost for VGH
  - 5-bits Resolution
  - 20V to 42V Programmable Output
  - Negative Temperature Compensation
- Negative Charge Pump / Inverting for VGL
  - 5-bits Resolution
  - -3V to -18V Output Voltage
  - Negative Temperature Compensation
- Operation Amplifier for VCOM
  - 7-bits Resolution
  - ±300mA Current Limit
  - Negative Temperature Compensation
- 14-Channel Programmable Gamma Buffers
  - 10-Bit Resolution
  - ±180mA Current Limit
- Under-Voltage Protection
- Over-Temperature Protection
- IIC Compatible Interface for Register Control
- Available in QFN-46 (4.5mmx6.5mm)
- RoHS Compliant and Halogen Free

Applications

- TFT LCD TV Panel

Marking Information

Device	Marking	Package	Shipping
LP6281QVF	LPS LP6281 YWX	QFN-46	3K/REEL
Y: Year code. **W**: Week code. **X**: Batch number.			

Typical Application Circuit

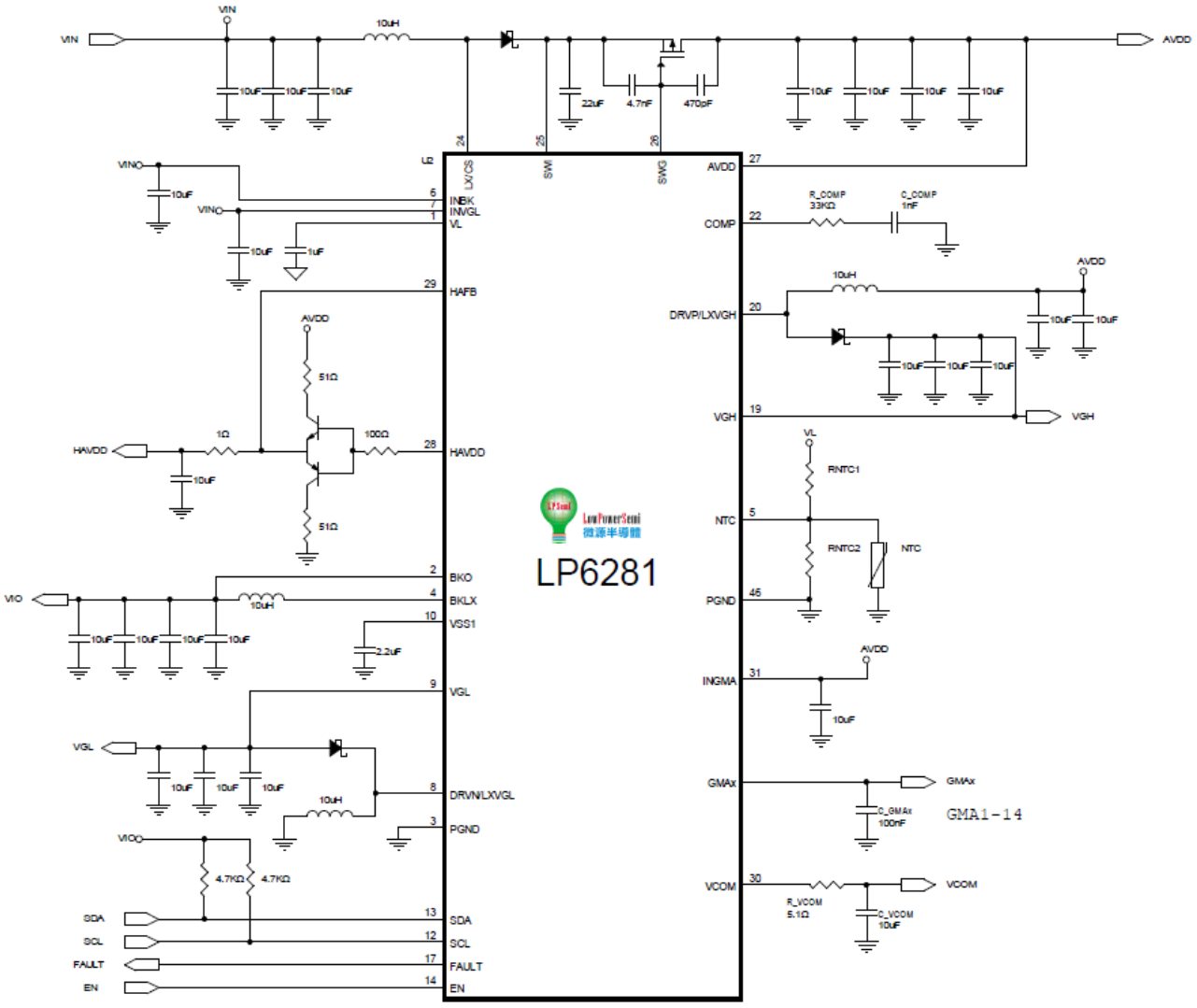


Figure 1. Application Circuit - AVDD Internal NMOS mode, VGH boost and VGL inverting type

Typical Application Circuit (Continued)

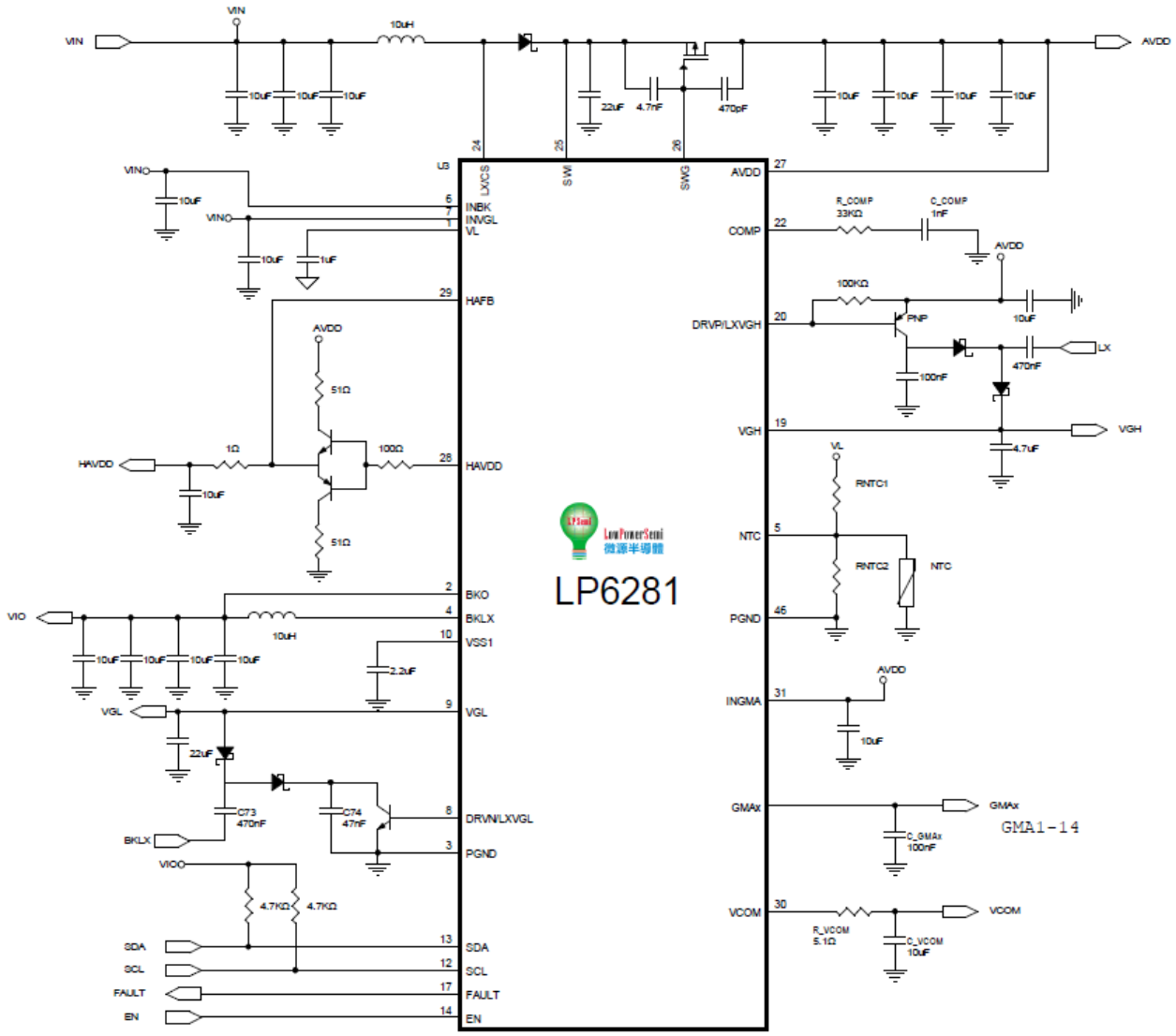


Figure 2. Application Circuit - AVDD Internal NMOS mode, VGH and VGL charge pump type

Block Diagram

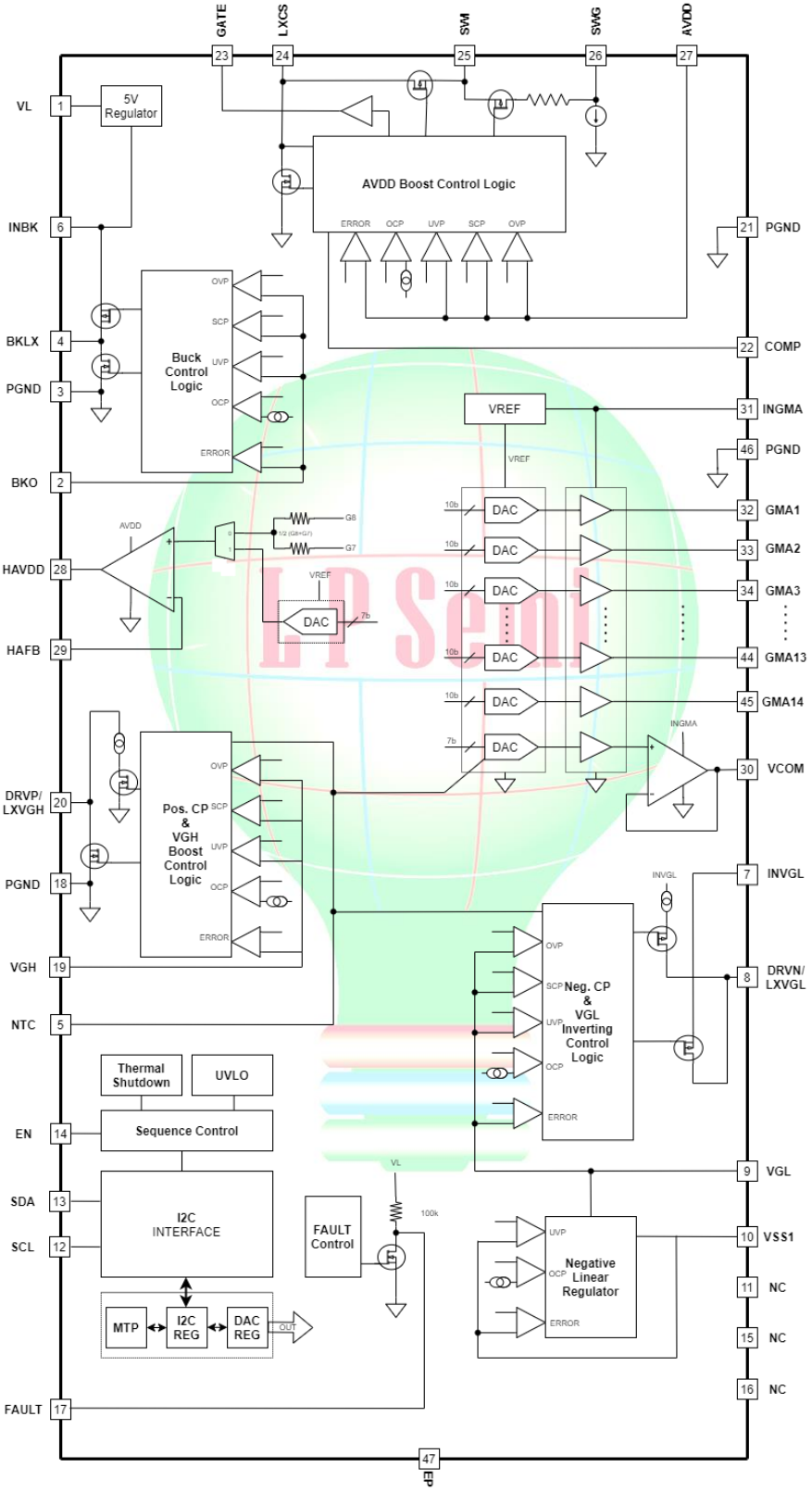


Figure 3. Block Diagram

Pin Configuration

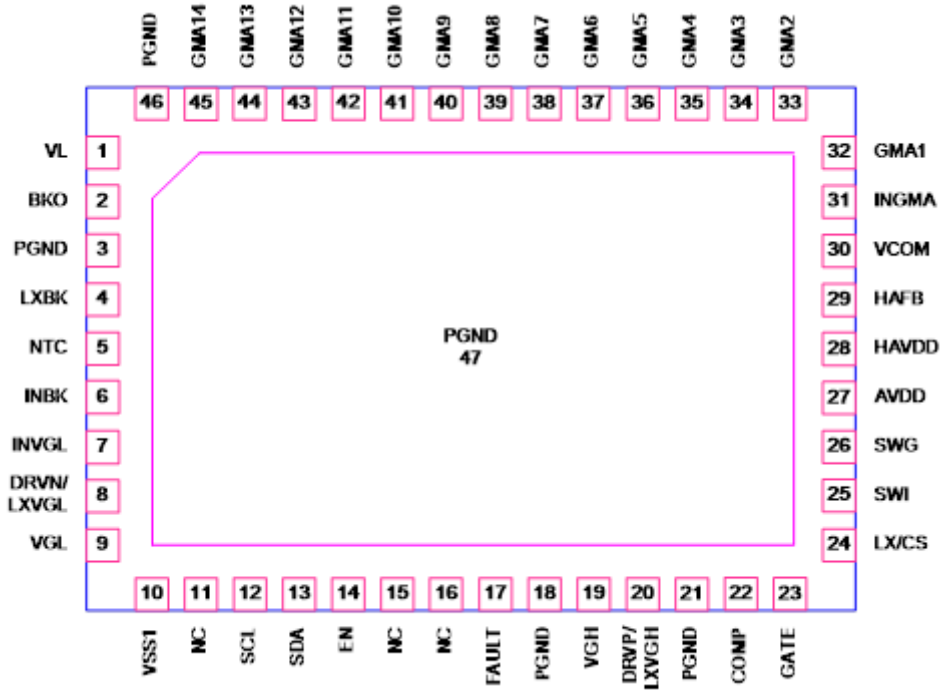


Figure 4. QFN-46 Package (4.5mm x 6.5mm)

Pin Description

Pin NO.	Pin Name	Description
1	VL	Internal Regulator Output. Connect 1uF capacitor to PGND.
2	BKO	Buck Regulator Voltage Sense Input Pin.
3, 18, 21, 46	PGND	Power Ground.
4	BKLX	Buck Regulator Switching Node. Connect the inductor and Schottky diode to BKLX.
5	NTC	Temperature Compensation Pin.
6	INBK	Supply Voltage Input for Buck and Internal Regulator. Connect a ceramic capacitor between VIN and PGND.
7	INVGL	Supply Voltage Input of the Inverting Converter.
8	DRVN/ LXVGL	DRVN：VGL Charge-Pump Regulator Driver Output. LXVGL：VGL Switch Node of the Inverting Converter.
9	VGL	VGL Feedback Voltage Sense Input Pin.
10	VSS1	Negative Supply Voltage of DISCHG.
11, 15, 16	NC	No Connection.
12	SCL	IIC interface clock signal.
13	SDA	IIC interface data signal.
14	EN	Enable Pin.
17	FAULT	FAULT Signal Input/Output Pin. The FAULT pin is an open drain pin with an internal pull-up resistor.
19	VGH	VGH Feedback Voltage Sense Input Pin.
20	DRVP/ LXVGH	DRVP：VGH Charge-Pump Regulator Driver Output. LXVGH：VGH Switch Node of the Boost Converter.
22	COMP	Boost Regulator Error Amplifier Compensation Pin.
23	GATE	External N-MOS gate driver for AVDD external mode.
24	LX/CS	LX：Boost Regulator Switch Node. Connect the inductor and the Schottky diode to LX. CS：External current sense for AVDD external mode.
25	SWI	Source Input of AVDD external isolation P-MOS.
26	SWG	Gate driver of the AVDD Boost converter external isolation P-MOS.
27	AVDD	Drain Output of AVDD external isolation P-MOS & Feedback Voltage Sense Input Pin.
28	HAVDD	HAVDD OP Output.
29	HAFB	HAVDD Feedback Voltage Sense Input Pin.
30	VCOM	VCOM OP Voltage Output Pin.
31	INGMA	Gamma Buffer and VCOM OP Power Source.
32 ~ 45	GMA1~14	Gamma Buffer Output.
47	EP	Exposed Pad. Connect this pin to PGND.

Absolute Maximum Ratings Note 1

- ✧ INBK, INVGL to PGND ---------- −0.3V to +23V
- ✧ BKLX to PGND ---------- -0.3 to (INBK+0.3)
- ✧ SWI, SWG, AVDD, HAVDD, HAFB, LX/CS to PGND ---------- −0.3V to +23V
- ✧ LX/CS to SWI ---------- −0.3 to +23V
- ✧ SWI to AVDD ---------- −0.3 to +23V
- ✧ EN, VL, SDA, SCL, FAULT to PGND ---------- −0.3V to +6V
- ✧ BKO, GATE, COMP, NTC to PGND ---------- −0.3V to (VL +0.3V)
- ✧ VGL, DRVN/LXVGL, VSS1 to PGND ---------- −20V to 0.3V
- ✧ VGL to VSS1 ---------- −20V to 0.3V
- ✧ DRVN/LXVGL to INVGL ---------- −40V to 0.3V
- ✧ VGH, DRVP/LXVGH to PGND ---------- −0.3V to +48V
- ✧ INGMA to PGND ---------- −0.3V to +23V
- ✧ VCOM, GMA1~GMA14 to PGND ---------- −0.3V to (INGMA +0.3V)
- ✧ Operating Junction Temperature Range (T_J) ---------- −40°C to +150°C
- ✧ Operation Ambient Temperature Range (T_A) ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1 Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. The functional operation of the device or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  QFN-46 4.5x6.5, θ_{JA} ---------- 35°C/W

  QFN-46 4.5x6.5, θ_{JC} ---------- 7°C/W

Electrical Characteristics

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General						
Input Supply Voltage	V_{IN}		7.4	--	18	V
Internal Oscillator Frequency	F_{OSC}	R[29h], Bit7=0	--	750	--	kHz
		R[29h], Bit7=1	--	500	--	kHz
V_{IN} Quiescent Current	I_Q	All LX Not Switching	--	10	--	mA
		All LX Switching	--	35	--	mA
Input UVLO Threshold	V_{UVLO}	V_{IN} Rising	--	6.8	--	V
UVLO Threshold Hysteresis	ΔV_{UVLO}	V_{IN} Falling Hysteresis	--	500	--	mV
AVDD UVLO Threshold	V_{UVLO_AVDD}	V_{AVDD} Rising	--	7.15	--	V
AVDD UVLO Threshold Hysteresis	ΔV_{UVLO_AVDD}	V_{AVDD} Falling Hysteresis	--	500	--	mV
Thermal Shutdown Threshold	T_{SD}	Temperature Rising	--	150	--	°C
Internal Regulator						
VL Output Voltage	V_L		4.9	5	5.1	V
Logic Input (SDA, SCL, EN)						
Input Threshold Voltage	V_{IH}	Logic High.	1.6	--	--	V
	V_{IL}	Logic Low	--	--	0.6	
EN Pull Down Resistance	R_{PD}		320	400	480	kΩ
IIC Output Low Voltage	V_{IIC}	I_{SINK}=6mA	0.3	--	--	V
IIC Input Capacitance			--	5	--	pF

Electrical Characteristics (Continued)

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
External NMOS Gate Driver (Gate of AVDD)						
Gate High Voltage	D_{Gate_OH}		4.5	5	5.5	V
Gate Low Voltage	D_{Gate_OL}		0	--	0.3	V
External NMOS Switch Current Limit	V_{CS_OCP}	R_{CS}=50mΩ	--	0.3	--	V
Gate to VL High-Side On Resistance	R_{DSon_GH}		--	3	--	Ω
Gate to GND Low-Side On Resistance	R_{DSon_GL}		--	3	--	Ω
ASYNC Boost Regulator (AVDD)						
AVDD Regulation Voltage Range	V_{AVDD}	R[00h], 6Bits, Step 0.1V	13.5	--	19.8	V
AVDD Output Accuracy		No load	-1	--	+1	%
Output Voltage Sense Resistor	R_{S_AVDD}	AVDD Pin	--	100	200	kΩ
NMOS Switch-ON Resistance	R_{DS_AVDD}	$I_{LX/CS}$=0.5A	--	100	185	mΩ
Transcocnductance	Gm	ΔI=5uA	--	120	--	uA/V
Current Sense Resistance	R_{CS}		--	250	--	mΩ
NMOS Switch Current Limit	I_{LIM_AVDD}	AVDD OCP	5	--	--	A
Soft Start Period	t_{SS_AVDD}	R[2Dh], Bit1=0	--	10	--	ms
Switch Leak Current	I_{LEAK}	$V_{LX/CS}$=19.8V	--	1	10	uA
SWI Over Voltage Protection	V_{OVP_SWI}	V_{SWI} Rising, hysteresis = 1V	--	21.8	--	V
AVDD Line Regulation		8V≦V_{IN}≦14V, I_{AVDD}=1mA	--	0.04	--	%/V
AVDD Load Regulation		1mA≦I_{AVDD}≦1A,	-1	--	+1	%/A
AVDD UVP Fault Trip Level	V_{UVP_AVDD}	V_{AVDD} Falling	--	85	--	%
AVDD UVP Fault Trigger Duration	T_{Fault_AVDD}		--	50	--	ms
AVDD SCP Fault Trip Level	V_{SCP_AVDD}	V_{AVDD} Falling	--	20	--	%
Maximum Duty Cycle	D_{MAX}		--	90	--	%
Gate Output High-Level	V_{GOH}		--	SWI	--	V
Gate Output Low-Level	V_{GOL}		--	SWI-6	--	V
Gate Pull-High Resistor	R_{AVDD}		--	10	--	kΩ
Gate Sink Current	I_{G_SINK}		--	10	--	uA
Power Off Discharge Resistance	R_{Dis_AVDD}	R[2Ch], Bit5 =1	--	4.7	--	kΩ

Electrical Characteristics (Continued)

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Inverting Converter and Negative Charge Pump Controller (VGL)						
VGL_NT Normal Temperature Voltage Range	V_{GL_NT}	R[05h], 5Bits	-18	--	-3	V
VGL_LT/HT Output Voltage Range	$V_{GL\_LT/HT}$	R[06h], 5Bits	-18	--	-3	V
Output Voltage Tolerance			-3	--	+3	%
Low-Side NMOS Switch on Resistance	R_{DS_VGL}		--	0.45	--	Ω
Minimum On Time			--	100	--	ns
PMOS Switch Current Limit	I_{LIM_VGL}		1.5	--	--	A
PMOS Switch Leak Current	I_{LEAK_LXVGL}	$V_{DRVN/LXVGL}$=V_{IN} or VGL	--	5	--	uA
VGL Line Regulation		8V≦V_{IN}≦14V, I_{VGL}=20mA	--	0.1	--	%/V
VGL Load Regulation		1mA≦I_{VGL}≦0.1A,	--	0.7	--	%/A
Soft Start Time	t_{SS_VGL}		--	3	--	ms
DRVN Source Current	I_{DRVN}	V_{DRVN}=0.7V	--	10	--	mA
VGL OVP Fault-Trip Level	V_{OVP_VGL}	VGL Falling, hysteresis: 105%	--	120	--	%
VGL UVP Fault Trip Level	V_{UVP_VGL}	VGL Rising	--	80	--	%
VGL Fault Trigger Duration	T_{Fault_VGL}		--	50	--	ms
VGL SCP Fault Trip Level	V_{SCP_VGL}	VGL Rising	--	20	--	%
Power Off Discharge Resistance	R_{Dis_VGL}	R[2Ch] Bit3=1	--	10	--	kΩ
VSS1 Negative Regulator (VSS1)						
Adjustable Output Voltage Range	V_{SS1}	R[07h] , 5Bits	-16	--	-3	V
Output Voltage Tolerance		No Load, Default Output	-3	--	+3	%
Current Limit	I_{LIM_VSS1}		--	100	--	mA
Soft Start Time	t_{SS}		--	3	--	ms
VSS1 UVP Fault Trip Level	V_{UVP_VSS1}		--	80	--	%
VSS1 UVP Fault Trigger Duration	T_{Fault_VSS1}		--	50	--	ms
Integral Nonlinearity	INL	No Load	-1	--	+1	LSB
Differential Nonlinearity	DNL	No Load	-1	--	+1	LSB
Load Regulation		I_{SS1}=-50mA to 50mA	--	±0.5	--	V/A
Power Off Discharge Resistance	R_{DIS_VSS1}	R[2Dh] Bit7=1	--	1.2	--	kΩ

Electrical Characteristics (Continued)

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ASYNC Boost Converter and Positive Charge Pump Controller (VGH)						
VGH_NT Normal Temperature Voltage Range	V_{GH_NT}	R[03h] , 5Bits	20	--	42	V
VGH_L Regulation Voltage Range	V_{GH_LT}	R[04h], 5Bits	20	--	42	V
Output Voltage Tolerance			-3	--	+3	%
Low-Side NMOS Switch on Resistance	R_{DSon_VGH}		--	0.55	--	Ω
NMOS Switch Current Limit	I_{LIM_VGH}		1.5	--	--	A
NMOS Switch Leak Current	I_{LEAK_VGH}	$V_{DRVP/LXVGH}$=42V	--	1	--	uA
VGH Line Regulation		8V≦V_{IN}≦14V, I_{VGH}=20mA	--	0.1	--	%/V
VGH Load Regulation		1mA≦I_{VGH}≦0.1A,	--	0.3	--	%/A
Soft Start Time	t_{SS_VGH}	R[2Dh] Bit0=0	--	3	--	ms
DRVP Sink Current	I_{DRVP}		--	5	--	mA
		VGH<VGH*20%	--	400	--	uA
VGH OVP Fault-Trip Level	V_{OVP_VGH}	VGH Rising, hysteresis: 3V	--	45	--	V
VGH UVP Fault Trip Level	V_{UVP_VGH}	VGH Falling	--	80	--	%
VGH UVP Fault Trigger Duration	T_{Fault_VGH}		--	50	--	ms
VGH SCP Fault Trip Level	V_{SCP_VGH}	VGH Falling	--	20	--	%
Power Off Discharge Resistance	R_{DIS_VGH}	R[2Ch] Bit4=1	--	30	--	kΩ
Thermal Compensation (VGH, VGL and VCOM)						
VGH & VGL Lower Bound Voltage of VTC1	V_{G_TC1}	R[2Eh], 4Bits	0.4	--	3.4	V
VGH & VGL Upper Bound Voltage of VTC2	V_{G_TC2}	R[2Eh], 4Bits	0.4	--	3.4	V
VCOM Lower Bound Voltage of VTC1	V_{C_TC1}	R[2Fh], 4Bits	0.4	--	3.4	V
VCOM Lower Bound Voltage of VTC2	V_{C_TC2}	R[2Fh], 4Bits	0.4	--	3.4	V

Electrical Characteristics (Continued)

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Buck Converter (VIO)						
Buck Output Voltage Range	V_{BK}	R[01h], 5Bits	1.8	--	3.35	V
Output Voltage Tolerance		I_{Load}=10mA	-2	--	+2	%
H-Side PMOS On Resistance	R_{DSon_BKH}	I_{LXBK}=0.5A	--	500	--	mΩ
L-Side NMOS On Resistance	R_{DSon_BKL}	I_{LXBK}=-0.1A	--	1	--	Ω
V_{BK} Current Limit	I_{LIM_BK}		3	--	--	A
H-Side PMOS Leak Current	I_{LEAK_BKLX}	V_{BKLX}=0V, V_{BKLX}=12V		1	10	uA
V_{BK} Line Regulation		8V≦V_{IN}≦14V, I_{BK}=0.1A	--	0.04	--	%/V
V_{BK} Load Regulation		0.1A≦I_{BK}≦1A	-1	--	+1	%
V_{BK} Soft Start Time	t_{SS_BK}		--	3	--	ms
V_{BK} Over Voltage Protection	V_{OVP_BK}	V_{BK} Raising	--	120	--	%
V_{BK} Under Voltage Threshold	V_{UVP_BK}	V_{BK} Falling	--	80	--	%
V_{BK} UVP Fault Trigger Duration	T_{Fault_VBK}		--	50	--	ms
V_{BK} SCP Fault Trip Level	V_{SCP_BK}	V_{BK} Falling	--	20	--	%
Power Off Discharge Resistance	R_{DIS_BK}	R[2Ch] Bit6=1	--	1	--	kΩ
HAVDD OPAMP (HAVDD)						
HAVDD Voltage Resolution			--	7	--	bits
Differential Nonlinearity	DNL	No load	-1	--	+1	LSB
Integral Nonlinearity	INL	No load	-4	--	+4	LSB
Output Voltage Swing High	V_{OH_HAVDD}	I_{HAVDD}=+100mA	--	V_{AVDD}-2	--	V
Output Voltage Swing Low	V_{OL_HAVDD}	I_{HAVDD}=-100mA	--	2	--	V
Output Current	I_{HAVDD}		--	±100	--	mA
Short Circuit Current	I_{SC_HAVDD}		--	±200	--	mA
Power Supply Rejection Ratio	PSRR		--	60	--	dB
Slew Rate	SR_{HA}		--	45	--	V/us
-3dB Bandwidth	BW		--	20	--	MHz
HAVDD Over Voltage Protection	V_{OVP_HA}	V_{HAVDD} Rising	--	120	--	%
HAVDD Under Voltage Threshold	V_{UVP_HA}	V_{HAVDD} Falling	--	80	--	%
HAVDD UVP Fault Trigger Duration	T_{Fault_HAVDD}		--	50	--	ms
HAVDD SCP Fault Trip Level	V_{SCP_HAVDD}	HAVDD Falling	--	20	--	%
Power Off Discharge Resistance	R_{DIS_HAVDD}	R[2Ch] Bit2=1	--	10	--	kΩ

Electrical Characteristics (Continued)

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gamma Buffers (GMA1 to GMA14)						
Supply Voltage Range	V_{INGMA}		13.5	--	19.8	V
Gamma Voltage Resolution		GMA1 to 14, 10Bits	--	V_{AVDD}/ 1024	--	V
Differential Nonlinearity Error	DNL	No Load	-1	--	+1	LSB
Integral Nonlinearity Error	INL	No Load	-4	--	+4	LSB
GMAx Voltage Swing High	V_{OH_GMAx}	I_{GMAx}=+10mA	V_{GMAI} -0.2	V_{GMAI} -0.15	--	V
GMAx Voltage Swing Low	V_{OL_GMAx}	I_{GMAx}=-10mA	--	0.15	0.2	V
GMAx Output Current	I_{GMAx}		--	±50	--	mA
Load Regulation		I_{GMA}=±10mA	--	±0.5	--	V/A
Short Circuit Current	I_{SC_GMAx}			±180		mA
Program to Output Delay	t_{D_GMAx}			15		us
VCOM OP (VCOM)						
Supply Voltage Range	V_{AVDD}		13.5	--	19.8	V
VCOM Voltage Resolution		V_{COM} will be clamped between V_{COM_MAX} and V_{COM_MIN}	--	V_{AVDD}/ 128	--	V
Adjustable Normal Temperature Output Voltage Range	V_{COM_NT}	R[08],7Bits, Res1=(V_{COM_MAX}-V_{COM_MIN})/127	0*Res1 + V_{COM_MIN}	--	127*Res1 + V_{COM_MIN}	V
Adjustable Low Temperature Output Voltage Range	V_{COM_HT}	R[09], 7Bits Res1=(V_{COM_MAX}-V_{COM_MIN})/127	0*Res1 + V_{COM_MIN}	--	127*Res1 + V_{COM_MIN}	V
Adjustable VCOM_MAX	V_{COM_MAX}	R[0A], 7Bits	V_{AVDD}/ 128	--	V_{AVDD}	V
Adjustable VCOM_MIN	V_{COM_MIN}	R[0B], 7Bits	0	--	0.992 * V_{AVDD}	V
Differential Nonlinearity	DNL	No load	-1	--	+1	LSB
Integral Nonlinearity	INL	No load	-4	--	+4	LSB
Output Current	I_{VCOM}		--	±150	--	mA
Load Regulation		I_{COM}=±100mA	--	±1	--	V/A
Short Circuit Current	I_{SC_VCOM}	VCOM to VINGMA or PGND	--	±300	--	mA
Slew Rate	SR_{VCOM}		--	45	--	V/us
Power Off Discharge Resistance	R_{DIS_VCOM}	R[2Ch] Bit1 & Bit0=1	--	8	--	kΩ

Electrical Characteristics (Continued)

T_A=25°C, V_{IN}=12V, V_{IO}=3.3V, V_{AVDD}=17.6V, V_{HAVDD}=8.8V, V_{VGH}=30V, V_{VGL}=-12V, V_{VSS1}=-6V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
IIC Timer Characteristics						
Serial Clock Frequency	F_{SCL}		0	--	1	MHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		500	--	--	ns
Hold Time (Repeated) START Condition	$t_{HD, DAT}$		250	--	--	ns
SCL Pulse-Width Low	t_{LOW}		300	--	--	ns
SCL Pulse-Width High	t_{HIGH}		300	--	--	ns
Setup Time for a Repeated START Condition	$t_{SU,STA}$		250	--	--	ns
Data Hold Time	$t_{HD, DAT}$		--	--	100	ns
Data Setup Time	$t_{SU, DAT}$		100	--	--	ns
SDA and SCL Receiving Rise Time	t_R		20+ 0.1CB	--	120	ns
SDA and SCL Receiving Fall Time	t_F		20+ 0.1CB	--	120	ns
SDA Transmitting Fall Time	t_{FF}		20+ 0.1CB	--	80	ns
Setup Time for STOP Condition	$t_{SU,STO}$		250	--	--	ns
Bus Capacitance	C_B		--	--	400	pF
Pulse Width of Suppressed Spike	t_{SP}		--	--	20	ns
EEPROM Start Up Blanking Time Note 2			--	30	50	ms
Program EEPROM Blanking Time Note 2			--	--	300	ms
Read EEPROM Blanking Time			--	1.5	5	ms

Note 2 The blanking time is defined as the duration of I2C REG. write to or load from EEPROM.

Power On/Off Sequence

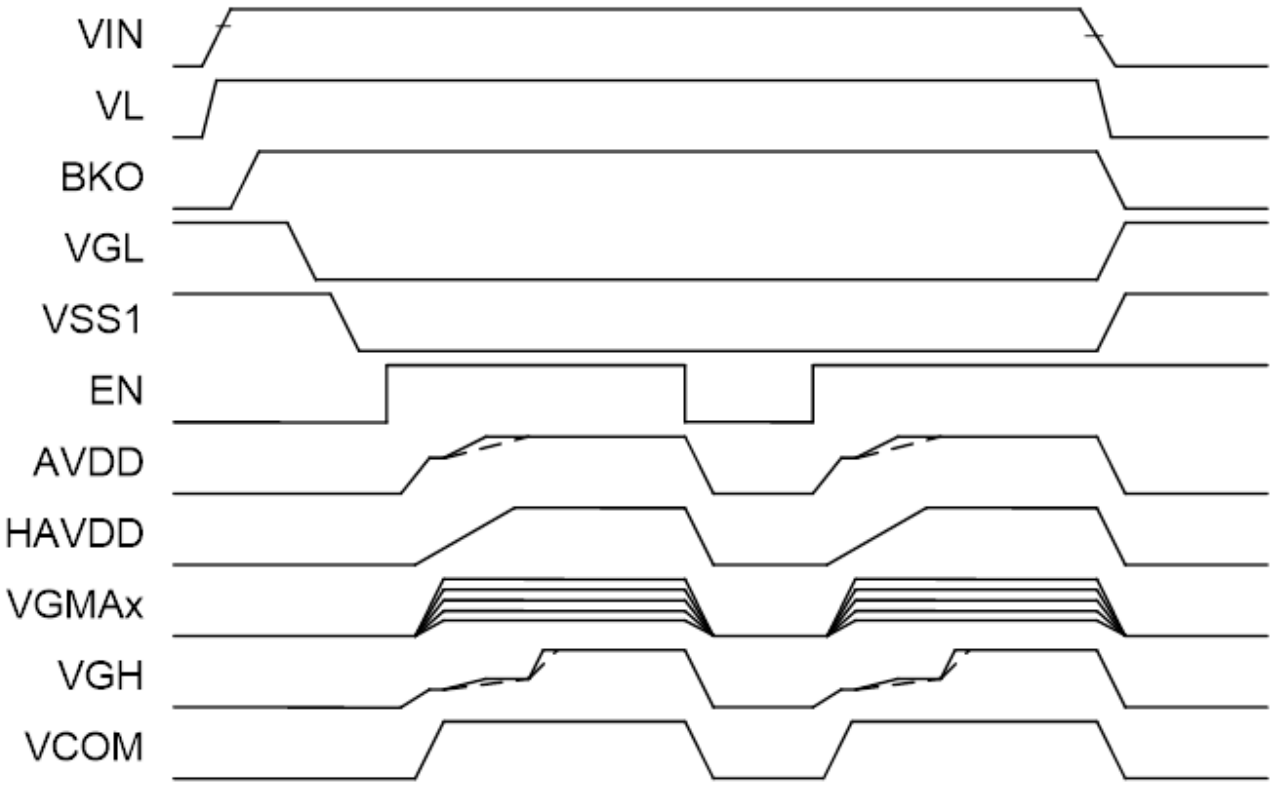
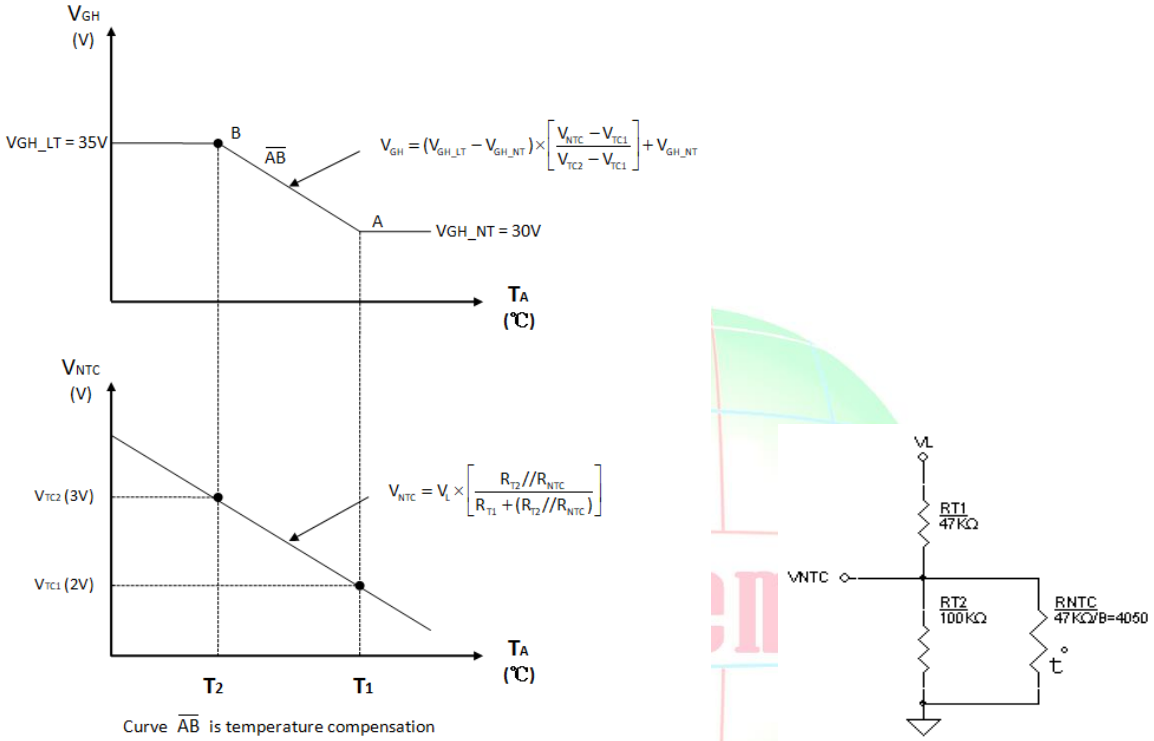


Figure 5. Power ON/OFF Sequence

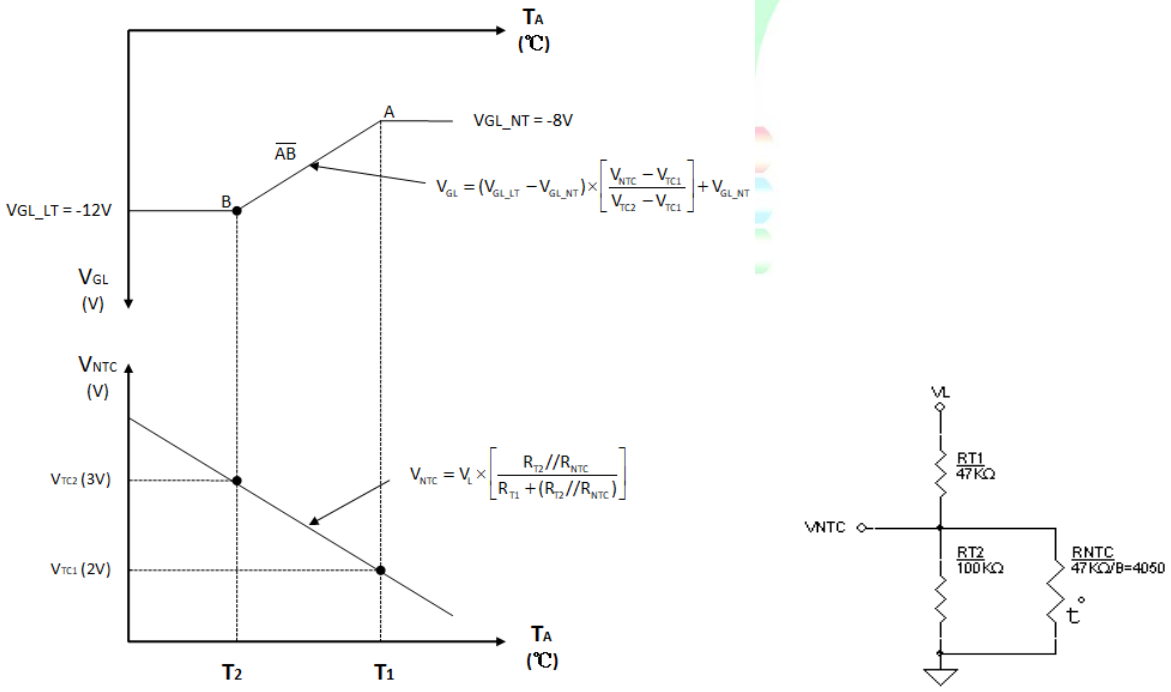
VGH/ VGH/ VCOM Temperature Compensation

1. VGH temperature compensation curve

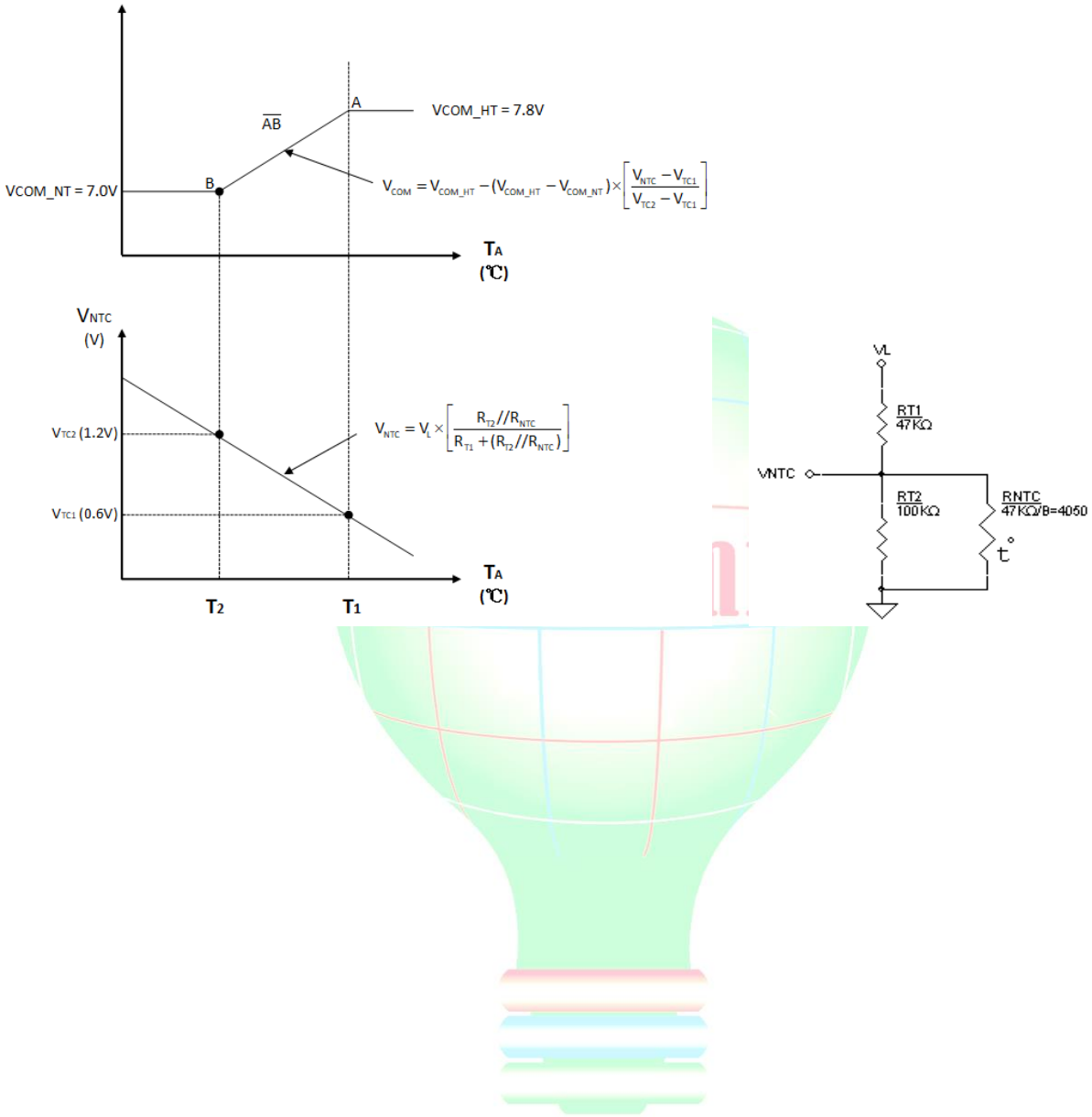


Curve $\overline{AB}$ is temperature compensation

2. VGL temperature compensation curve



3. VCOM temperature compensation curve



Application Information

1. IIC Interface Slave Address

The LP6281 can easily modify the parameters via IIC bus that the slave address is shown below:

Slave Address							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
0	*1*	*0*	*0*	*0*	*0*	*0*	1/0

IIC is a two wire serial interface developed, the bus consists of a clock line (SCL) and a data line (SDA) with pull-up resistor. The LP6281 works as a slave mode and the data transfer protocol follow IIC-Bus Specification's standard mode (100kbps) and fast mode (400kbps).

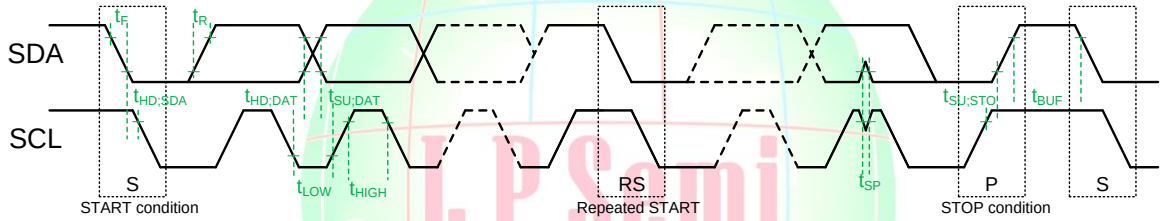


Figure 6. START and STOP Conditions

2. Write Data to Register

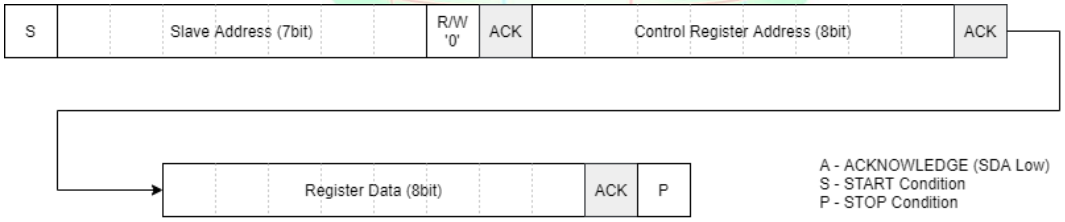


Figure 7. Write Single Byte Data to Register

3. Read Data to Register

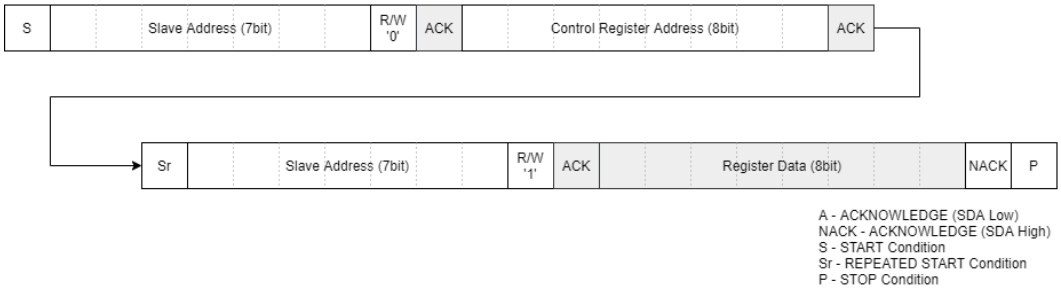


Figure 8. Read Single Byte Data from Register

Application Information (Continued)

4. IIC REGISTER MAP

The lowest bit number (0) represents the least bit, the highest bit number (7) represents the most bit, and R/W indicates whether the bit is read only (R), write only (W), or both read and write (R/W).

Register	Parameter	Symbol	Range	Resolution	MTP Factory Value
00h	[5:0] AVDD output voltage	AVDD	13.5V (00h) to 19.8V (3Fh)	0.1V	17.6V (29h)
01h	[4:0] VBK output voltage	VBK	1.8V (00h) to 3.35V (1Fh)	0.05V	3.3V (1Eh)
02h	[6:0] HAVDD output voltage	HAVDD	192*Res2 (00h) to 319*Res2 (7Fh) Res2=VAVDD/512	AVDD/512	Res2*(64+192) (40h)
03h	[4:0] VGH output voltage	VGH_NT	20V (00h) to 42V (16h)	1V	30V (0Ah)
04h	[7] VGH low temperature enable	VGH_LT_EN	0: Disable 1: Enable		0: Disable
	[4:0] VGH low temperature voltage	VGH_LT	20V (00h) to 42V (16h)	1V	35V (0Fh)
05h	[4:0] VGL normal temperature voltage	VGL_NT	-3V (00h) to -18V (1Eh)	0.5V	-8V (0Ah)
06h	[7] VGL temperature compensation enable	VGL_LT/HT_EN	0: Disable 1: Enable		0: Disable
	[6] VGL low or high temperature compensation selection	VGL_LT/HT_SEL	0: VGL_LT 1: VGL_HT		0: VGL_LT
	[4:0] VGL low temperature voltage/ VGL high temperature voltage	VGL_LT/HT	-3V (00h) to -18V (1Eh)	0.5V	-12V (12h)
07h	[7] VCOM high temperature enable	VCOM_HT_EN	0: Disable 1: Enable		0: Disable
	[4:0] VSS1 output voltage	VSS1	-3V (00h) to -16V (1Ah)	0.5V	-6V (06h)
08h	[7:1] VCOM_NT normal temperature voltage	VCOM_NT	V_{COM_MIN} to V_{COM_MAX} $Res1=(V_{COM\_MAX}-V_{COM\_MIN})/127$	Res1	$63*Res1+V_{COM\_MIN}$ (7Eh)
09h	[7:1] VCOM high temperature voltage	VCOM_HT	V_{COM_MIN} to V_{COM_MAX} $Res1=(V_{COM\_MAX}-V_{COM\_MIN})/127$	Res1	$93*Res1+V_{COM\_MIN}$ (BAh)
0Ah	[6:0] VCOM high limit voltage	V_{COM_MAX}	1*Res3 (00h) to 128*Res3 (7Fh) Res3=VAVDD/128	Res3	64*Res3 (3Fh)
0Bh	[6:0] VCOM low limit voltage	V_{COM_MIN}	0*Res3 (00h) to 127*Res3 (7Fh) Res3=VAVDD/128	Res3	38*Res3 (26h)

Register	Parameter	Symbol	Range	Resolution	MTP Factory Value
0Ch 0Dh	[9:0] Gamma1 output voltage	GAMMA1	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
0Eh 0Fh	[9:0] Gamma2 output voltage	GAMMA2	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
10h 11h	[9:0] Gamma3 output voltage	GAMMA3	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
12h 13h	[9:0] Gamma4 output voltage	GAMMA4	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
14h 15h	[9:0] Gamma5 output voltage	GAMMA5	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
16h 17h	[9:0] Gamma6 output voltage	GAMMA6	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
18h 19h	[9:0] Gamma7 output voltage	GAMMA7	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
1Ah 1Bh	[9:0] Gamma8 output voltage	GAMMA8	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
1Ch 1Dh	[9:0] Gamma9 output voltage	GAMMA9	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
1Eh 1Fh	[9:0] Gamma10 output voltage	GAMMA10	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
20h 21h	[9:0] Gamma11 output voltage	GAMMA11	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
22h 23h	[9:0] Gamma12 output voltage	GAMMA12	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
24h 25h	[9:0] Gamma13 output voltage	GAMMA13	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)
26h 27h	[9:0] Gamma14 output voltage	GAMMA14	0V (00h) to VAVDD (3FFh) Res4= VAVDD/1024	Res4	512*Res4 (200h)

Register	Parameter	Symbol	Range	Resolution	MTP Factory Value
28h	[7] Power Group B Enable Note*	Group B_EN	0: Disable 1: Enable		0: Disable
	[6] VGL Enable	VGL_EN	0: Disable 1: Enable		1: Enable
	[5] VSS1 Enable	VSS1_EN	0: Disable 1: Enable		1: Enable
	[4] AVDD Enable	AVDD_EN	0: Disable 1: Enable		1: Enable
	[3] HAVDD Enable	HAVDD_EN	0: Disable 1: Enable		1: Enable
	[2] Gamma Enable	GMA_EN	0: Disable 1: Enable		1: Enable
	[1] VCOM Enable	VCOM_EN	0: Disable 1: Enable		1: Enable
	[0] VGH Enable	VGH_EN	0: Disable 1: Enable		1: Enable
29h	[7] Frequency select	FREQ_SEL	0: 750kHz 1: 500kHz		0: 750kHz
	[4] AVDD Internal / External	AVDD_NMOS_INT/EXT	0: Internal 1: External		0: Internal
	[3] VGH structure type	VGH_TYPE	0: Boost 1: Charge pump		0: Boost
	[2] VGL structure type	VGL_TYPE	0: Inverting 1: Charge pump		0: Inverting
	[1] VGL charge pump source	VGL_PUMP_SOURCE	0: LXBK 1: LXCS		0: VBK1
	[0] Gamma channel type	GMA_CH_TYPE	0: 14CH (1to 14 CH) 1: 4CH (1, 7, 8, 14CH)		0: 14CH
2Ah	[5:4] VBK_Delay	VBK_DLY	00: 0ms 01: 2ms 10: 4ms 11: 6ms		10: 4ms
	[3:2] VGL_Delay	VGL_DLY	00: 0ms 01: 5ms 10: 10ms 11: 15ms		01: 5ms
	[1:0] VSS1_Delay	VSS1_DLY	00: 0ms 01: 2ms 10: 4ms 11: 6ms		01: 2ms
2Bh	[6:5] AVDD_Delay	AVDD_DLY	00: 0ms 01: 5ms 10: 10ms 11: 15ms		01: 5ms
	[4:3] VGH_Delay	VGH_DLY	00: 0ms 01: 2ms 10: 4ms 11: 6ms		01: 2ms
	[2:0] VCOM_Delay	VCOM_DLY	000: 0ms 001: 30ms 010: 60ms 011: 90ms 100: 120ms 101: 150ms 110: 180ms 111: 210ms		000: 0ms
2Ch	[7] All Discharge Enable	ALL_DIS_EN	0: Disable 1: Enable		1: Enable
	[6] Bulk discharge	BK_DIS	0: 0.5kohm 1: 1kohm		1: 1kohm
	[5] AVDD discharge	AVDD_DIS	0: 1.4kohm 1: 4.7kohm		1: 4.7kohm
	[4] VGH discharge	VGH_DIS	0: 1.5kohm 1: 30kohm		1: 30kohm
	[3] VGL discharge	VGL_DIS	0: Disable 1: 10kohm		1: 10kohm
	[2] HAVDD discharge	HAVDD_DIS	0: Disable 1: 10kohm		1: 10kohm
	[1:0] VCOM discharge	VCOM_DIS	00: Disable 01: 20ohm 10: 1kohm 11: 8kohm		1: 8kohm

Register	Parameter	Symbol	Range	Resolution	MTP Factory Value
2Dh	[7] VSS1 discharge enable	VSS1_DIS	0: Disable 1: 1.2kohm		1: 1.2kohm
	[4] VCOM discharge type	VCOM_DIS_TYP	0: VIN_UVLO_F 1: Reserved		0: VIN_UVLO_F
	[3] HAVDD feedback mode type	HAVDD_FB	0: (G7+G8)/2 1: HAVDD DAC register		0: (G7_G8)/2
	[1] AVDD soft start	AVDD_SS	0: 10ms 1: 20ms		0: 10ms
	[0] VGH soft start	VGH_SS	0: 3ms 1: 6ms		1: 6ms
2Eh	[7:4] VGH & VGL_VTC2	VGH&VGL_ VTC1/2	0000: 0.4V to 1111: 3.4V	0.2V	1101: 3.0V
	[3:0] VGH & VGL_VTC1		0000: 0.4V to 1111: 3.4V	0.2V	1000: 2.0V
2Fh	[7:4] VCOM_VTC2	VCOM_ VTC1/2	0000: 0.4V to 1111: 3.4V	0.2V	0100: 1.2V
	[3:0] VCOM_VTC1		0000: 0.4V to 1111: 3.4V	0.2V	0001: 0.6V
30h	[5:4] AVDD external driving of Gate	AVDD_EXT_DRV	00: EXT_DRV0 01: EXT_DRV1 10: EXT_DRV2 11: EXT_DRV3		01: EXT_DRV1
	[3:2] VGH boost converter mode compensation	VGH_COMP	00: VGH_COMP0 01: VGH_COMP1 10: VGH_COMP2 11: VGH_COMP3		10: VGH_COMP2
	[1:0] VGL inverting mode compensation	VGL_COMP	00: VGL_COMP0 01: VGL_COMP1 10: VGL_COMP2 11: VGL_COMP3		10: VGL_COMP2
FFh	[7] & [0] Control register	Ctrl	00h, 01h, 40h, 80h		00h

Note*: Power Group A: VBK

Power Group B: AVDD, HAVDD, VGH, VGL, VSS1, Gamma, VCOM

AVDD Output Voltage Register (00h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R	R/W	R/W	R/W	R/W	R/W	R/W
-	-	1	0	1	0	0	1

Value	AVDD	Value	AVDD	Value	AVDD	Value	AVDD
00h	13.5V	10h	15.1V	20h	16.7V	30h	18.3V
01h	13.6V	11h	15.2V	21h	16.8V	31h	18.4V
02h	13.7V	12h	15.3V	22h	16.9V	32h	18.5V
03h	13.8V	13h	15.4V	23h	17.0V	33h	18.6V
04h	13.9V	14h	15.5V	24h	17.1V	34h	18.7V
05h	14.0V	15h	15.6V	25h	17.2V	35h	18.8V
06h	14.1V	16h	15.7V	26h	17.3V	36h	18.9V
07h	14.2V	17h	15.8V	27h	17.4V	37h	19.0V
08h	14.3V	18h	15.9V	28h	17.5V	38h	19.1V
09h	14.4V	19h	16.0V	29h	17.6V	39h	19.2V
0Ah	14.5V	1Ah	16.1V	2Ah	17.7V	3Ah	19.3V
0Bh	14.6V	1Bh	16.2V	2Bh	17.8V	3Bh	19.4V
0Ch	14.7V	1Ch	16.3V	2Ch	17.9V	3Ch	19.5V
0Dh	14.8V	1Dh	16.4V	2Dh	18.0V	3Dh	19.6V
0Eh	14.9V	1Eh	16.5V	2Eh	18.1V	3Eh	19.7V
0Fh	15.0V	1Fh	16.6V	2Fh	18.2V	3Fh	19.8V

VBK Output Voltage Register (01h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R	R	R/W	R/W	R/W	R/W	R/W
-	-	-	1	1	1	1	0

Value	VBK	Value	VBK	Value	VBK	Value	VBK
00h	1.80V	08h	2.20V	10h	2.60V	18h	3.00V
01h	1.85V	09h	2.25V	11h	2.65V	19h	3.05V
02h	1.90V	0Ah	2.30V	12h	2.70V	1Ah	3.10V
03h	1.95V	0Bh	2.35V	13h	2.75V	1Bh	3.15V
04h	2.00V	0Ch	2.40V	14h	2.80V	1Ch	3.20V
05h	2.05V	0Dh	2.45V	15h	2.85V	1Dh	3.25V
06h	2.10V	0Eh	2.50V	16h	2.90V	1Eh	3.30V
07h	2.15V	0Fh	2.55V	17h	2.95V	1Fh	3.35V

HAVDD Output Voltage Register (02h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
-	1	0	0	0	0	0	0

HAVDD voltage formula

HAVDD = Res2 *(HAVDD_CODE+192)

Res2 = AVDD / 512

HAVDD_CODE = 0 ~ 127

HAVDD Output Voltage

Value	HAVDD	Value	HAVDD	Value	HAVDD	Value	HAVDD	Value	HAVDD
00h	Res2*(0+192)	1Ah	Res2*(26+192)	34h	Res2*(52+192)	4Eh	Res2*(78+192)	68h	Res2*(104+192)
01h	Res2*(1+192)	1Bh	Res2*(27+192)	35h	Res2*(53+192)	4Fh	Res2*(79+192)	69h	Res2*(105+192)
02h	Res2*(2+192)	1Ch	Res2*(28+192)	36h	Res2*(54+192)	50h	Res2*(80+192)	6Ah	Res2*(106+192)
03h	Res2*(3+192)	1Dh	Res2*(29+192)	37h	Res2*(55+192)	51h	Res2*(81+192)	6Bh	Res2*(107+192)
04h	Res2*(4+192)	1Eh	Res2*(30+192)	38h	Res2*(56+192)	52h	Res2*(82+192)	6Ch	Res2*(108+192)
05h	Res2*(5+192)	1Fh	Res2*(31+192)	39h	Res2*(57+192)	53h	Res2*(83+192)	6Dh	Res2*(109+192)
06h	Res2*(6+192)	20h	Res2*(32+192)	3Ah	Res2*(58+192)	54h	Res2*(84+192)	6Eh	Res2*(110+192)
07h	Res2*(7+192)	21h	Res2*(33+192)	3Bh	Res2*(59+192)	55h	Res2*(85+192)	6Fh	Res2*(111+192)
08h	Res2*(8+192)	22h	Res2*(34+192)	3Ch	Res2*(60+192)	56h	Res2*(86+192)	70h	Res2*(112+192)
09h	Res2*(9+192)	23h	Res2*(35+192)	3Dh	Res2*(61+192)	57h	Res2*(87+192)	71h	Res2*(113+192)
0Ah	Res2*(10+192)	24h	Res2*(36+192)	3Eh	Res2*(62+192)	58h	Res2*(88+192)	72h	Res2*(114+192)
0Bh	Res2*(11+192)	25h	Res2*(37+192)	3Fh	Res2*(63+192)	59h	Res2*(89+192)	73h	Res2*(115+192)
0Ch	Res2*(12+192)	26h	Res2*(38+192)	40h	Res2*(64+192)	5Ah	Res2*(90+192)	74h	Res2*(116+192)
0Dh	Res2*(13+192)	27h	Res2*(39+192)	41h	Res2*(65+192)	5Bh	Res2*(91+192)	75h	Res2*(117+192)
0Eh	Res2*(14+192)	28h	Res2*(40+192)	42h	Res2*(66+192)	5Ch	Res2*(92+192)	76h	Res2*(118+192)
0Fh	Res2*(15+192)	29h	Res2*(41+192)	43h	Res2*(67+192)	5Dh	Res2*(93+192)	77h	Res2*(119+192)
10h	Res2*(16+192)	2Ah	Res2*(42+192)	44h	Res2*(68+192)	5Eh	Res2*(94+192)	78h	Res2*(120+192)
11h	Res2*(17+192)	2Bh	Res2*(43+192)	45h	Res2*(69+192)	5Fh	Res2*(95+192)	79h	Res2*(121+192)
12h	Res2*(18+192)	2Ch	Res2*(44+192)	46h	Res2*(70+192)	60h	Res2*(96+192)	7Ah	Res2*(122+192)
13h	Res2*(19+192)	2Dh	Res2*(45+192)	47h	Res2*(71+192)	61h	Res2*(97+192)	7Bh	Res2*(123+192)
14h	Res2*(20+192)	2Eh	Res2*(46+192)	48h	Res2*(72+192)	62h	Res2*(98+192)	7Ch	Res2*(124+192)
15h	Res2*(21+192)	2Fh	Res2*(47+192)	49h	Res2*(73+192)	63h	Res2*(99+192)	7Dh	Res2*(125+192)
16h	Res2*(22+192)	30h	Res2*(48+192)	4Ah	Res2*(74+192)	64h	Res2*(100+192)	7Eh	Res2*(126+192)
17h	Res2*(23+192)	31h	Res2*(49+192)	4Bh	Res2*(75+192)	65h	Res2*(101+192)	7Fh	Res2*(127+192)
18h	Res2*(24+192)	32h	Res2*(50+192)	4Ch	Res2*(76+192)	66h	Res2*(102+192)		
19h	Res2*(25+192)	33h	Res2*(51+192)	4Dh	Res2*(77+192)	67h	Res2*(103+192)		

VGH Output Voltage Register (03h)

Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R	R	R/W	R/W	R/W	R/W	R/W
-	-	-	0	1	0	1	0

Value	VGH_NT	Value	VGH_NT	Value	VGH_NT
00h	20V	08h	28V	10h	36V
01h	21V	09h	29V	11h	37V
02h	22V	0Ah	30V	12h	38V
03h	23V	0Bh	31V	13h	39V
04h	24V	0Ch	32V	14h	40V
05h	25V	0Dh	33V	15h	41V
06h	26V	0Eh	34V	16h	42V
07h	27V	0Fh	35V		

VGH_LT Output Voltage Register (04h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R/W	R	R	R/W	R/W	R/W	R/W	R/W
0	-	-	0	1	1	1	1

Bit[7]: VGH Low Temperature Compensation Enable	
Value	Description
0	Disable
1	Enable

[4:0]: VGH Low Temperature Voltage					
DAC value	VGH_LT	DAC value	VGH_LT	DAC value	VGH_LT
00h	20V	08h	28V	10h	36V
01h	21V	09h	29V	11h	37V
02h	22V	0Ah	30V	12h	38V
03h	23V	0Bh	31V	13h	39V
04h	24V	0Ch	32V	14h	40V
05h	25V	0Dh	33V	15h	41V
06h	26V	0Eh	34V	16h	42V
07h	27V	0Fh	35V		

VGL Output Voltage Register (05h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R	R	R/W	R/W	R/W	R/W	R/W
-	-	-	0	1	0	1	0

Value	VGL_NT	Value	VGL_NT	Value	VGL_NT	Value	VGL_NT
00h	-3.0V	08h	-7.0V	10h	-11.0V	18h	-15.0V
01h	-3.5V	09h	-7.5V	11h	-11.5V	19h	-15.5V
02h	-4.0V	0Ah	-8.0V	12h	-12.0V	1Ah	-16.0V
03h	-4.5V	0Bh	-8.5V	13h	-12.5V	1Bh	-16.5V
04h	-5.0V	0Ch	-9.0V	14h	-13.0V	1Ch	-17.0V
05h	-5.5V	0Dh	-9.5V	15h	-13.5V	1Dh	-17.5V
06h	-6.0V	0Eh	-10.0V	16h	-14.0V	1Eh	-18.0V
07h	-6.5V	0Fh	-10.5V	17h	-14.5V		

VGL_LT Output Voltage Register (06h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
0	0	-	1	0	0	1	0

Bit[7]: VGL Low Temperature Compensation Enable	
Value	Description
0	Disable
1	Enable

Bit[6]: VGL Low Temperature Compensation Selection	
Value	Description
0	VGL_LT
1	VGL_HT

[4:0]: VGL_LT/HT Low Temperature Voltage							
Value	VGL_LT/HT	Value	VGL_LT/HT	Value	VGL_LT/HT	Value	VGL_LT/HT
00h	-3.0V	08h	-7.0V	10h	-11.0V	18h	-15.0V
01h	-3.5V	09h	-7.5V	11h	-11.5V	19h	-15.5V
02h	-4.0V	0Ah	-8.0V	12h	-12.0V	1Ah	-16.0V
03h	-4.5V	0Bh	-8.5V	13h	-12.5V	1Bh	-16.5V
04h	-5.0V	0Ch	-9.0V	14h	-13.0V	1Ch	-17.0V
05h	-5.5V	0Dh	-9.5V	15h	-13.5V	1Dh	-17.5V
06h	-6.0V	0Eh	-10.0V	16h	-14.0V	1Eh	-18.0V
07h	-6.5V	0Fh	-10.5V	17h	-14.5V		

VCOM High Temperature Enable & VSS1 Output Voltage Register (07h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R/W	R	R	R/W	R/W	R/W	R/W	R/W
0	-	-	0	0	1	1	0

Bit[7]: VCOM High Temperature Compensation Enable	
Value	Description
0	Disable
1	Enable

[4:0]: VSS1 Output Voltage							
Value	VSS1	Value	VSS1	Value	VSS1	Value	VSS1
00h	-3.0V	08h	-7.0V	10h	-11.0V	18h	-15.0V
01h	-3.5V	09h	-7.5V	11h	-11.5V	19h	-15.5V
02h	-4.0V	0Ah	-8.0V	12h	-12.0V	1Ah	-16.0V
03h	-4.5V	0Bh	-8.5V	13h	-12.5V		
04h	-5.0V	0Ch	-9.0V	14h	-13.0V		
05h	-5.5V	0Dh	-9.5V	15h	-13.5V		
06h	-6.0V	0Eh	-10.0V	16h	-14.0V		
07h	-6.5V	0Fh	-10.5V	17h	-14.5V		

VCOM_NT Temperature Voltage Register (08h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0	1	1	1	1	1	1	-

VCOM_NT voltage formula

VCOM_NT = Res1*VCOM_NT CODE +V_{COM_MIN}

Res1 = (V_{COM_MAX} - V_{COM_MIN})/127

VCOM_NT CODE = 0 ~ 127

VCOM_HT Temperature Voltage Register (09h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
1	0	1	1	1	0	1	-

VCOM_HT voltage formula

VCOM_HT = Res1*VCOM_HT CODE + V_{COM_MIN}

Res1 = (V_{COM_MAX} - V_{COM_MIN})/127

VCOM_HT CODE = 0 ~ 127

VCOM High Limit Voltage Register (0Ah)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
-	0	1	1	1	1	1	1

VCOM High Limit Voltage Register (0Bh)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
-	0	1	0	0	1	1	0

VCOM_MAX / VCOM_MIN voltage formula

V_{COM_MAX} = Res3 * [(VCOM_MAX_CODE) + 1]

V_{COM_MIN} = Res3 * VCOM_MIN_CODE

Res3 = V_{AVDD} / 128

GAMMA1~14 Output Voltage — 0Ch~27h

Register	Name	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	GMA1	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA1[9:8]	
0Dh	GMA1	00h	GMA1[7:0]							
0Eh	GMA2	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA2[9:8]	
0Fh	GMA2	00h	GMA2[7:0]							
……	……	……	……	……	……	……	……	……	……	
……	……	……	……							
……	……	……	……	……	……	……	……	……	……	
……	……	……	……							
24h	GMA13	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA13[9:8]	
25h	GMA13	00h	GMA13[7:0]							
26h	GMA14	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA14[9:8]	
27h	GMA14	00h	GMA14[7:0]							

VGAMMA1~14 voltage formula

VGAMMA1~14 = Res4 x VGAMMA1~14_CODE

Res4 = VAVDD / 1024

Channel Enable Register (28h)							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Group B_ EN	VGL_EN	VSS1_EN	AVDD_EN	HAVDD_EN	GMA_EN	VCOM_EN	VGH_EN
0	1	1	1	1	1	1	1

Bit[7]: Group Enable	
Value	**Description**
0	Disable Group B Channel
1	Enable Group B Channel

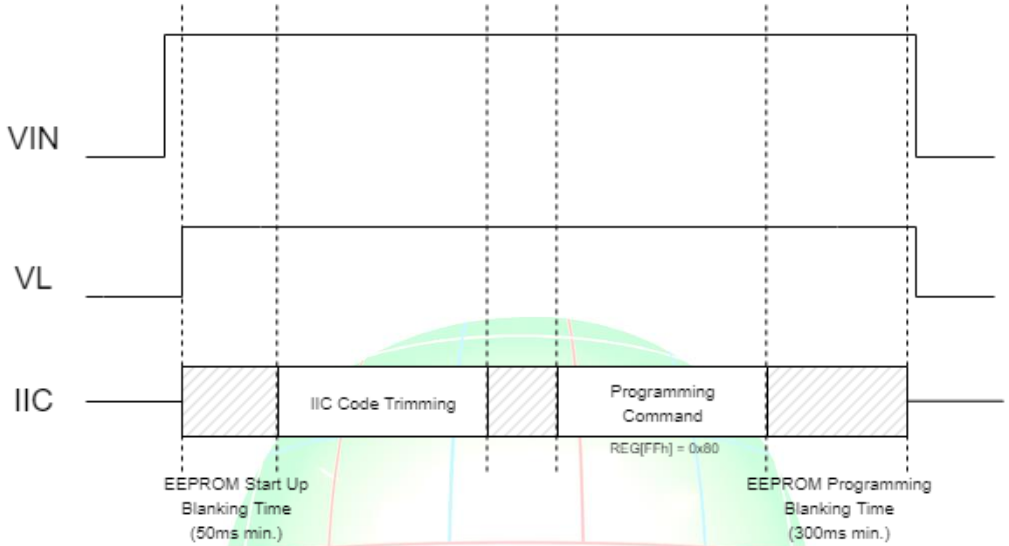
Control Function Register (FFh) – 0x00, 0x01, 0x40, 0x80							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
W	W	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0

Bit[7]: Write all data to EEPROM	
Value	**Description**
0	Read data from register.
1	Write all register value to EEPROM.

Bit[6]: Write VCOM data to EEPROM	
Value	**Description**
0	Read data from register.
1	Write VCOM register value to EEPROM.

Bit[0]: Read Data from Register or EEPROM	
Value	**Description**
0	Read data from register.
1	Read data from EEPROM.

5. IIC MTP Programming Timing



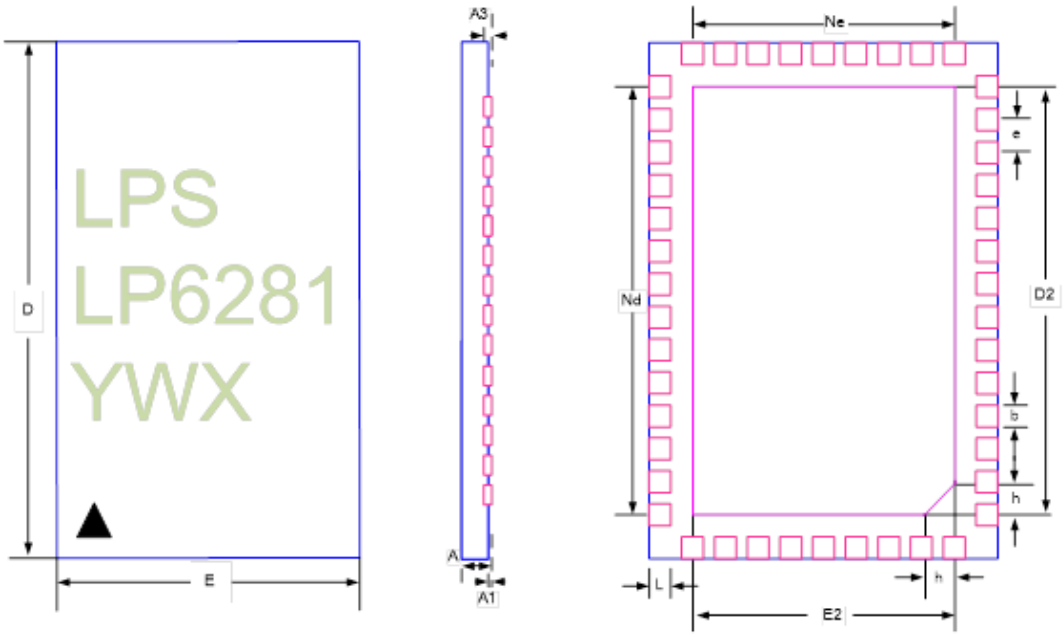
Layout Consideration

The proper PCB layout and component placement are critical for all circuit. The careful attention to prevent the electromagnetic interference (EMI) problems is necessary. Here are some layout suggestions to the layout design of LP6281.

- Connected all ground together with one uninterrupted ground plane, which include power ground and analog ground.
- The placements of the input bypass capacitor must be as close as possible to the LP6281 to reduce the input ripple voltage and noise coupling. The ground of input bypass capacitor must connect near to the IC's ground pin.
- Use wide and short traces for high current paths minimizing the area of high current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the terminals of internal power switches, LX, BKLX, LXVGH and LXVGL. The long and narrow trace increases the ESR and ESL, and that will induce more effective noise at high frequency easily.
- The compensation network should connect to LP6281 as close as possible. Each output voltage feedback route should keep away from any switching node.
- The Exposed Pad should be connected to a strong ground plane for maximum thermal consideration.

Package Information

QFN-46 Package (4.5x6.5) pitch 0.4 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.150	0.200	0.250
A3	0.180	0.200	0.250
D	6.400	6.500	6.600
D2	5.000	5.100	5.200
E	4.400	4.500	4.600
E2	3.000	3.100	3.200
e	0.400 BSC		
Nd	5.200 BSC		
Ne	3.200 BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400