Features

- **Case Charging Management**
  - Support 4.1V to 6.0 V input voltage with 30V absolute maximum input voltage rating
  - Programmable fast charge current up to 1.7A with up to 95% efficiency and 5% accuracy
  - Programmable floating voltage with 0.5% accuracy
  - Automatic recharge function
  - Programmable trickle charge current
  - Programmable termination current
- **Smart Earphone Charging Management**
  - Independent earphone insert detection and charging path
  - Smart earphone ultra-low dropout charging to maximize battery run time
  - Programmable earphone fast charge current up to 300mA each channel
  - Programmable End of Charge (EEOC) current
  - Bi-directional communication to earphones
- Programmable Always-on Linear Regulator
- Temperature Management
  - JEITA standard NTC management during charging and discharging
  - Charging current thermal foldback
  - Thermal shutdown protection
- I2C interface with interrupt indication
- 5-uA ultra-low quiescent current
- 4mm X 4mm QFN-24 package
- RoHS Compliant and 100% Lead (Pb) free

Applications

- TWS charging case
- Wireless microphone
- Smart Glasses

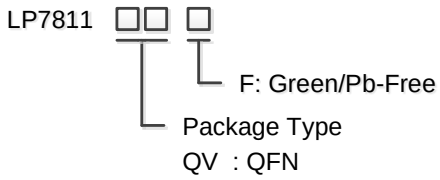
General Description

The LP7811 is an advanced TWS charging case management IC targeting to improve the total battery run time of the TWS earphones. The IC features a switching charger protects up to 30V input voltage and digitally programmable up to 1.7-A charge current via an I2C bus. The smart discharge voltage management feature tries to maximize the battery run time with ultra-low dropout charging scheme. The VOL and the VOR outputs track the battery voltages of the earphones when operating together with the companion linear charger (LP408X) in the earphone, minimizing the power loss. An NTC interface is offered to manage the charge and discharge operation based on the battery temperature sensed by the NTC resistor. Additional silicon temperature management ensure the safe operation. Earphone insertion and removal detections simplify the design of the earphone detection. The IC supports two independent bidirectional communication bus to the left and right earphone. An I2C bus is offered for programmability and flexibility of the device.

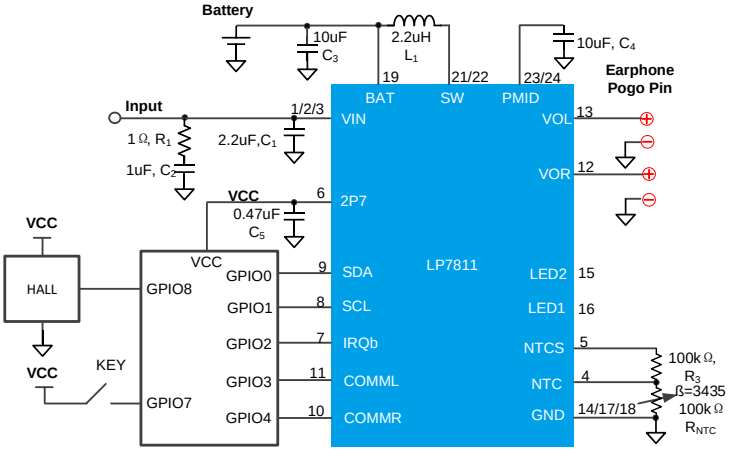
The quiescent current is 5-uA in standby mode.

The whole system is in a small 24-pin 4x4 QFN package.

Order Information



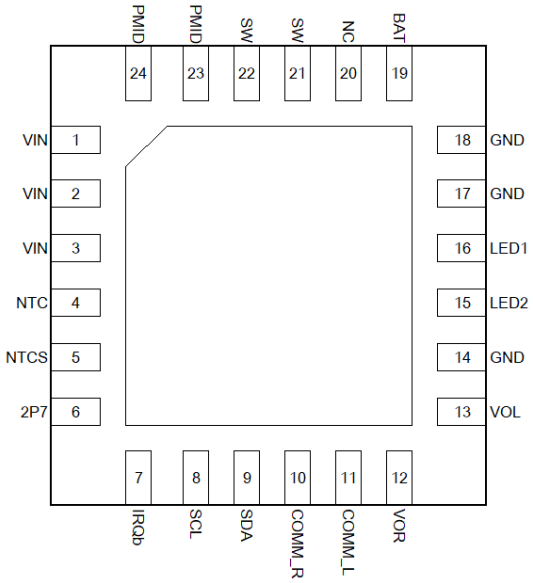
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	MSL
LP7811QVF	LPS LP7811 YWX	QFN-24	3K/REEL	LEVEL 3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. MSL: Moisture Sensitivity Level according to JEDEC Standard.				

Pin Diagram



LP7811 Pinout

Pin Description

Pin #	Name	Description
1，2，3	VIN	Input voltage that is connected to the positive input of the USB port. 30V maximum voltage rating. A 0.1uF or higher value input decoupling capacitor must be connected to this pin and the GND pin.
4	NTC	NTC input sense pin.
5	NTCS	2P7 load switch output. This pin is controlled by STD bit to connect or cutoff the power from the 2P7 pin.
6	2P7	Ultra-low power LDO ouput to power an external MCU. This supply is also used to bias the NTC circuit as well as the communication signal to the earphones.
7	IRQb	Interrupt open-drain output to the external MCU.
8	SCL	Clock line of the I2C bus.
9	SDA	Data line of the I2C bus.
10	COMM_R	Right earphone communication input/output
11	COMM_L	Left earphone communication input/output
12	VOR	Output to the right earphone.
13	VOL	Output to the left earphone.
14	GND	Ground. Must be connected with pin17,18 on PCB.

15	LED2	Open-drain LED output.
16	LED1	Open-drain LED output.
17，18	GND	Ground. Must be connected with pin14 on PCB.
19	BAT	Battery voltage sense pin of the charger.
20	NC	no connection.
21,22	SW	Switch node of the boost converter/ buck charger.
23,24	PMID	The power supply to the two current regulators to the left and the right earphones. A 10uF ceramic capacitor is required between this pin and the GND pin.
Thermal PAD		Connect to ground panel for thermal dissipation.

Absolute Maximum Ratings (Note)

VIN to GND ---------- -0.3V to 30V
Others to GND ---------- -0.3V to 6.5V
Operating Ambient Temperature Range (TA) ---------- -40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 45℃/W

Recommended Operating Conditions

Notes:
(1) All the values are effective capacitance or inductance.
(2) X5R and 16V or higher voltage rating are recommended.

Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	4.1		6.0	V
I_{CC}	Fast Charge Current	0.05		1.7	A
T_J	Operating Junction Temperature Range (T_J)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃
L	Output Inductance(1)	0.7	2.2	2.8	μH
C_{IN}	Input Capacitance (1) (2)	0.6	1	4.7	μF
C_{PMID}	PMID Capacitance(1) (2)	4	10	30	μF
C_{BAT}	BAT Capacitance(1) (3)	4	10	20	μF

(The specifications are at $V_{VIN\_UVLO} < V_{VIN} < V_{VIN\_OVP}$, L=2.2μH, T_J = -40°C to +85°C and T_J = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{VIN}	VIN quiescent current	VIN=5.0V，BAT=4.3V，NTC=10kΩ, EN_BST=1		250		μA
I_{Q_BAT}	Battery quiescent current	V_{BAT} = 4.5V, VIN pin floating,, EN_BST=0, PUP=00, STD=1		5		μA
		V_{BAT} = 4.5V, VIN pin floating,, EN_BST=0, PUP=00, STD=0		23		μA
INPUT VOLTAGE						
V_{VIN}	VIN operation range		4.1		6.0	V
V_{VIN_UVLO}	VIN UVLO threshold	VIN rising	3.7	3.85	4	V
V_{VIN_UVLO}	VIN UVLO	VIN falling		150		mV

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$_{HYS}$	hysteresis					
V_{VIN_OVP}	VIN OVP threshold	VIN rising	5.7	5.85	6.0	V
$V_{VIN\_OVP\_HYS}$	VIN OVP hysteresis	VIN falling		150		mV
$R_{dson,input}$	Input FET Rds,on	VIN=5V,		110		mΩ
I_{INLIM}	Input Current Limit	VIN=5V, ILIM[1:0]=01, 3A	2	3	4	A
V_{SCP_PMID}	PMID Short circuit protection threshold	VIN=5.0V, PMID falling edge		2.5		V
V_{SCP_HYS}	PMID Short circuit protection hysteresis	Hysteresis		200		mV
V_{POR}	POR threshold	battery voltage rising	2.0		2.6	V
V_{POR_HYS}	POR hysteresis	battery voltage falling		0.18		V
BUCK Charger Management						
V_{DPM_PMID}	PMID dynamic power management threshold	Reference to PMID, BUCK_DPM[1:0]=10		4.65		V
V_{TRK}	Trickle charge voltage threshold	battery voltage rising. VTRI[0]=1,25C	2.95	3.0	3.05	V
V_{TRK_HYS}	Trickle charge voltage hysteresis	battery voltage falling		100		mV
I_{TRK}	Trickle charge current	ITRI[2:0]=101	90	120	150	mA
		ITRI[2:0]=000	14	20	26	mA
I_{CC}	CC current	25°C, ICC[4:0]=10011, BAT=3.6V	-5%	1000	+5%	mA
		From -10°C to 85°C, ICC[4:0]=10011, BAT=3.6V	-10%	1000	+10 %	mA
		25°C, ICC[4:0]=01000, BAT=3.6V	-15%	450	+5%	mA
		25°C, ICC[4:0]=11111, BAT=3.6V	-10%	1700	+10 %	mA
V_{CV}	CV voltage	From -10°C to 85°C, BAT_CV[2:0]=010	-0.6		0.6	%
		25 °C, BAT_CV[2:0]=010	-0.4		0.3	%
	Re-charge threshold	falling edge, Reference to CV voltage		-150		mV
I_{TERM}	Charge termination current	ITERM[2:0]=101, From -10°C to 85°C,	90	120	150	mA
		ITERM[2:0]=000, From -10°C to 85°C,	14	20	30	mA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal foldback threshold		100	120	140	℃
f_{sw_buck}	Buck charger switching frequency	VIN=5.0V, BAT=3.8V, ICC=1.5A		1400		kHz
Earphone charge						
$R_{on,HS}$	High-side FET on-resistance	PMID=5.0V		70		mΩ
$R_{on,LS}$	Low-side FET on-resistance	PMID=5.0V		70		mΩ
I_{peak}	Boost mode peak current limit	BAT=3.6V, boost mode	1.4	2.0	2.6	A
I_{byp}	Bypass mode current limit	0ºC to 125ºC, PMID loaded, bypass mode	600	750		mA
f_{sw_boost}	Boost switching frequency	BAT=3.8V, PMID=5.0V		1100		kHz
V_{PMID}	Boost output voltage accuracy	VBST[2:0]=111，EN_BST=1 PMID=100mA load, 25 ºC	4.95	5.0	5.05	V
I_{PUP}	Insert detection current	1-μA pull up current, BAT=3.6V	0.9	1	1.1	uA
V_{INSERT}	Insert detection threshold	VIN floating, BAT=3.8V, BST_EN=0, reference to BAT voltage		-0.7		V
EICC	Earphone fast charge current	0℃ to 125℃, 250mA	225	250	275	mA
		0℃ to 125℃, 250mA	45	50	55	mA
EEOC	Earphone end of charge current threshold	EEOC=2mA	1	2	3	mA
		EEOC=10mA	7	10	13	mA
NTC Management						
T_{-10}	NTC -10℃ threshold	V_{NTC} voltage rising	80.4	81.2	81.9	%
T_{-10_HYS}	NTC -10℃ hysteresis	V_{NTC} voltage falling		1.5		%
T_0	NTC 0℃ threshold	V_{NTC} voltage rising	72.4	73.3	74.2	%
T_{0_HYS}	NTC 0℃ hysteresis	V_{NTC} voltage falling		1.5		%
T_{10}	NTC 10℃ threshold	V_{NTC} voltage rising	63.3	64.3	65.3	%
T_{10_HYS}	NTC 10℃ hysteresis	V_{NTC} voltage falling		1.5		%
T_{45}	NTC 45℃ threshold	V_{NTC} voltage falling	32.1	32.9	33.7	%
T_{45_HYS}	NTC 45℃ hysteresis	V_{NTC} voltage rising		2		%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{60}	NTC 60℃ threshold	V_{NTC} voltage falling	22.5	23.2	23.8	%
T_{60_HYS}	NTC 60℃ hysteresis	V_{NTC} voltage rising		2		%
2.7V always-on linear regulator						
V_{2P7}	LDO output voltage accuracy	BAT=3.8V, 2.7V	2.69	2.72	2.76	V
I_{2P7}	LDO output current capability		15			mA
Digital						
R_{UP}	VOL/R pull up resistor	2.7V, 500ohm pull up resistor		500		Ω
I_{DOWN}	VOL/R pull down current capability	PMID=5V， VOL/VOR=0.4V	10			mA
I_{LED}	LED pull down current capability	PMID=5V， VLED=0.4V	10			mA
I_{irqb}	IRQb pull down current capability	PMID=5V， VIRQb=0.4V	0.5			mA

Typical Characteristics

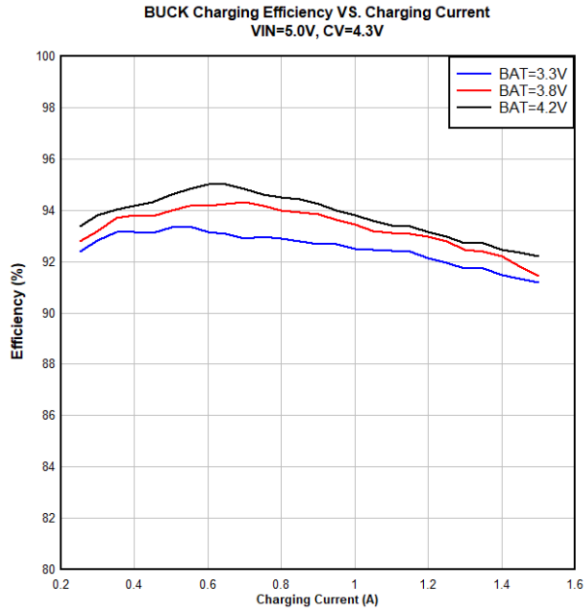


Figure 1. BUCK Charging Efficiency VS. Different Battery Voltage, VIN=5.0V, DCR_L=30mΩ, 2.2uH

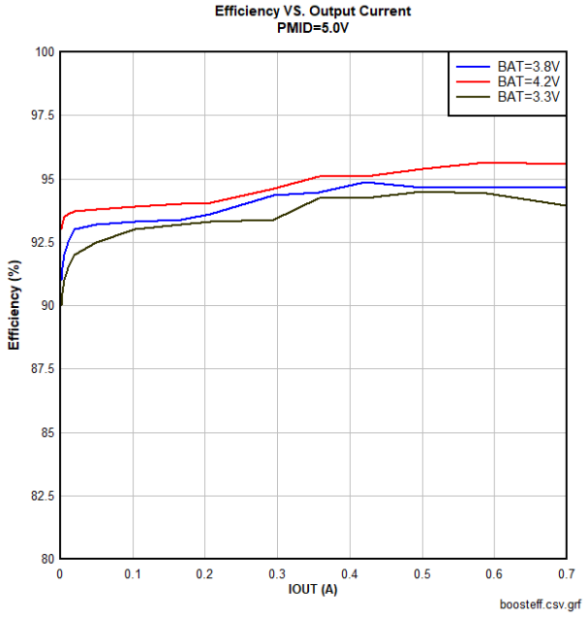


Figure 2. BOOST Efficiency VS. Different Battery Voltage, PMID=5.0V, DCR_L=30mΩ, 2.2uH

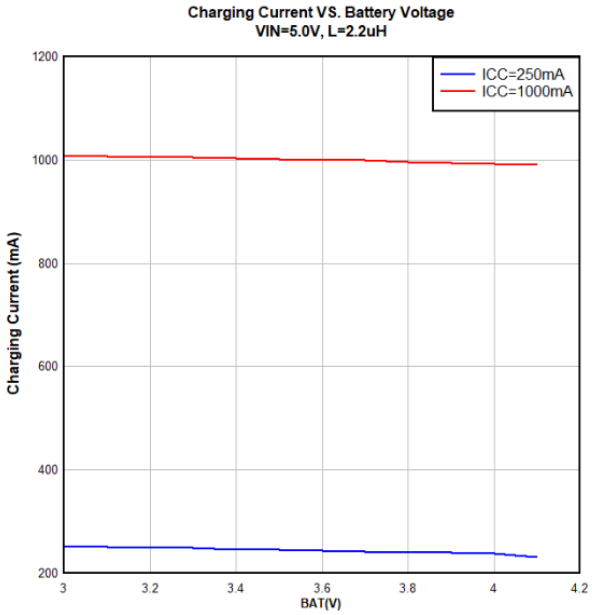


Figure 3. BUCK Charging Current VS. Battery Voltage, VIN=5.0V, DCR_L=30mΩ, 2.2uH

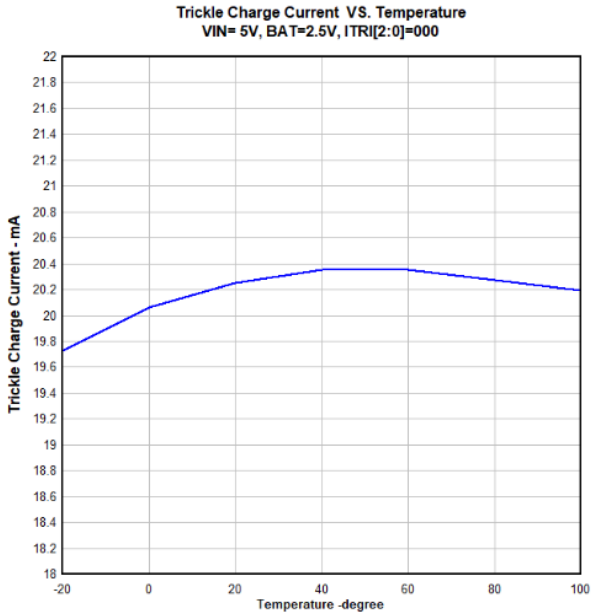


Figure 4. Trickle Charge Current VS. Temperature

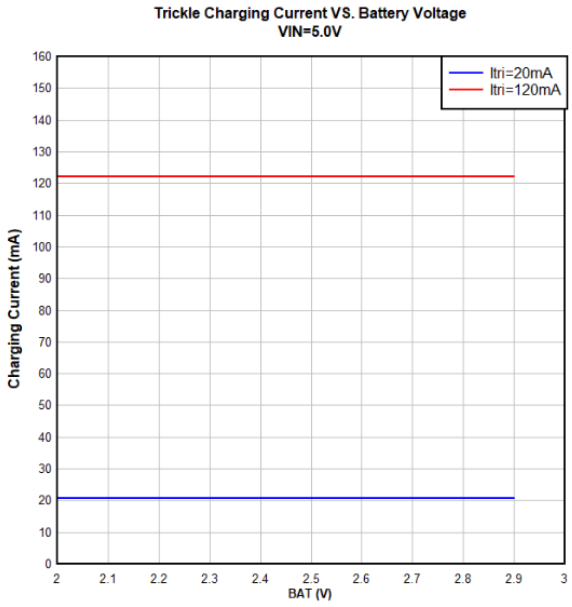


Figure 5. Trickle Charging Current VS. Battery Voltage

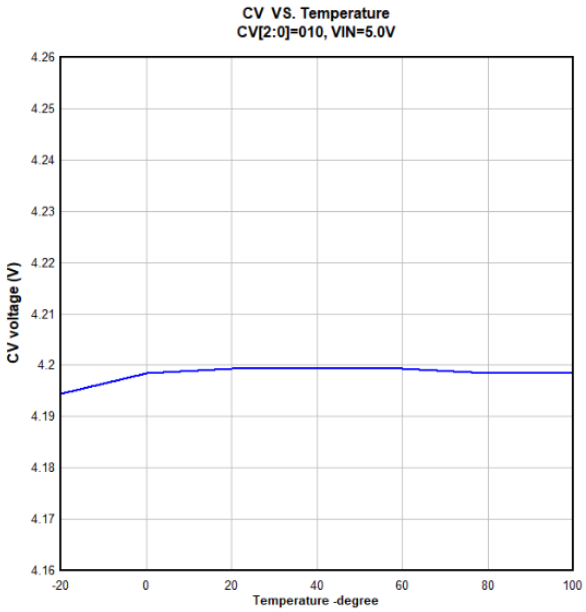
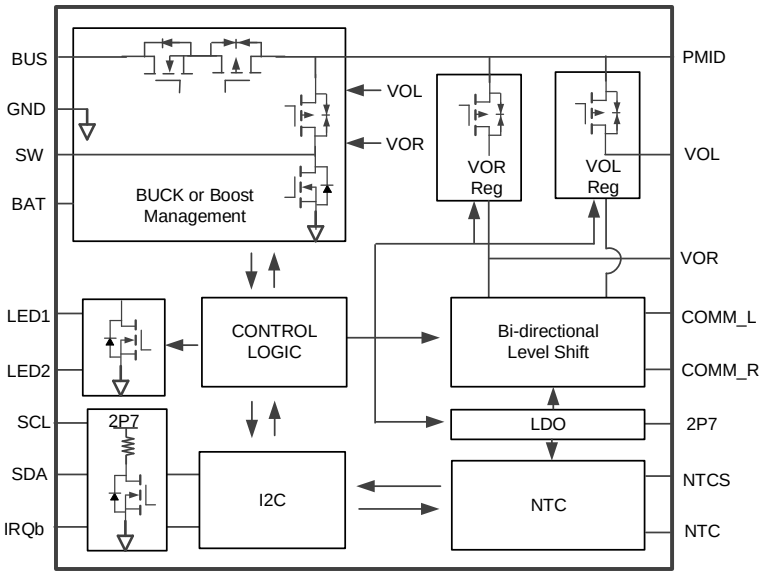


Figure 6. Floating Voltage VS. Temperature

Functional Block Diagram



Detailed Description

Overview

The LP7811 is a TWS charging case management IC that will extend the battery run time when worked together with dedicated battery chargers in the earphone. The LP7811 works as a BUCK charger or boost converter according to different scenarios. The LP7811 also integrates two earphone chargers to charge the earphones. When a valid power supply is connected to the VIN pin, the LP7811 is configured as a switching BUCK charger and charge the battery in the charging case. The LP7811 can also supply the earphone batteries at the same time. When no valid input power supply at VIN pin, the LP7811 is configured as a reverse boost regulator and provides power for the earphones automatically. Two earphone detection circuits allow an easy detection of the insertion of the left and the right earphones. A programmable linear regulator is offered to power an external MCU or sensors. The linear regulator will always be on as long as either the VIN or the BAT pin is powered. An NTC management circuit detects five thresholds to accommodate the compliance of the JIETA guidelines. The LP7811 supports bi-directional communication between the charging case and the earphones with both 5V or 2.7V logic. Two GPIOs can be used to drive two external LEDs. Various charging parameters are programmable via an I2C bus and an IRQb interrupt output is provided to interrupt the MCU when an interruptible event occurs.

The LP7811 can be configured to enter standby mode when the device is not in operation. The standby current from the case battery is 5-μA typically.

Power-on Reset (POR)

When either the BAT rises above the BAT_POR threshold or the VIN rises above the VIN_UVLO threshold during assembly, the LP7811 will perform a power-on reset. All registers will be set to the default values. The external MCU can access all the registers after POR. The POR register is set to 1 after power on reset operation. The MCU should write this register to 0 after POR to avoid missing the new POR event notification.

The register values are kept until both the BAT and VIN pin falls below the UVLO thresholds accordingly.

Input Section

The VIN voltage is monitored by the internal resistor divider. The input load switch will be shutdown and both the reverse blocking NMOS FETs are turned off when the VIN falls below the UVLO threshold V_{VIN_UVLO} or rises above the OVP threshold V_{VIN_OVP}. Both the UVLO and OVP comparators have a typical 100-mV hysteresis.

The LP7811 outputs a power good indication when the input voltage is below V_{VIN_OVP} and above the V_{VIN_UVLO}, the reverse blocking FETs are turned on after 100-us deglitch time. An interrupt is sent out on IRQb pin after another typical 20-ms deglitch time.

The input power switch integrates soft-start and over current protection as well. The input current limit threshold is programmable in the reg 07H and the default current limit is disabled. When the PMID is overloaded, the PMID_OL bit in the status register is set to 1 and the interrupt is sent to the master MCU by IRQb pin at the same time. The LP7811 enters hiccup protection mode when the PMID drops lower than 2.5-V. The power paths are all shutdown for 200-ms, including: the input load switch, bi-direction buck/boost power stage, and earphone charging paths. The input load switch tries a new soft-start after the hiccup protection time.

The reverse current protection is implemented in the load switch as well.

Charge Management

The LP7811 integrates a switching charger with three charging modes, i.e., trickle, constant current (CC), and constant voltage (CV) modes. The EN_CHG bit can enable the charger. The default value is of EN_CHG is 0 and the host MCU can enable the charger by I2C. The charger starts charging when all the conditions below are valid:

1. The input voltage is in the range of 2.7V to 6V
2. The EN_CHG bit is set to 1.
3. PMID is 100mV higher than the BAT voltage

4. BAT voltage is below the CV voltage.
5. the NTC is in the range of 0 °C to 45 °C

The LP7811 monitors the battery voltage and regulates the charging current and voltage accordingly after start charging.

1. **Trickle charge:** The trickle-charge current and voltage are programmable. The default trickle-charge voltage threshold is 3.0V and the default trickle charge current is 20mA.
2. **CC charge:** The LP7811 starts constant current (CC) charging when the battery voltage is higher than the trickle charge threshold but lower than the constant voltage (CV) threshold. The CC current is programmable between 50mA to 1.7A with 50mA/step. Its value is determined by the fast charge current set register in the reg 06H. The default value is 250mA.
3. **CV charge:** The LP7811 starts constant voltage (CV) charging when the battery voltage rises above the CV threshold. The charging decreases gradually until the charging termination is triggered in this phase. The CV voltage is programmable via the CV set register in the reg 06H. The default value is 4.2V.
4. **Termination:** Charge terminates when the charge current reaches the value set by the termination current and the battery voltage is higher than the recharge threshold. The termination current is programmable via the termination current set register in the reg 07H. The default value is 20mA.
5. **Recharge:** A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage.
6. **Charge current foldback** : When the die temperature reaches 120°C, the charger current decreases until a new temperature balance is reached.
7. **Dynamic power management**: The PMID voltage is monitored and the DPM threshold is programmable from 4.45V~ 4.75-V in the reg 0CH to avoid the system crash caused by the bad input power supply. The default value is 4.65V.
8. **Battery voltage monitor:** The LP7811 integrates a 4-bit ADC to convert the battery voltage every 100-ms. The internal register stores the battery voltage information (from 2.9V to 4.4V with 100mV/step).

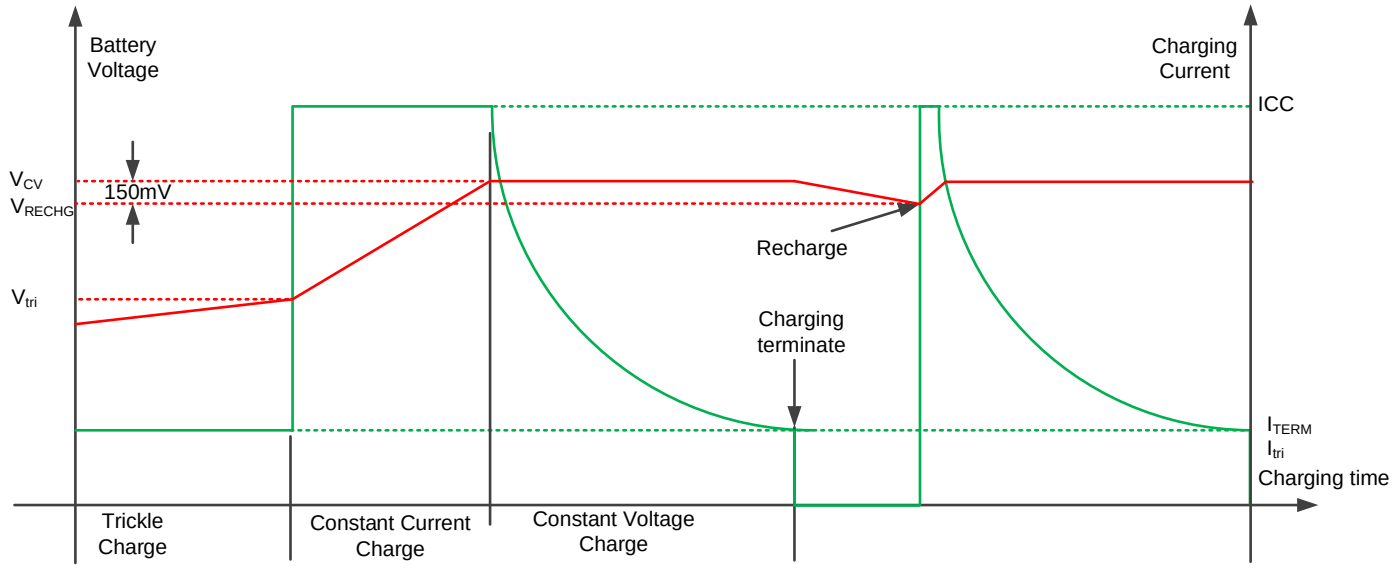


Figure 7. Charging Profile

Earphone Charger

Earphone Detection

An internal programmable 1uA to 20uA pull-up current source is offered for earphone insertion or removal detection.

Insertion detection: When the earphone is not in the charging case, the 1μA pull up current will pull the VOL/R pin to

the higher voltage of BAT and PMID. The EN_VOL/R bit should be set to 0 when the pull up current is enabled. When an earphone is inserted, the input pull-down resistor or quiescent current in the earphone will pull the VOL/R pin to low. Once the VOL/R falls 0.7-V below the setting voltage after a 20ms deglitch time, the earphone insertion is detected and an interrupt (iL_inserted or iR_inserted) will be sent to the MCU through the IRQb pin.

Removal detection: Once the VOL/R recovers to less than 0.5-V below the PMID or BAT voltage with a 20ms deglitch time, the earphone removal is detected and an interrupt (iREM_L or iREM_R) will be sent to the MCU and the L/R_insert bit is cleared at the same time.

The removal of the earphone interrupt should be masked when the EN_VOL/R is set to 1. The L/R_insert bit is cleared once the EN_VOL/R bit is set.

Earphone short circuit detection: iSCP_L/R are triggered when the VOL/R pins are pulled to lower than 0.7V threshold with 1ms deglitch time.

Boost Regulator

The LP7811 integrates a 2-uA typical ultra-low quiescent current regulator. The maximum output current is up to 1A.

1. **Boost Converter Operation:** The boost regulator has two operation modes. It operates in the voltage step-up mode when the PMID voltage is required to be higher than the case battery voltage. It operates in a by-pass mode when the PMID voltage is required to be lower or equal to the battery voltage. The maximum boost regulator output voltage is programmed by the Maximum Output Voltage of Boost Converter register. The range is between 4.2V- 5.0V.
2. **Feedback selection:** The higher voltage of the VOL and VOR will be selected to set the reference for the PMID output, however, when either VOL or VOR channel is not in the charge mode, that channel of feedback can be disconnected. The disconnection can be performed by setting FBK_L or FBK_R bit to 0. The PMID is regulated at a voltage setting by the Maximum Output Voltage of Boost Converter register when both the FBK_L and FBK_R bit are set to 0.
3. **Battery Under Voltage Lockout (BAT_UV):** The LP7811 integrates battery over discharge protection as well. Discharge will stop when the battery voltage drops below the Battery Discharging Undervoltage Control register, this voltage is programmable in the register BAT_UV[2:0]. The LP7811 enters standby mode when the battery is under BAT_UV threshold and the VIN is not valid at the same time.
4. **Current Limit and Hiccup Operation:** The LP7811 supports current limit protection both in boost mode and bypass mode. The peak current is limited to 2A when LP7811 is in boost mode and the current flow the high-side FET of the boost regulator is limited to 750mA when PMID is lower than the BAT. The LP7811 shuts down the boost converter if the overload condition lasts 1.2-ms typical time and the PMID_OL bit will be set when 1.2-ms expires. After a 30ms hiccup time, the boost converter will perform a new startup.
5. **Enable and Disable:** The EN_BST bit in the Charge Control Register enables the boost regulator. When EN_BST is low, the boost regulator is disabled. When the boost regulator is enabled, it will go through a new soft-start.

Earphone fast charge (EICC) and EEOC

The VOL and the VOR pins provide power to charge the left and the right earphone batteries.

The charging of the earphones is enabled by the EN_VOL or EN_VOR bit. The EN_BST bit needs be set at the same time to enable the boost regulator. The charging current is programmed by the Earphone Charge Current Control Register.

The EOC_L/R bit is set when the charging current of the earphone drops to 2mA or 10mA, programmable by the EEOC bit in the Earphone Charge Control register, if the VOL/R voltage is higher than a set threshold (4V typically) at the same time. The iEOC_L/R interrupt is sent to the MCU when the EOC_L/R happens.

Bi-directional Communication

Bi-directional communication to the earphone is supported in the LP7811. Two independent communication channels support UART or one-wire codes. The L_TX bit enables the transmission of the signals to the earphones from the COMM_L pin to the VOL pin while the L_RX bit enables the signals from the earphone to the COMM_L pin. The pull-up voltage for the communication is selectable by the I2C bus to the PMID voltage or the LDO output to support selectable 5V or 2.7V communication. The pull-up is enabled by the L_PUP and the R_PUP bits.

A communication session is always started by the MCU in the charging case sending a request first. Typically, the MCU

will first pull the COMM_L pin to low for a certain amount of time (controlled by the MCU) to reset the VOL/R communication line. The duration of such a low signal allows the circuit in the earphone to stop charging build the communication bus on the earphone side. After the bus reset, the MCU will pull the COMM_L pin high to start the STOP bit of the UART communication protocol.

The communication baud rate is configurable by setting different pull up resistor as shown in the table.

Table 1 UART communication baud rate configuration

VSEL	Pull-up resistor	Capacitor at VOL pin	Recommend baud rate
2.7V	500Ω	no connection	2Mbps
2.7V	1000Ω	no connection	1Mbps
PMID	2500Ω	no connection	500kbps

NTC Management

When the charging case is in the charge mode or discharge mode, the NTCS outputs the 2P7 bias voltage for the external resistive divider. An NTC resistor with 1% accuracy and with a beta of 3435 is recommended. The NTCS disables the output during the standby mode to reduce the quiescent current. Five thresholds are achieved: -10°C, 0°C, 10°C, 45°C, and 60°C temperature threshold detection. An iNTC interrupt will be sent when the temperature is crossing these thresholds for MCU to take actions according to the temperature.

The NTC [2:0] bits are used to indicate the temperature range in the status register. The MCU can change the charging parameters or disable the charging operations by using the control registers.

The linear charger is forced to be turned off when the temperature is outside the range of 0°C to 45°C.

The NTC[2:0] will be set to 011 when the LP7811 is in standby mode.

2P7 Output

The 2P7 output is an always-on linear regulator output that is powered by either the VIN or the BAT pin. This output is to power the external MCU, the NTC circuit, the internal logic circuit, and the 2.7V communication circuit. A 0.1~0.47-uF external ceramic capacitor is required. The LDO output voltage is programmable in the reg 09H from 2.7V to 3.3V.

Standby Mode

The LP7811 enters standby mode when STD bit is set to 1 in the reg 0CH. This function is only valid when the USB is not present at VIN. Most internal control circuit are disabled in standby mode to save power. The boost converter is still available in standby mode but the earphone charge function is forced off. The LDO and the communication interface are still available as well, including the I2C and UART communication. The total quiescent current is 5uA in standby mode.

The battery voltage monitor register can still be updated in this mode but the NTC is disabled in standby mode.

LED Outputs

Two LED outputs are offered that can be controlled by the I2C bus. Each pin has 10mA current capability.

The LED1/2 outputs support breathing mode when the LED1[1:0] or the LED2[1:0] in the register 0CH is set to 10. The breathing frequency is fixed at 0.5Hz with 100Hz resolution.

The LED outputs support flash mode as well with a typical 2Hz flash when the LED1/2 register is set to 11.

Thermal Shutdown

When the internal junction temperature of LP7811 exceeds the thermal shutdown threshold of 150° C, the LP7811 disables all the power paths. The linear charger, boost converter and VOL/VOR all will be disabled.

I2C Bus and Interrupt

The LP7811 has an I2C bus with an interrupt IRQb pin and internal registers. The LP7811 operates as a slave device and the I2C slave address is 6BH (7bit, **1101011**), a 1 or 0 should be placed at the end of the address which represents read or write operation. The interrupt pin IRQb is an open-drain output that pulls to low when an interruptible event happens in the chip. All of the SDA, SCL and IRQb have internal pull up resistor and no external resistor is needed,

Receiving control inputs from the master device reads and writes the internal registers 00H through 09H. The LP7811 supports both standard mode(100kbps) and fast mode(400kbps). Both SDA and SCL are pulled up to 2V7 pin with a typical 5.1-k ohm resistor internally.

DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

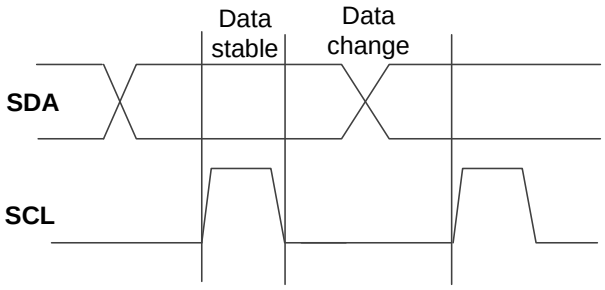


Figure 8. I2C Data validity

Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the SDA line while the SCL is high means a data transfer starts. A rising edge on the SDA line while the SCL is at high means a data transfer stops.

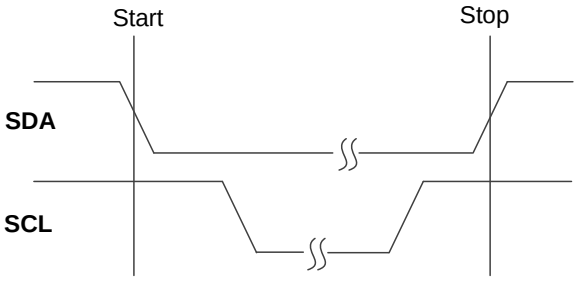


Figure 9. I2C Start and Stop Conditions

Byte format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 10. Single-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK
							8 bit	1bit	1bit
							Data from Address	NACK	STOP

Figure 11. Single-byte Read

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit								
START	Slave address	0	ACK	Register address	ACK	START								
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit			
				Data to Address	ACK	Data to Address	ACK	.....	Data to Address	ACK	stop			

Figure 12. Multi-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1

8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit
Data from Address	ACK	Data from Address	ACK	.....	Data from Address	NACK	stop

Figure 13. Multi-byte Read

Register Maps

Table 2 Device Registers

Reg	Addr	R/W	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Value
Reg 0	00H	R	NTC			PMID_OL	EOC_R	EOC_L	CHG	PGD	6C
Reg 1	01H	R	L_SCP	R_SCP	L_insert	R_insert	V_BATM				00
Reg 2	02H	R/C			iRem_R	iRem_L	iSCP_R	iSCP_L	iBAT_UV	iTSD	00
Reg 3	03H	R/C	iINS_R	iINS_L	iEOC_R	iEOC_L	iPMID_OL	iNTC	iCHG	iPGD	00
Reg 4	04H	R/W			mRem_R	mRem_L	mSCP_R	mSCP_L	mBAT_UV	mTSD	00
Reg 5	05H	R/W	mINS_R	mINS_L	mEOC_R	mEOC_L	mPMID_OL	mNTC	mCHG	mPGD	00
Reg 6	06H	R/W	BAT_CV			ICC					44
Reg 7	07H	R/W	ILIM		ITERM			ITRI			C0
Reg 8	08H	R/W	BYP	BAT_UV			VBST			VTRI	3F
Reg 9	09H	R/W	V_LDO		FBK_R	FBK_L	EN_VOR	EN_VOL	EN_BST	EN_CHG	30
Reg 10	0AH	R/W	PUP_RES	R_PUP	L_PUP	VSEL	R_RX	L_RX	R_TX	L_TX	00
Reg 11	0BH	R/W	PUP		EEOC	EICC					44
Reg 12	0CH	R/W	STD	BUCK_DPM		LED2		LED1		POR	41

Note: **R**: read only; **R/C**: read and clear; **R/W**: read and write

Status Register 0 /Address: 00H (default: 0x6C)

Table 3 Status register 0

Bit	Symbol	Description	Read/Write	Default
7	NTC[2]	NTC temperature range: 000: <-10 °C, 001: -10 °C~0 °C, 010: 0 °C~10 °C, 011: 10 °C~45 °C, 100:45°C~60 °C, 101~111:>60 °C	r	011
6	NTC[1]		r	
5	NTC[0]		r	
4	PMID_OL	=1 PMID output over-loaded.	r	0
3	EOC_R	=1 when the right earphone is end of charge (VOR higher than 4V and current less than 2/10mA)	r	1
2	EOC_L	=1 when the left earphone is end of charge (VOL higher than 4V and current less than 2/10mA)	r	1
1	CHG	=1 when charger is in trickle, CC, or CV mode.	r	0
0	PGD	=1 when input is between UVLO and OVP.	r	0

Status Register 1 /Address: 01H (default: 0x 00)

Table 4 Status register 1

Bit	Symbol	Description	Read/Write	Default
7	L_SCP	1: left earphone short circuit	r	0
6	R_SCP	1: right earphone short circuit	r	0
5	L_insert	1: left earphone insertion	r	0
4	R_insert	1: right earphone insertion	r	0
3	V_BATM[3]	Case battery voltage: 0000:<2.9V, 0001:3.0V, 0010:3.1V, 0011:3.2V 0100:3.3V, 0101:3.4V, 0110:3.5V, 0111:3.6V 1000:3.7V, 1001:3.8V, 1010:3.9V, 1011:4.0V	r	0
2	V_BATM[2]		r	0
1	V_BATM[1]		r	0

0	V_BATM[0]	1100:4.1V, 1101:4.2V, 1110:4.3V, 1111:>4.4V	r	0

Interrupt Register/Address: 02H (default: 0x00).

Table 5 Interrupt register

Bit	Symbol	Description	Read/Write	Default
7		RESERVE		
6		RESERVE		
5	iREM_R	right earphone removal interrupt	r/c	0
4	iREM_L	left earphone removal interrupt	r/c	0
3	iSCP_R	right earphone short circuit interrupt	r/c	0
2	iSCP_L	left earphone short circuit interrupt	r/c	0
1	iBAT_UV	battery UVLO protection interrupt	r/c	0
0	iTSD	thermal shutdown interrupt	r/c	0

Interrupt Register/Address: 03H (default: 0x00).

Table 6 Interrupt register

Bit	Symbol	Description	Read/Write	Default
7	iINS_R	right earphone insert interrupt	r/c	0
6	iINS_L	left earphone insert interrupt	r/c	0
5	iEOC_R	Right earphone EOC interrupt, rising edge	r/c	0
4	iEOC_L	Left earphone EOC interrupt, rising edge	r/c	0
3	iPMID_OL	PMID overload interrupt, rising edge	r/c	0
2	iNTC	NTC cross range or thermal shutdown	r/c	0
1	iCHG	Case charging status change, rising/falling	r/c	0
0	iPGD	Input voltage status change, rising/falling	r/c	0

Interrupt Mask Register/Address: 04H (default: 0x00)

Table 7. Interrupt mask register

Bit	Symbol	Description	Read/Write	Default
7			r/w	0
6			r/w	0
5	mREM_R		r/w	0
4	mREM_L		r/w	0
3	mSCP_R		r/w	0
2	mSCP_L		r/w	0
1	mBAT_UV		r/w	0
0	mTSD		r/w	0

Interrupt Mask Register/Address: 05H (default: 0x00)

Table 8. Interrupt mask register

Bit	Symbol	Description	Read/Write	Default
7	mR_ins		r/w	0
6	mL_ins		r/w	0
5	mEOC_R		r/w	0
4	mEOC_L		r/w	0
3	mBST_OL		r/w	0
2	mNTC		r/w	0
1	mCHG		r/w	0
0	mPGD		r/w	0

Control Register 0/Address: 06H (default: 0x44)

Table 9 Control Register0

Bit	Symbol	Description	Read/Write	Default
7	BAT_CV[2]	Constant voltage set: 000: 4.0V 001:4.1V 010:4.2V 011:4.3V 100: 4.35V 101:4.38V 110:4.4V 111:4.425V	r/w	4.2V(010)
6	BAT_CV[1]		r/w	
5	BAT_CV[0]		r/w	
4	ICC[4]	Constant charge current set: 00000:50mA,00001:100mA,00010:150mA,00011:200mA 00100:250mA,00101:300mA,00110:350mA,00111:400mA 01000:450mA,01001:500mA,01010:550mA,01011:600mA 01100:650mA,01101:700mA,01110:750mA,01111:800mA 10000:850mA,10001:900mA,10010:950mA,10011:1A 10100:1.05mA,10101:1.1A,10110:1.15A, 10111:1.2A 11000:1.25A,11001:1.3A,11010:1.35A, 11011:1.4A 11100:1.45A,11101:1.5A,11110:1.55A, 11111:1.7A	r/w	250mA (00100)
3	ICC[3]		r/w	
2	ICC[2]		r/w	
1	ICC[1]		r/w	
0	ICC[0]		r/w	

Control Register1 /Address: 07H (default: 0X C0)

Table 10. Control Register 1

Bit	Symbol	Description	Read/Write	Default
7	ILIM[1]	Input current limit set: 00: 2.5A, 01:3.0A, 10: 4.0A, 11: no input current limit	r/w	no current limit (11)
6	ILIM[0]		r/w	
5	ITERM[2]	Termination current set: 000:20mA, 001:40mA, 010:60mA, 011:80mA,100:100mA, 101:120mA, 110~111: not valid	r/w	20mA (000)
4	ITERM[1]		r/w	
3	ITERM[0]		r/w	
2	ITRI[2]	Trickle charge current set: 000:20mA, 001:40mA, 010:60mA, 011:80mA, 100:100mA, 101:120mA, 110~111: not valid	r/w	20mA (000)
1	ITRI[1]		r/w	
0	ITRI[0]		r/w	

Control Register2 /Address: 08H (default: 0x3F)

Table 11. Control Register 2

Bit	Symbol	Description	Read/Write	Default
7	BYP	Earphone charge mode set: 1: 5V bypass without current limit, 0: with current limit	r/w	0
6	BAT_UV[2]	Boost UVLO set: 000:2.8V, 001:2.9V, 010:3.0V, 011:3.1V, 100:3.2V,101:3.3V, 110:3.4V, 111:3.5V	r/w	3.1V (011)
5	BAT_UV[1]		r/w	
4	BAT_UV[0]		r/w	
3	V_BST[2]	Boost output voltage set: 000:4.2V, 001:4.3V, 010:4.4V, 011:4.5V, 100:4.6V,101:4.7V, 110:4.8V, 111:5.0V	r/w	5.0V (111)
2	V_BST[1]		r/w	
1	V_BST[0]		r/w	
0	VTRI	Trickle charge voltage set: 1: 3.0V, 0:2.8V	r/w	1

Control Register 3 /Address: 09H (default: 0x30)

Table 12 Control Register3

Bit	Symbol	Description	Read/Write	Default
7	V_LDO[1]	Ultra-low power LDO output voltage set: 00: 2.7V, 01:2.8V, 10:3.0V, 11:3.3V	r/w	0
6	V_LDO[0]		r/w	0
5	FBK_R	Right earphone feedback enable 0=off, 1=on	r/w	1
4	FBK_L	Left earphone feedback enable 0=off, 1=on	r/w	1
3	EN_VOR	1: Right earphone charging enable	r/w	0
2	EN_VOL	1: Left earphone charging enable	r/w	0

1	EN_BST	1: Boost regulator enable	r/w	0
0	EN_CHG	1: Charge enable.	r/w	0

Control Register 4 /Address: 0AH (default: 0x00)

Table 13 Control Register4

Bit	Symbol	Description	Read/Write	Default
7	PUP_RES	VOL/VOR communication pull-up resistor, 0=500ohm, 1=1000ohm	r/w	0
6	R_PUP	1: VOR communication pull-up enabled.	r/w	0
5	L_PUP	1: VOL communication pull-up enabled.	r/w	0
4	VSEL	pull-up bias voltage: PMID or 2P7 voltage 0 = 2P7, 1=PMID	r/w	0
3	R_RX	1: right earphone receive data enable	r/w	0
2	L_RX	1: left earphone receive data enable	r/w	0
1	R_TX	1: right earphone transmit data enable	r/w	0
0	L_TX	1: left earphone transmit data enable	r/w	0

Control Register 5 /Address: 0BH (default: 0x44)

Table 14 Control Register5

Bit	Symbol	Description	Read/Write	Default
7	PUP[1]	Pull up current for earphone insert detection: 00: off, 01: 1uA, 10: 7uA, 11: 20uA	r/w	0
6	PUP[0]		r/w	1
5	EEOC	Earphone charge current EOC threshold set: 0: 2mA or 1:10mA	r/w	0
4	EICC[4]	High accuracy earphone charge current set: 00000:30mA, 00001:35mA, 00010:40mA, 00011:45mA, 00100:50mA, 00101:55mA, 00110:60mA, 00111:65mA,01000:70mA, 01001:75mA, 01010:80mA, 01011:85mA 01100:90mA, 01101:95mA, 01110:100mA, 01111:105mA,10000:110mA, 10001:115mA, 10010:120mA, 10011:130mA,10100:140mA, 10101:150mA, 10110:160mA, 10111:170mA 11000:180mA, 11001:190mA, 11010:200mA, 11011:210mA,11100:230mA, 11101:250mA, 11110:275mA, 11111:300mA	r/w	50mA (00100)
3	EICC[3]		r/w	
2	EICC[2]		r/w	
1	EICC[1]		r/w	
0	EICC[0]		r/w	

Control Register 6 /Address: 0CH (default: 0x41)

Table 15 Control Register6

Bit	Symbol	Description	Read/Write	Default
7	STD	1: LP7811 enters standby mode	r/w	0
6	BUCK_DPM[1]	BUCK DPM voltage set 00:4.45V 01:4.55V, 10:4.65V, 11:4.75V	r/w	4.65V (10)
5	BUCK_DPM[0]		r/w	
4	LED2[1]	00: LED2=OFF; 01: LED2=ON: 10: LED2 breathing 100Hz, 11: LED2 flash.	r/w	0
3	LED2[0]		r/w	0
2	LED1[1]	00: LED1=OFF; 01: LED1=ON: 10: LED1 breathing 100Hz, 11: LED1 flash.	r/w	0
1	LED1[0]		r/w	0
0	POR	1: power on reset indication, MCU should write to 0 after POR. Write 1 to this bit is not valid.	r/w	1

Application Information

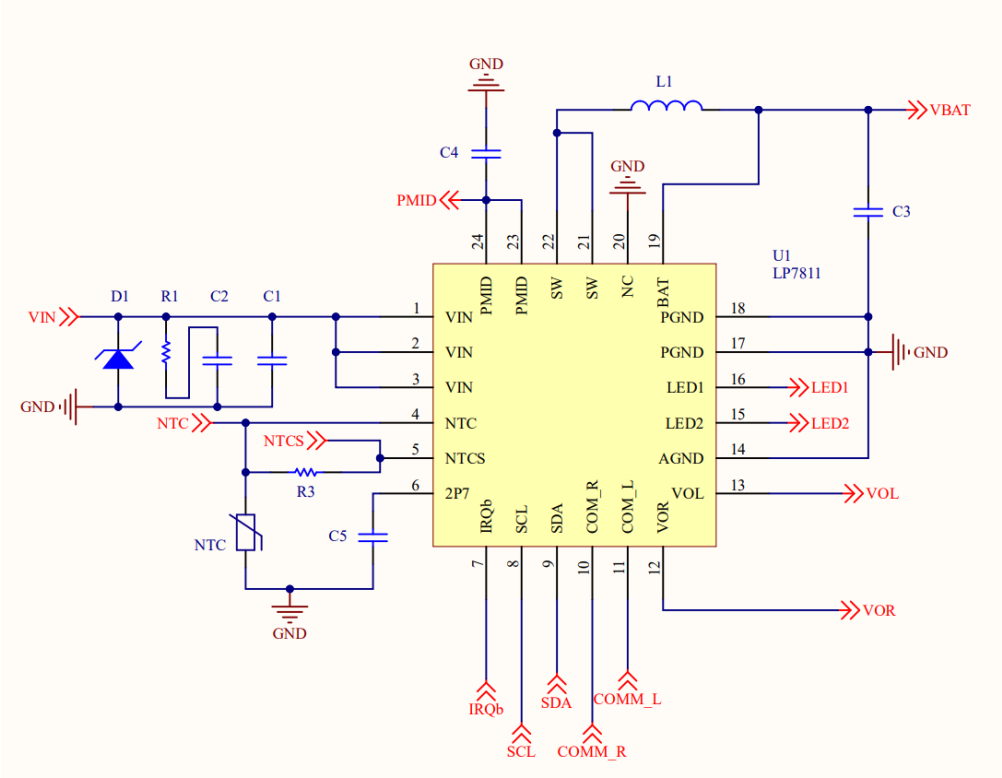


Figure 14. Typical Application circuit

A typical application consists of the multi-function-in-one power management IC of LP7811 and a host MCU. When powering up in default mode, the battery CV voltage of LP7811 is 4.2V, the constant charging current is 250mA, the termination current and trickle charge current are 20mA. The maximum output voltage of boost converter is 5.0V and the discharge undercharge threshold is 3.3V. The MCU can change all the default values by I2C interface.

Capacitor selection:

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the VIN, BAT, 2P7 and PMID pin to the GND pin. The VIN capacitor C_1 should be 50V rating with minimum 2.2uF capacitance. The BAT capacitor C_3 should be at least 6.3V rating with minimum 10uF capacitance. The PMID capacitor C_4 should be at least 6.3V rating with minimum 10uF capacitance, this capacitor influences the right-half-plane-zero location of the boost converter and should not be too small. The 2P7 linear regulator capacitor C_5 should be at least 0.47uF to ensure the loop stability and MCU power stability. All the capacitors should be placed as close as possible to the pins.

Inductor selection:

The LP7811 is optimized to work with inductor values between 0.68uH and 2.2uH. For best stability consideration, a 1-uH and 2.2uH inductors are recommended. The peak current of the inductor should be higher than the saturation current from the inductor's datasheet. A low DCR inductor should be used to get a desired efficiency. As a recommendation, a 1-uH with a 30mΩ DCR inductor is a good choice for the 1.5A BUCK charging and 500mA output current application and a 2.2uH with a 60mΩ DCR inductor for the 0.8A BUCK charging.

NTC design:

As all the trigger point thresholds of the internal NTC comparators are well design with a certain type of NTC resistor, an 10-kΩ NTC resistor with 1% accuracy and with a beta of 3435 is recommended. The R1 should be set to 10-kΩ to cooperate with the 10-kΩ NTC resistor. The following equation helps calculating the trigger point when the NTC resistor changes. All the trigger point thresholds can be found in the electrical characteristics table. The default NTC threshold indicates the temperature of -10 °C, 0 °C, 10 °C, 45 °C,

60 °C. The NTC pin can't be left float, setting the R_3 and R_{NTC} to 2MΩ or higher if NTC is not used.

Typical Waveforms:

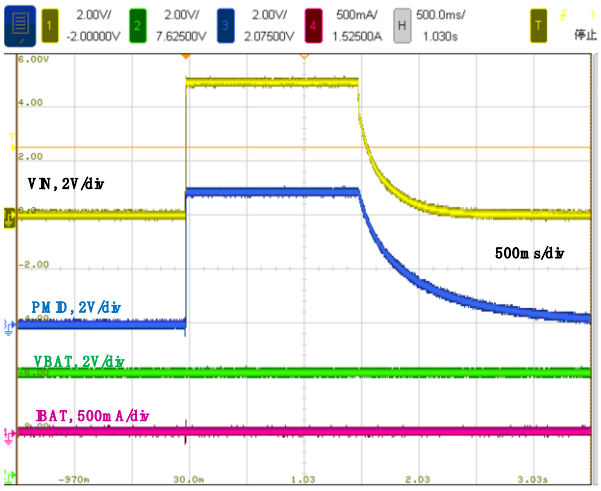


Figure 15. VIN plugged in and unplugged with EN_BST=0, EN_CHG=0，no load, BAT=3.6V

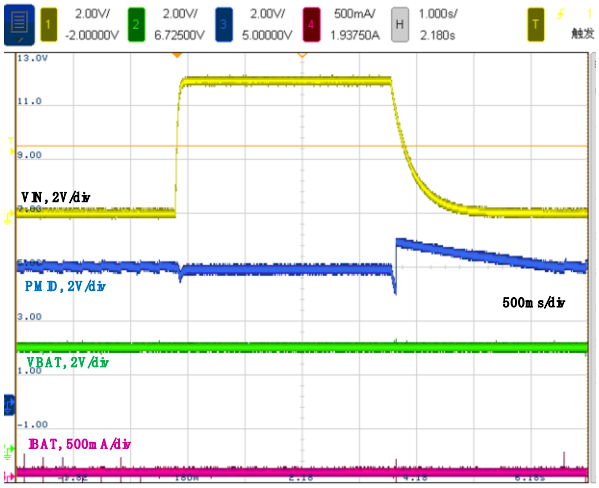


Figure 16. VIN plugged in and unplugged with EN_BST=1, EN_CHG=0，no load, BAT=3.6V

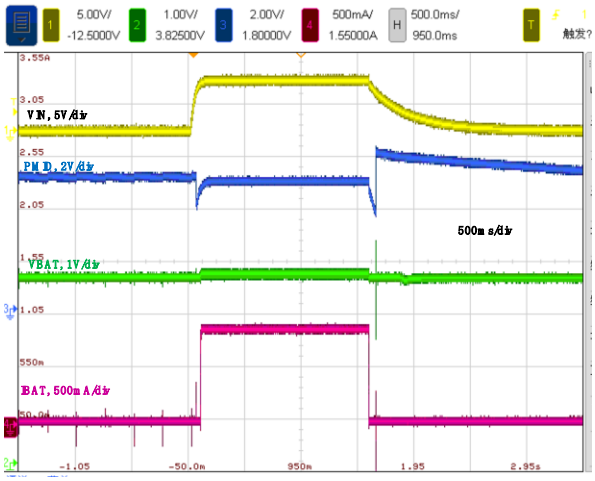


Figure 17. VIN plugged in and unplugged with EN_BST=1,EN_CHG=1,ICC=850mA, BOOST no load

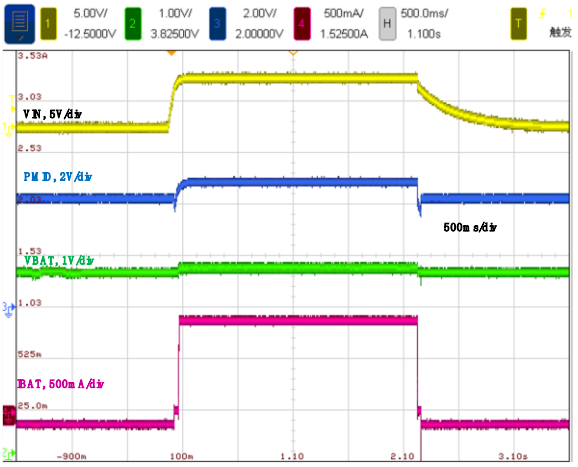


Figure 18. VIN plugged in and unplugged with EN_BST=1, EN_CHG=1, EN_VOL=1, ICC=850mA, VOL=3.9V, EICC=120mA

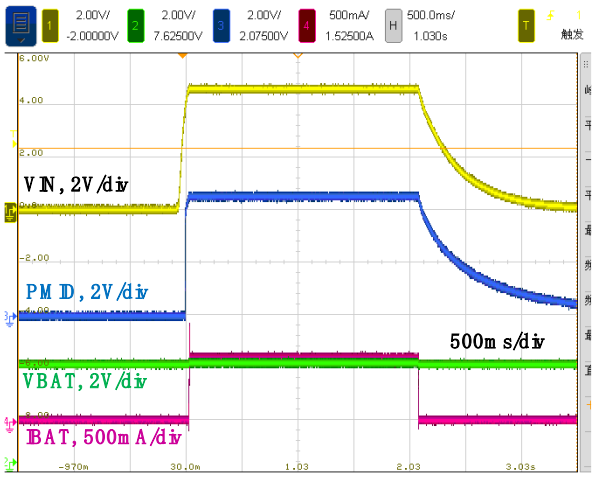


Figure 19. VIN plugged in and unplugged with VIN DPM, EN_BST=1,EN_CHG=1,ICC=850mA, BOOST no load

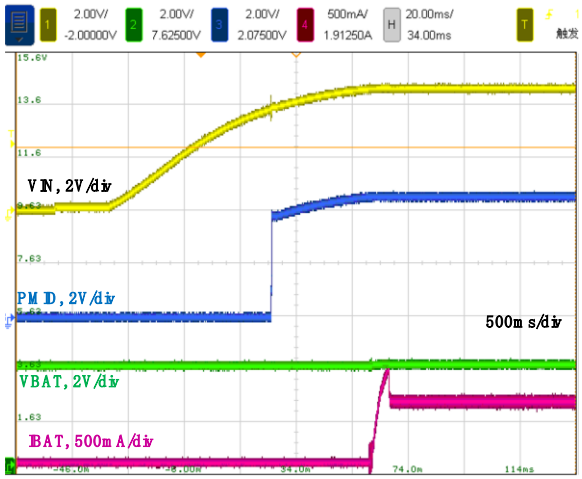


Figure 20. VIN plugged in with VIN DPM, EN_BST=1,EN_CHG=1,ICC=850mA, BOOST no load

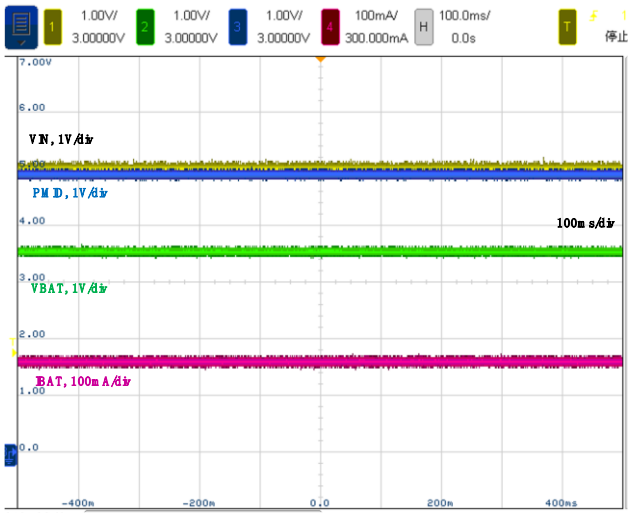


Figure 21. Charge with low ICC, ICC=150mA

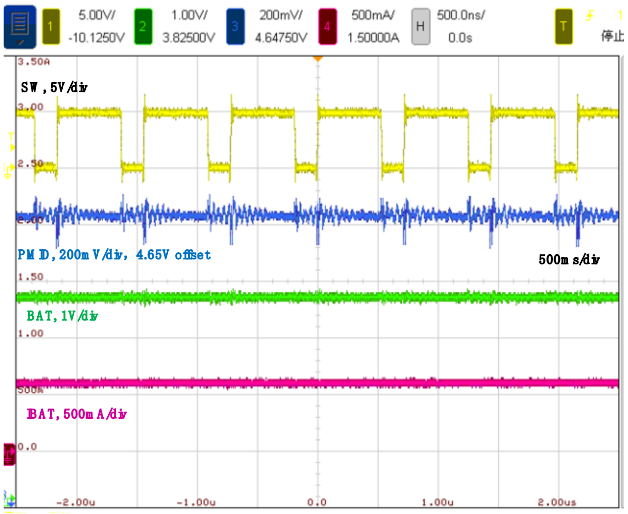


Figure 22. Charge with middle ICC, ICC=650mA

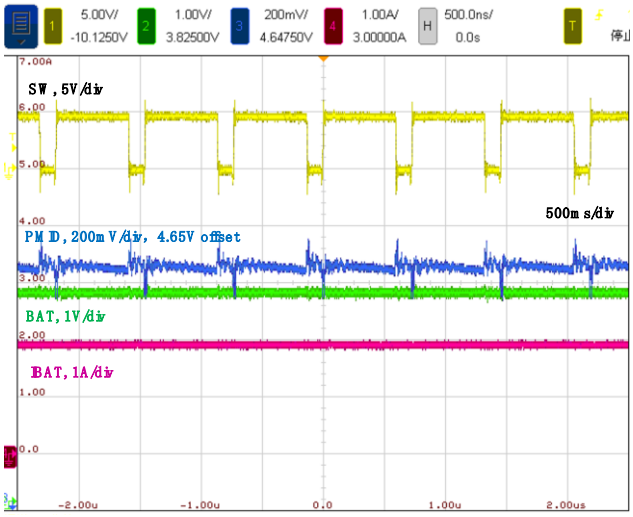


Figure 23. Charge with middle ICC, ICC=1700mA

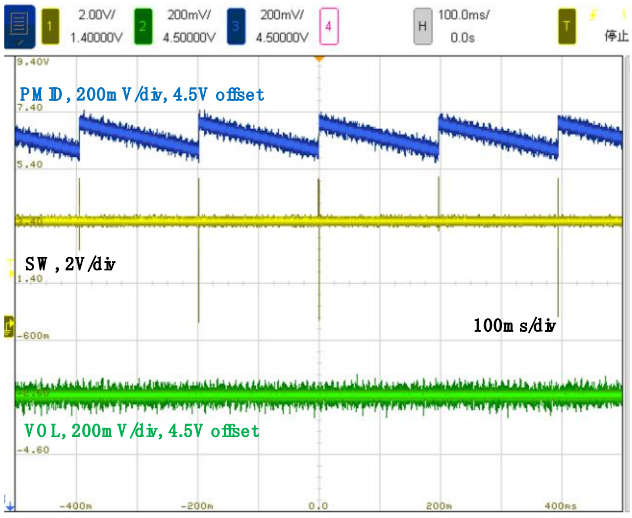


Figure 24. BOOST operation, no load, VOL=4.1V, EN_VOL=0

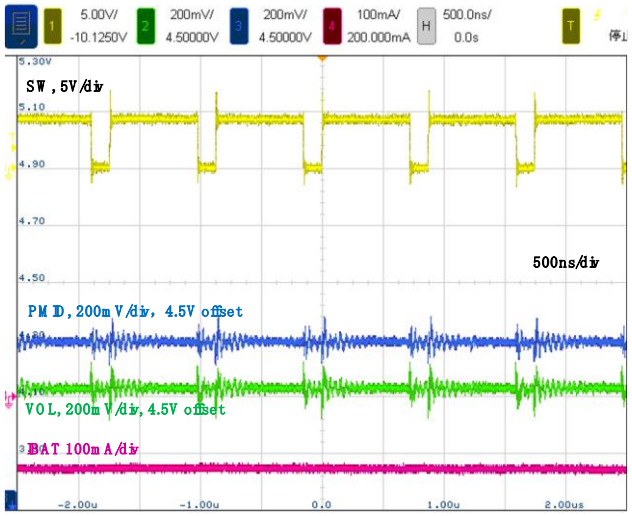


Figure 25. Earphone charging with EICC=100mA , VOL=4.1V, EN_VOL=1

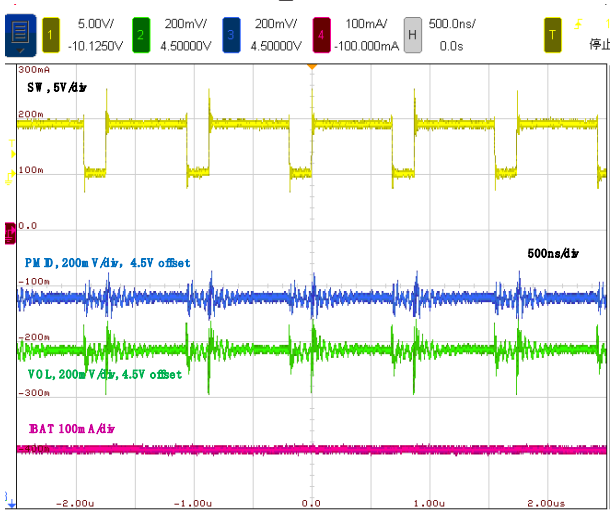


Figure 26. Earphone charging with EICC=300mA , VOL=4.1V, EN_VOL=1

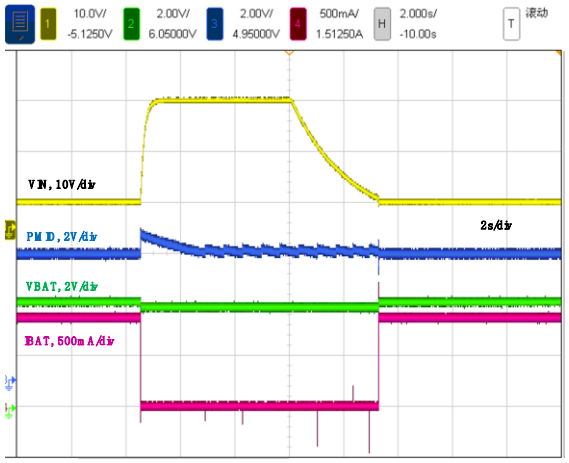


Figure 27. VIN OVP and recover, VIN=5V→25V→5V
EN_BST=1, EN_CHG=1, ICC=850mA

PCB Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.
Please follow the rules when designing the PCB layout.

1. the high frequency filtering capacitor C_1 C_3 C_4 should be placed as close to the pin and GND as possible. **Especially the C_4 (10uF recommend) high frequency capacitor should be placed between PMID and GND pins directly (not by vias). A Snubber circuit is strongly recommended to be placed between SW and GND plane .**
2. both the VIN, PMID and GND power paths should be wide and short to improve the system efficiency.
3. no capacitors should be placed at the VOL and VOR pins to guarantee the UART communication speed.(For 1Mbps UART communication, the total capacitance at VOL to GND should be less than 470pF)
4. the thermal pad should connect to the ground plane to help dissipating the power from the silicon.

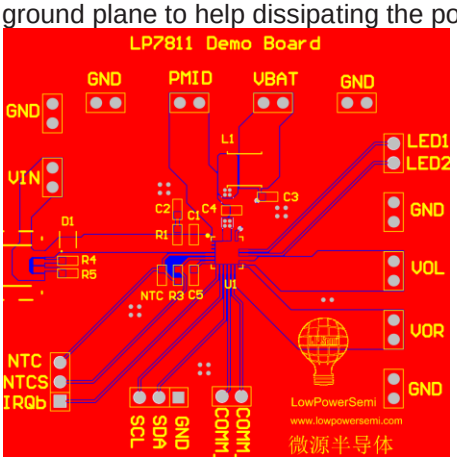
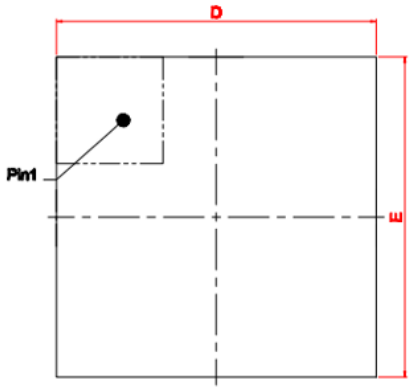


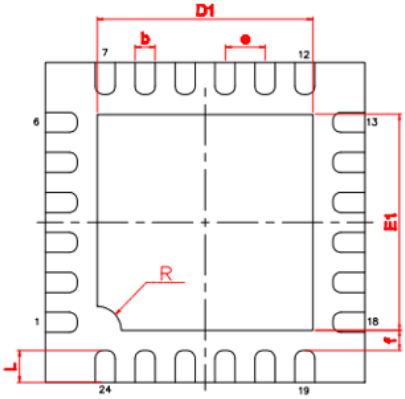
Figure 28.PCB example

Packaging Information

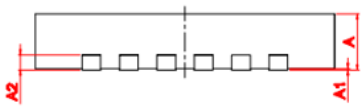
QFN-24



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
* A1	0.00	0.02	0.05
* A2		0.20 REF	
* b	0.20	0.25	0.30
* D	3.90	4.00	4.10
* E	3.90	4.00	4.10
* D1	2.60	2.70	2.80
* E1	2.60	2.70	2.80
* e	0.45	0.50	0.55
R		0.30 REF	
* f	0.20	0.25	0.30
* L	0.30	0.40	0.50

Revision History

Revision	Date	Change Description
Rev 0.1p0	5/5/2022	Product Brief
Rev 1p0	10/5/2022	Initial Release
Rev 1p1	4/5/2023	1. Add MSL information 2. Typo error fix 3. iEOC/iPMID interrupts rising edge only 4. Add PCB information 5. Update Figure 7/8/9/14