LP4081B

19V Linear Charger with Power Path Management

Features

- Input over-voltage protected up to 19V
- Charge management
  - Programmable charge current up to 1A
  - Programmable floating voltage with 0.3% accuracy
  - Programmable trickle charge and termination current with minimum 1mA termination current
- Automatic re-charge and thermal foldback
- I2C bus to SoC with an interrupt pin
- Power path management
- Charge safety timer and watchdog
- NTC management
- Rich protections: UVLO, OVP, SCP
- Minimum 0.6-μA ultra-low iq in normal operation
- 0.4-μA ultra-low iq in ship mode
- 2mm X 2mm QFN-12 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Smart Watch
- Fitness Application
- TWS
- Remote Control
- Solar Charger

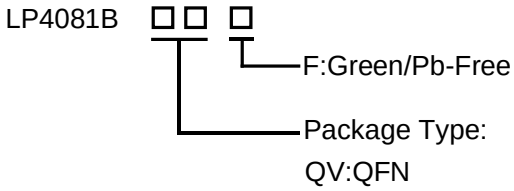
General Description

The LP4081B is a fully integrated linear charger solution with power path management targeting single-cell Li-ion battery powered wearable applications. A low on-resistance BUS-FET is integrated to manage the input power from a BUS pin. A bidirectional BAT-FET is integrated to manage charging and discharging of the battery. An NTC circuit is offered to manage the temperature range that charging is allowed. A SYS pin delivers power to the system that contains an SoC typically. The LP4081B offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the BUS input and the battery to meet the system loading needs. An I2C interface enables programming various parameters of charging, discharging, and multiple protection functions. An interrupt output (IRQb) sends a signal to the SoC when an interrupt event happens so the SoC can take actions accordingly.

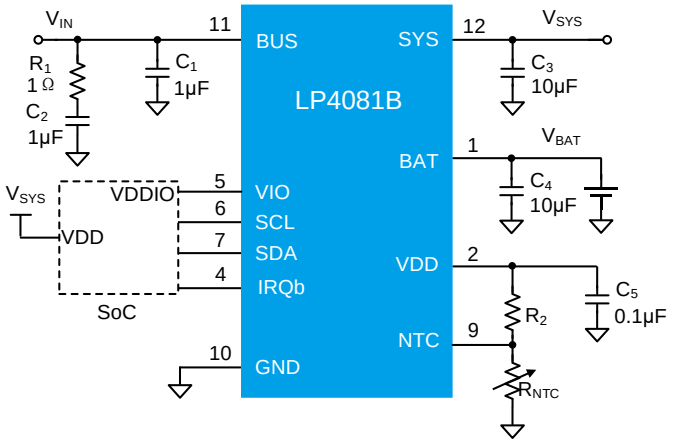
Multiple features are offerd for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), system reset, watchdog timer, etc. When powered by a battery, LP4081B can operate with only 0.6-μA current and this current can be further reduced to 0.4-μA when entering ship mode.

The whole system is in a 12-pin 2 X 2 QFN package.

Order Information



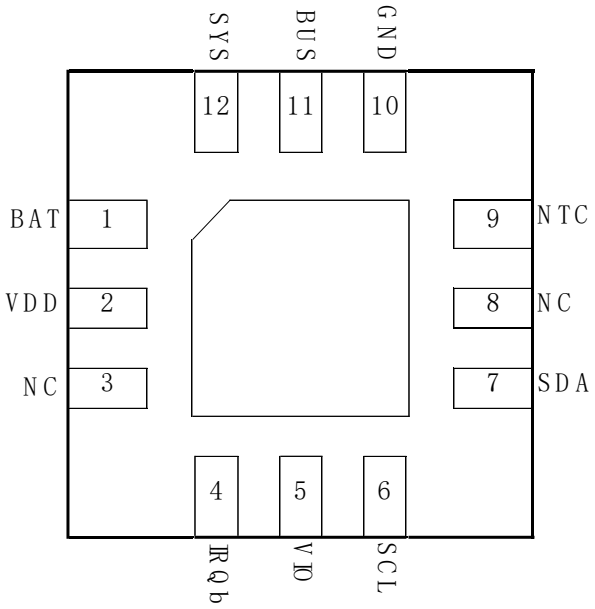
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	MSL
LP4081BQVF	LPS LP4081B YWX	12-pin 2 X 2 QFN	4K/REEL	LEVEL 3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. **MSL: Moisture Sensitivity Level according to JEDEC Standard.**				

Pin Diagram



LP4081B Pinout

Pin Description

Pin #	Name	Description
1	BAT	Battery pin of the linear charger. A 10uF decoupling capacitor is recommended.
2	VDD	NTC bias voltage output. A 0.01~0.1uF decoupling capacitor is recommended. Don't use this pin for other functions.
3	NC	No connection. Leave this pin floating.
4	IRQb	Interrupt output. This pin requires external pull-up.
5	VIO	I2C power supply input. Don't leave this pin open.
6	SCL	Clock line of the I2C bus. This pin requires is pulled to VIO internally.
7	SDA	Data line of the I2C bus. This pin requires is pulled to VIO internally.
8	NC	No connection. Leave this pin floating.
9	NTC	NTC pin. Connect the NTC resistor divider between this pin, VDD and GND pin.
10	GND	Power Ground.
11	BUS	Input power supply. A 1-10uF decoupling capacitor is recommended.
12	SYS	Power output for the system. A 10uF decoupling capacitor is recommended.
		Thermal PAD. Connect to power ground.

Absolute Maximum Ratings (Note 1)

BUS to GND ---------- -0.3V to 19V
All other pins to GND ---------- -0.3V to 6.5V
Maximum Junction Temperature (TJ) ---------- 150°C
Operating Ambient Temperature Range (TA)---------- -40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec)----------260℃

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ----------2kV
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ----------65℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{BUS}	Input voltage	3		5.6	V
I_{BUS}	Input current			1.5	A
T_A	Ambient temperature range	-40		85	°C
C_{BUS}	Input decoupling capacitor	0.1	1		μF
C_{sys}	System capacitor	1	10		μF
C_{bat}	Battery capacitor	1	10		μF

Electrical Characteristics

(The specifications are at V_{UVLO_BUS} < V_{BUS} < V_{OVP_BUS}, T_A = -40°C to +85°C and T_A = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{UVLO_BUS}	BUS UVLO	V_{BUS} falling		3.0		V
	Hysteresis			100		mV
V_{OVP_BUS}	BUS OVP threshold	V_{BUS} rising	5.6	5.7	5.8	V
	Hysteresis			100		mV
I_{q_BUS}	BUS input quiescent current	V_{BUS} =5.0V , V_{BAT} =4.3V , EN_CHG=1		100	130	μA
R_{DSON_BUS}	BUS-FET on- resistance	V_{BUS} =5.0V		0.3	0.4	Ω
I_{IN_LIM}	Input current limit	I_{IN_LIM} = 0	0.5	0.7		A
	Hiccup wait time[Note 2]			60		ms
BATTERY SECTION						
V_{BAT_POR}	BAT Power-on-reset	V_{BAT} rising	1.6		2.4	V
	Hysteresis			100		mV
I_{BAT}	Quiescent current from BAT	Discharge mode, V_{BUS} =0V, V_{BAT} =3.8V, SYS pin float, DIS[1:0]=10, EN_WTD=1		16		μA
		Charge mode, V_{BUS} =5V, V_{BAT} =4.5V, EN_Term=1		2	3	μA
		Miminum quiescent current in normal operation, V_{BUS} =0V, V_{BAT} =3.8V, DIS[1:0]=00, EN_WTD=0 , EN_NTC=0		0.6	1	μA
		Ship mode , V_{BUS} =0V, V_{BAT} =3.8V, SHIP=1		0.4		μA
CHARGE MANAGEMENT						
V_{TRI}	Trickle charge voltage threshold	V_{BAT} rising, V_{TRI}=3.0V	2.95	3.0	3.05	V
	Hysteresis			100		mV
I_{TRI}	Trickle charge current	ITERM[2:0]=001, I_{TRI} =3.3mA	3	3.3	3.6	mA
I_{CC}	CC current	25°C	53	55	58	mA
V_{CV}	CV voltage	From -10°C to 85°C, I_{CC}=204mA, V_{CV}=4.2V	-0.5		0.5	%
		From -10°C to 85°C, I_{CC}=55mA, V_{CV}=4.2V	-1		0.5	%
V_{RECHG}	Re-charge threshold	V_{BAT} falling, Reference to CV voltage		-150		mV
t_{drechg}	Recharge deglitch time[Note 2]			200		ms
I_{TERM}	Charge termination current	ITERM[2:0]=001, I_{TERM} =3.3mA	3	3.3	3.6	mA
t_{dterm}	termination deglitch time[Note 2]			30		ms
V_{SYS_DPM}	SYS dynamic power management threshold	V_{SYS} falling, DPM[2:0]= 011, 3.6V	3.55	3.6	3.65	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{therm}	Thermal foldback threshold		100	120	140	°C
t_{Tri_safe}	Trickle charge safety timer expiration time [Note 2]	From trickle charge start to exit trickle charge		0.75		Hr
t_{Fast_safe}	Fast charge safety timer expiration time[Note 2]	From exit trickle to charge terminate		3.75		Hr
POWER PATH MANAGEMENT						
R_{DSON_BAT}	BAT-FET on resistance	V_{BAT} =3.8V		0.15		Ω
I_{DIS_LIM}	Discharge SCP limit	IDIS_LIM[1:0]=00,		0.4		A
t_{denter_ship}	Enter ship mode delay time[Note 2]			1		s
t_{dexit_ship}	Exit ship mode delay time[Note 2]			2		s
V_{BAT_UV}	Battery UVLO	V_{BAT} falling, BAT_UV[1:0]=00		2.85		V
	Hysteresis	V_{BAT} rising		0.2		V
t_{d_BATUV}	BAT_UV deglitch			40		ms
NTC MANAGEMENT						
T_0	0°C threshold	V_{NTC} rising, in % of VDD	72.4	73.3	74.2	%
	Hysteresis	in % of VDD		1.5		%
T_{10}	10°C threshold	V_{NTC} rising, in % of VDD	63.3	64.3	65.3	%
	Hysteresis	in % of VDD		1.5		%
T_{45}	45°C threshold	V_{NTC} falling, in % of VDD	32.1	32.9	33.7	%
	Hysteresis	in % of VDD		2		%
SCL, SDA and IRQb						
V_H	Logic High		1.2			V
V_L	Logic Low				0.4	V
I_{sink}	SDA, SCL, IRQb sink current capability	V_{BAT} =3.8V， V_{PIN}=0.4V	0.5			mA
t_{Irqb}	IRQb low pulse width[Note 2]			256		μs

Note 2: Not production tested. Guaranteed by design.

Typical Characteristics

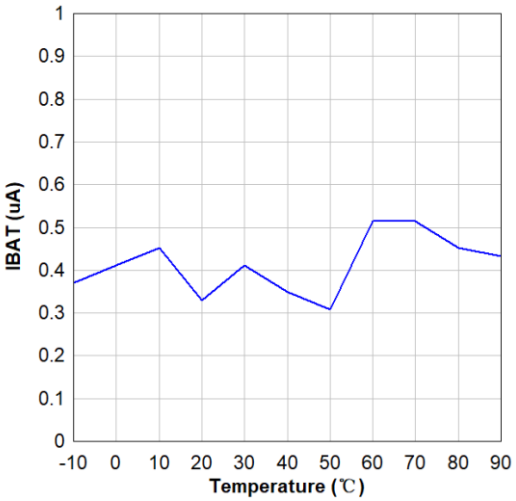


Figure 1. I_{BAT} vs. Ambient Temperature. V_{BAT}=3.6V, ship mode

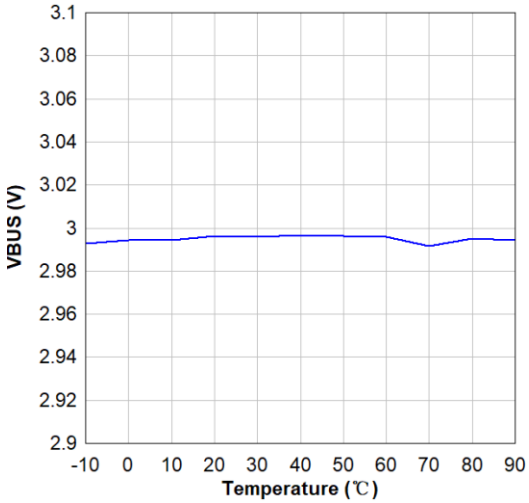


Figure 2. V_{UVLO_BUS} vs. Ambient Temperature. VBUS falling edge

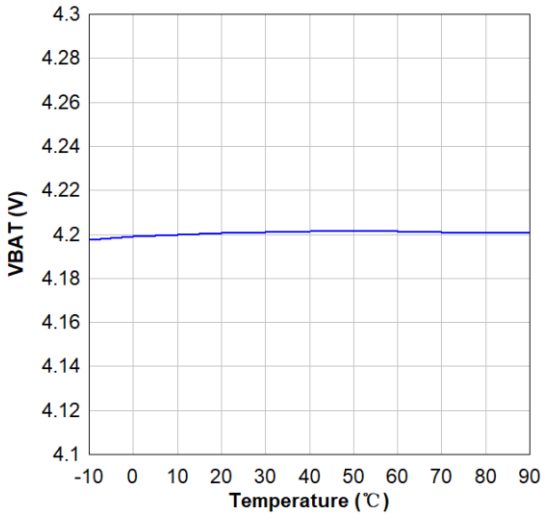


Figure 3. V_{CV} vs. Ambient Temperature. CV=4.2V

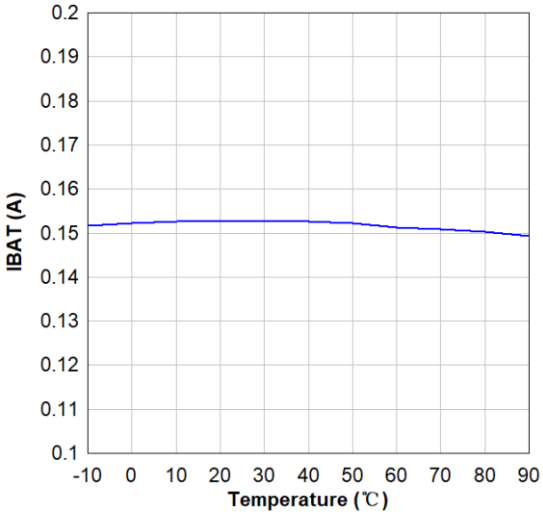


Figure 4. I_{CC} vs. Ambient Temperature. I_{CC}=154.5mA

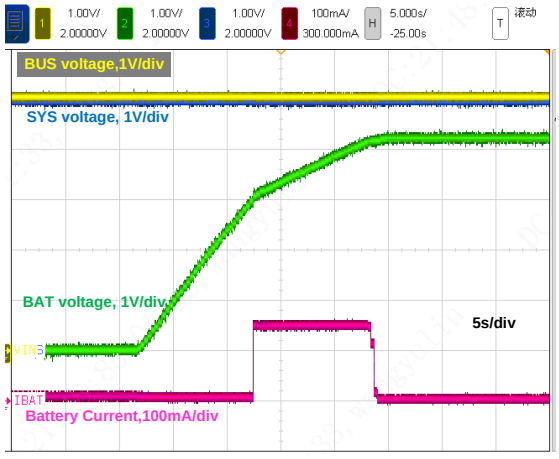


Figure 5. Battery Charging Curve, I_{TRI}= 3.3mA,I_{CC}=154.5mA, I_{TERM}=3.3mA

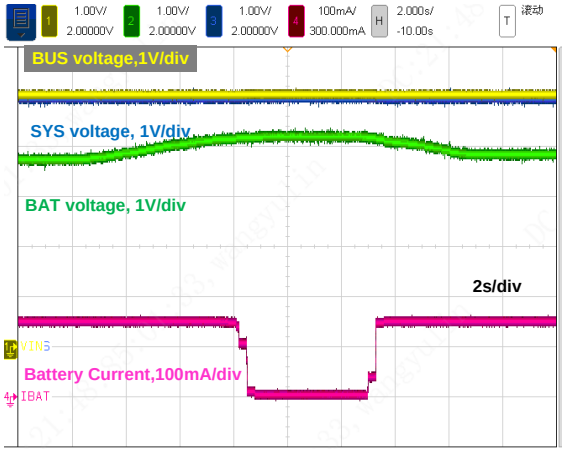


Figure 6. Auto-Recharge

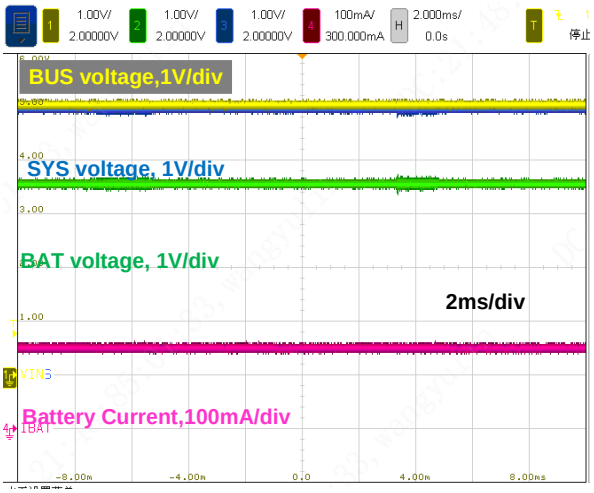


Figure 7. CC Steady State

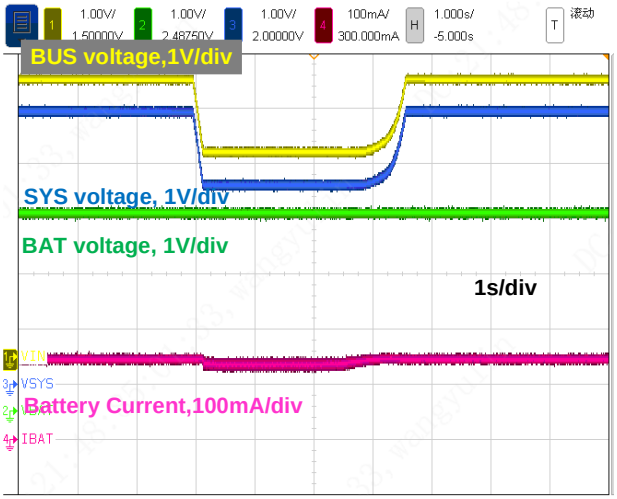


Figure 8. VIN Based DPM

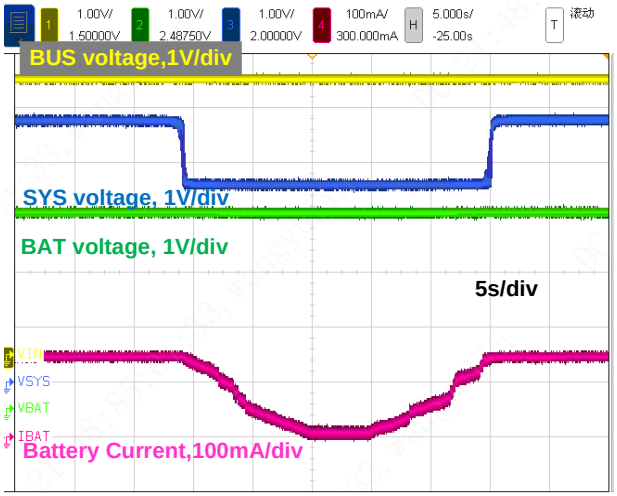


Figure 9. Input Current Limit Based DPM

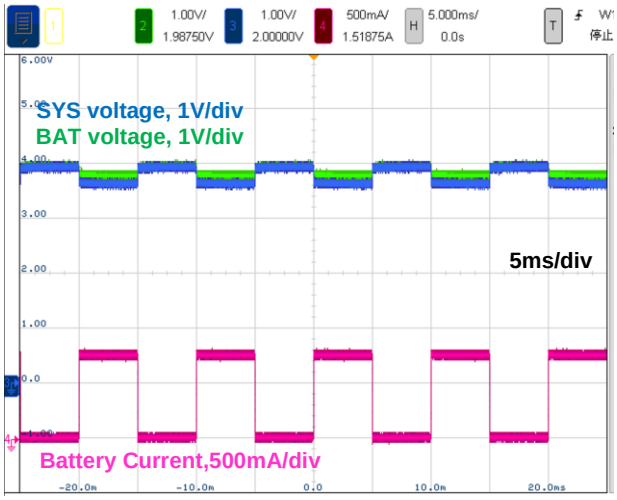


Figure 10. SYS Load Transient, 0A-0.8A-0A, BAT=4.0V, bypass mode

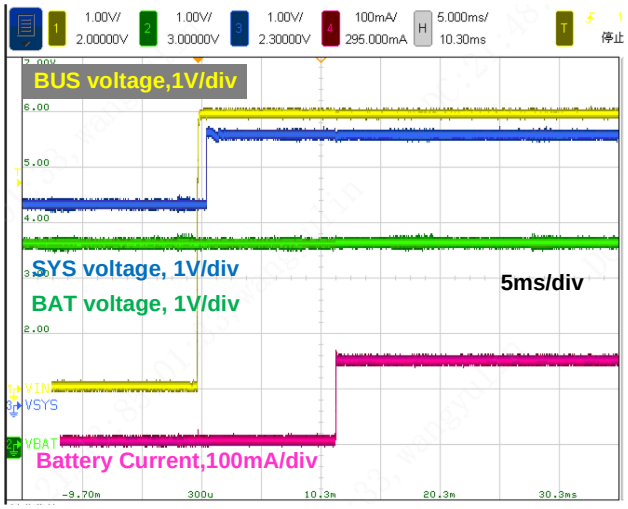


Figure 11. VIN Power Up

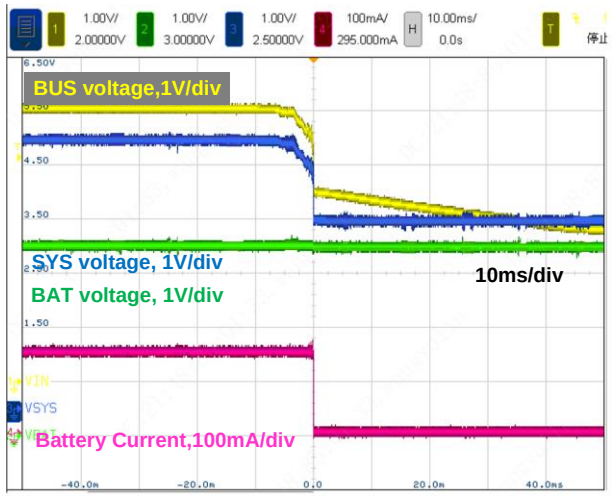


Figure 12. VIN Power Down

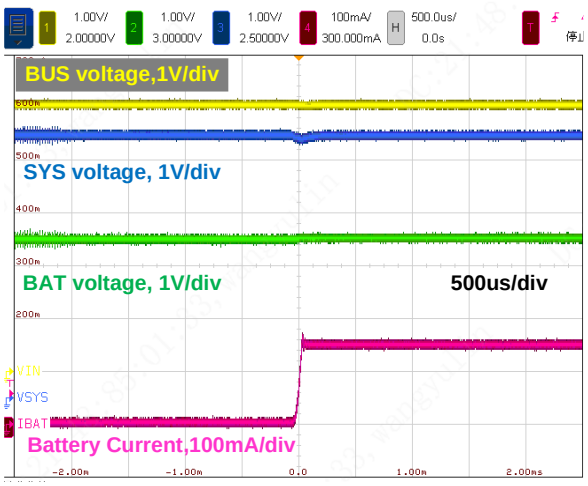


Figure 13. Charge Enable

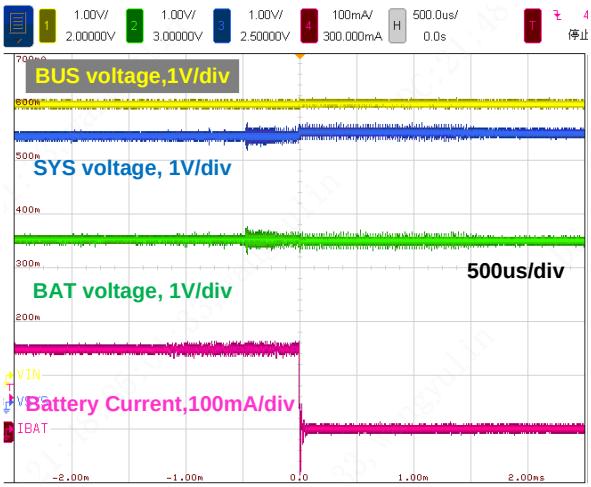


Figure 14. Charge Disable

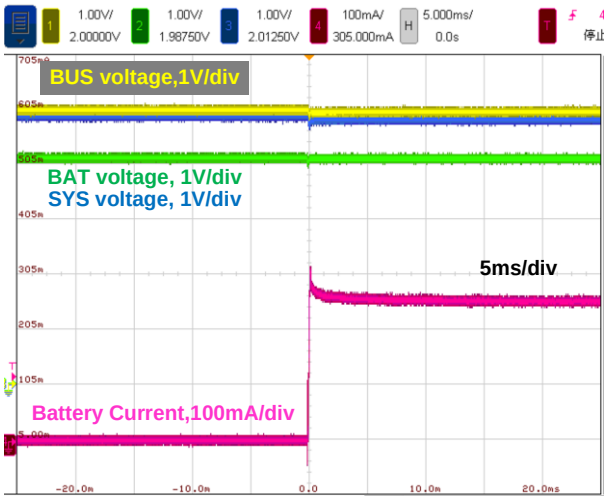


Figure 15. Battery Insert

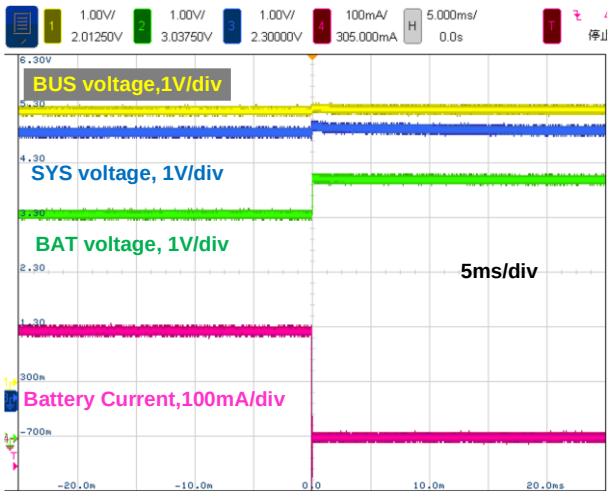


Figure 16. Battery Removal

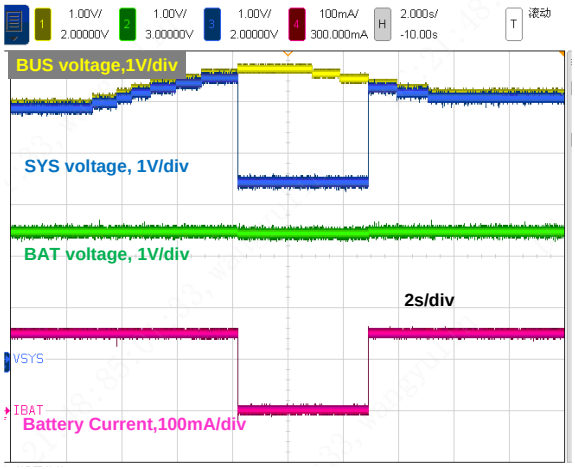
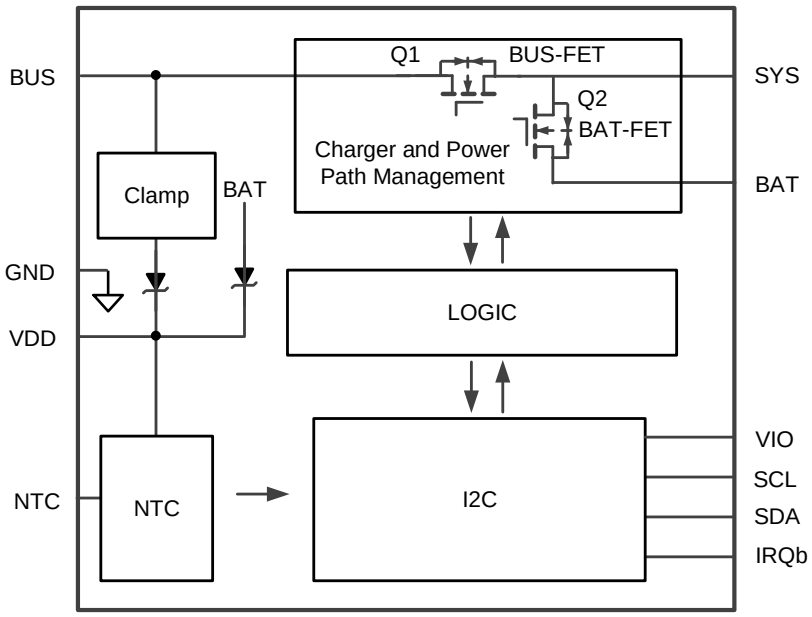


Figure 17. VIN OVP and recover

Functional Block Diagram



Detailed Description

Overview

The LP4081B is a fully integrated linear charger solution with power path management targeting single-cell Li-ion battery powered wearable applications. A low on-resistance BUS-FET is integrated to manage the input power from the BUS pin. A bidirectional BAT-FET is integrated to manage charging and discharging of the battery that is connected to the BAT pin. An NTC circuit is offered to manage the temperature range that charging is allowed. The SYS pin delivers power to the system that contains an SoC typically. The LP4081B offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the BUS input and the battery to meet the system loading needs. An I2C interface enables programming various parameters of charging, discharging, and multiple protection functions. The interrupt output (IRQb) sends a signal to the SoC when an interrupt event happens so the SoC can take actions accordingly.

Multiple features are offerd for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), system reset, watchdog timer, etc. When powered by a battery, LP4081B can operate with only 0.6-μA current and this current can be further reduced to 0.4-μA when entering ship mode.

Power-on Reset (POR)

The LP4081B performs a POR when either the BUS input voltage or the BAT pin voltage is higher than the $V_{BAT\ POR}$ rising threshold. All registers will be set to default values when performing the POR. Refer to the Register Map section for more register information. The SoC or MCU can access all registers after POR.

Input Section

The input section contains the BUS-FET and its control circuitry to realize UVLO, OVP, RCP, ideal diode, current limit, and short-circuit protection functions.

UVLO and OVP

The input section control circuit monitors the BUS-pin voltage to determine when to turn on or off the BUS-FET. The LP4081B detects an over-voltage event when the input voltage is higher than OVP threshold and turns off the BUS-FET immediately. The LP4081B detects an under voltage (UV) event when the input voltage is lower than V_{UVLO_BUS} falling threshold. The LP4081B turns off the BUS-FET as well after a typical 100-us deglitch time.

BUS Power Good (PGD)

When it is between the UVLO and the OVP threshold, the input voltage is in a power-good (PGD) range. The BUS-FET is turned on with a typical 1-ms startup time and the PGD bit of the Status Register 0 is set after a 30-ms deglitch time. If the BUS voltage falls off the PGD range, the BUS-FET is turned off.

Ideal Diode Function with Current Limit

The BUS-FET is controlled as an ideal diode with a 50mV forward regulation and a current limit. When the BUS-FET is turned on, the forward voltage across the BUS-FET will be dependent on the forward current passing through. The BUS-FET is firstly turned on fully so the voltage is the product of the forward current and the R_{DSON_BUS} (which is 300mΩ typically). As the forward current reduces, the forward voltage reduces accordingly. As the forward voltage drops to 50mV, a forward-voltage regulation control loop will start to increase the R_{DSON} so the forward voltage remains regulated at 50mV. On the other hand, if it reaches a current limit (programmable with the IIN_LIM bit of Control Register 0, default 700mA), the forward current will be regulated at the current limit. If the BUS-FET is reversely biased, i.e. the SYS-pin voltage is higher than the BUS-pin voltage, the reverse current is fully blocked.

System SCP

The LP4081B has a system short-circuit protection (SCP) function. When the SYS-pin voltage is pulled lower than 2.5V for 1ms when PGD bit is 1, the LP4081B enters hiccup mode. Both the BUS-FET and the BAT-FET are turned off for 64ms and then the device will try to restart powering up the SYS pin for 1ms. If the SYS-pin voltage rises above the 2.5V threshold within 1ms, the hiccup will stop; otherwise, the BUS-FET and the BAT-FET will be turned off for 64ms again and repeat the restart-up.

Charge Management

The LP4081B will charge the battery through the BAT-FET when the SYS-pin voltage is higher than the battery voltage.

The charger is a typical linear charger with three charging modes, i.e., trickle, CC, and CV modes. A typical charging cycle is shown in Figure 18. The charging currents and CV are programmable by I2C. The EN_CHG bit of Control Register 2 can enable the charger. The following describes the details of the charging operation.

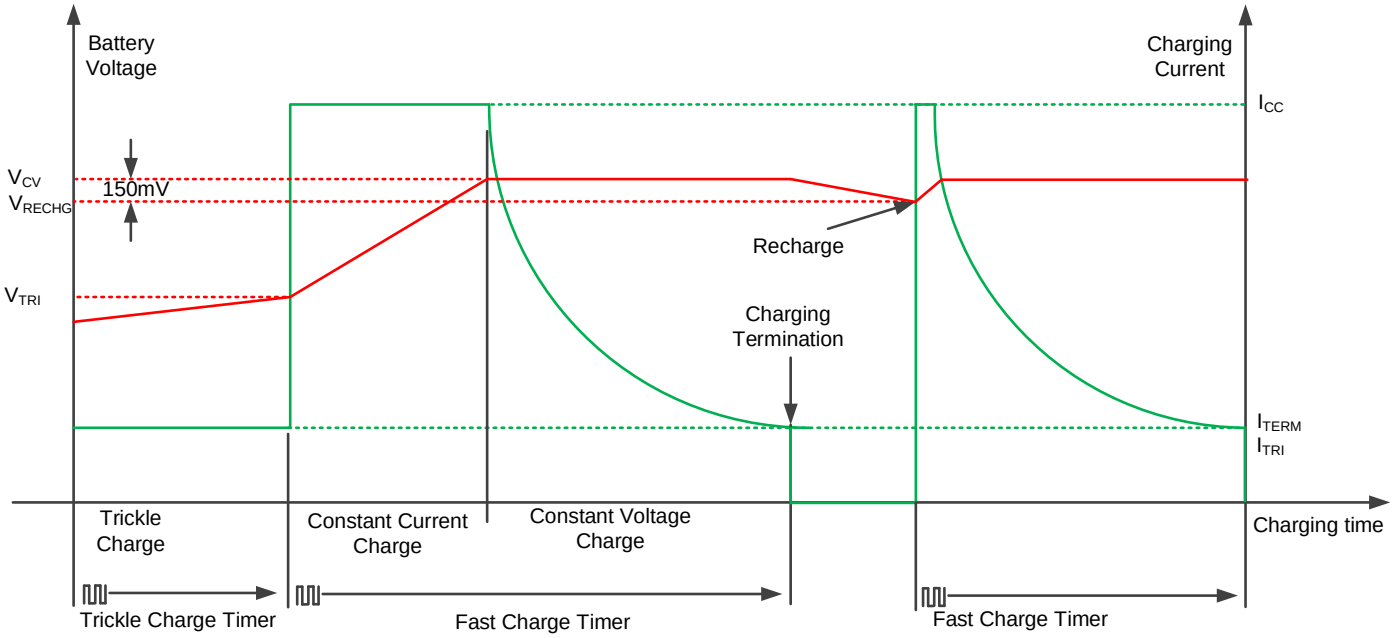


Figure 18. 5V normal charging profile with power source current unlimited

Start of a Charge Cycle

The linear charger can be in a charge cycle when all the conditions below are valid,

- PGD = 1
- EN_CHG = 1
- The NTC-pin voltage is in the range of T_0 and T_{45} given in the Electrical Characteristics table.

A new charge cycle will start when the last of the above conditions changes from invalid to valid. For example, when the NTC-pin voltage and the PGD are valid when the EN-CHG bit is set. Both the trickle and the fast charge safety timers are reset when a new charge cycle starts. See the following section for more information on safety timers.

Trickle Mode

The charger enters the trickle mode at the beginning of a charge cycle if the battery voltage is below the trickle-charge voltage threshold (V_{TRI}) that is programmable via the VTRI bit of the Control Register 2. The default value is 3.0V. The trickle-charge current is programmable with the ITERM[2:0] bits of the Control Register 1. A safety timer will start at the beginning of the trickle mode. If V_{TRI} is not reached before the trickle charge safety timer (which is 0.75Hr typically) expires, the charging cycle will be terminated and the TRI_TE bit of the Status Register is set.

CC Mode

The LP4081B starts the CC mode when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The charging current is determined by the ICC[5:0] bits of the Control Register 2 and the ICC_EXT bit of Control Register 0. The CC current is programmable from 15~1200mA when ICC_EXT is set to 1 and the range is reduced to 6~506mA when the ICC_EXT bit is set to 0. The default charging current is 28mA and ICC_EXT bit is 0.

A fast charge safety timer starts when the CC mode begins and the TERM_TE bit of the Status Register is cleared. The timer expires in 3.75 hours. The TERM_TE bit is set when the fast charge safety timer expires.

BAT-FET Ideal Diode Mode when in CC Mode

When the power supply to the BUS pin has a current capability lower than the sum of the CC charge current and system load current and the battery voltage is higher than the Dynamic Power Management (DPM) threshold, the linear charger will enter an ideal diode mode. The typical charging is shown is shown Figure 19.

When the BAT-FET is turned on, the forward voltage across the BAT-FET will be dependent on the forward current

passing through. The BAT-FET is firstly turned on fully so the voltage is the product of the charging current and the R_{DSON_BAT}. As the charging current reduces when LP4081B enters CV or the input current from the BUS pin is limited, the forward voltage reduces accordingly. As the forward voltage drops to 25mV, a forward-voltage regulation control loop will start to increase the R_{DSON_BAT} so the forward voltage remains regulated at 25mV.

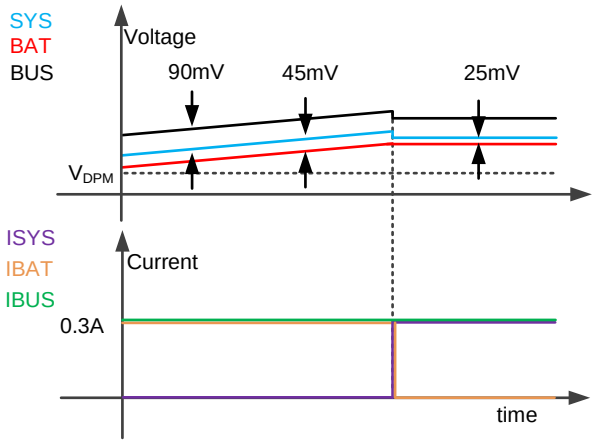


Figure 19. BAT-FET ideal diode mode charging with 300mA input current limit

CV Mode

The LP4081B starts the CV mode when the battery voltage reaches the CV threshold. The charging current decreases gradually until the charging termination is triggered in this mode. The CV voltage is programmable via the BAT_CV[4:0] bits of the Control Register 1. The default value is 4.2V.

The fast charge safety timer will continue until the 3.75-hour expiration time.

Charge Cycle Termination

When the BAT voltage is higher than the recharge voltage and the charging current drops to the termination current threshold, the charging termination is triggered. The charging is terminated immediately if EN_TERM bit is set to 1 and the CHG[2:1] bits of the Status Register0 are set to 11; otherwise, only the CHG[2:1] bits are set to 11 but the charging continues until the fast charge safety timer expires.

Recharge

A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage while the BUS voltage is still present. The charging cycle starts again, together with the safety timer.

Charge Current Thermal Foldback

When the die temperature reaches 120 ºC, the charging current decreases to prevent further temperature rise.

NTC Management

An NTC resistor with 1% accuracy and a beta of 3435 is recommended for LP4081B. The NTC resistor is enabled by the EN_NTC bit with its default value of 1. The VDD and the internal NTC detection circuitry are disabled when EN_NTC is set to 0 or the BUS pin falls below the V_{UVLO_BUS} to reduce the quiescent current.

Three temperature detecting thresholds are provided, i.e., T_0, T_{10}, and T_{45} . An NTC interrupt pulse will be sent when the temperature is crossing these thresholds.

The NTC [2:0] bits are used to indicate the temperature range in the Status Register 1. The SoC can change the charging parameters or disable the charging operation by using the control registers.

The charging function and charger safety timers are forced to be turned off when the temperature is outside the range of T_0 to T_{45}. The charging function recovers when temperature returns inside the range of T_0 to T_{45}. The trickle/fast charge safety timers are reset and starts counting again. The NTC[2:0] will be set to 011 when EN_NTC=0.

EN_CHG Bit

EN-CHG bit can enable the charger. When EN_CHG is set to 0, the charging cycle is terminated immediately. When EN_CHG is set to 1 from 0, a new charging cycle starts again.

Power Path Management

The LP4081B integrates the power path management function. The SYS pin can be powered from the input voltage, the battery, or both at the same time under different scenarios.

Dynamic Power Management

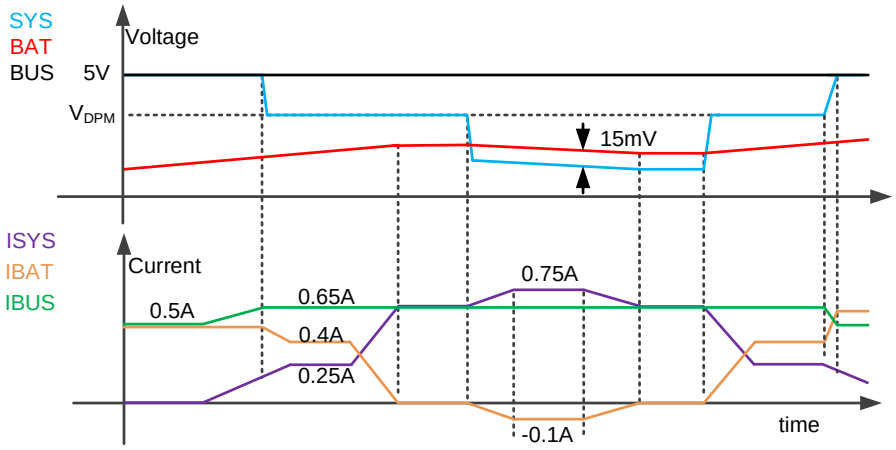


Figure 20. Dynamic power management with with power source current unlimited

The voltage at the SYS pin and currents through the BUS-FET and BAT-FET are monitored continuously when the LP4081B is powered. The minimum SYS-pin voltage is set by the DPM[2:0] bits of the Control Register 3. When the SYS-pin voltage drops (due to system loading) to the voltage set by the DPM[2:0] bits , the charging current is reduced to prevent the SYS-pin voltage from dropping further. The battery will start providing current if the current through the BUS-FET (limited at 650mA) alone is not surfficient to prevent the SYS-pin voltage further dropping, in which case the BAT-FET is controlled as an ideal diode with 15mV forward voltage regulation. The Figure 20 shows the operation of the dynamic power management. When the input power is removed, the system is powered from the battery only.

BAT-FET Operation Modes

When the input power is removed, the BAT-FET has four operation modes configurable with the DIS[1:0] bits of the Control Register 0, i.e. bypass, system reset, auto, and ship mode, as shown in Table 1. The default value is 10.

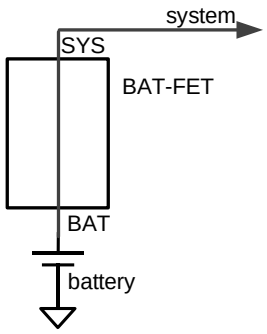
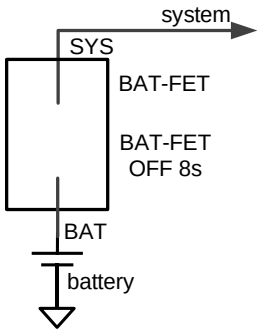
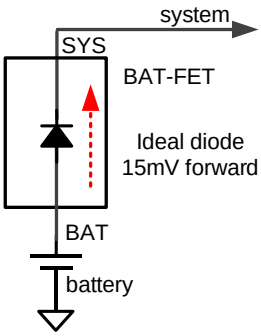
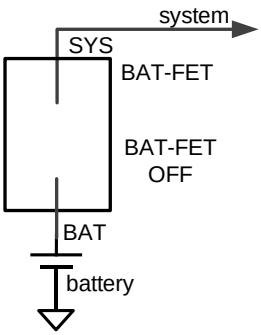
The BAT-FET is fully turned on in the bypass mode when DIS[1:0] is set to 00. The BAT-FET current limit function is disabled to save power. The power loss is minimized in this mode and the quiescent current is only 0.6μA.

The BAT-FET starts the system reset mode when the DIS[1:0] is set to 01. The BAT-FET is turned OFF for 8 seconds to power down the system. After 8 seconds, the BAT-FET is turned on again and the whole chip will perform a POR with all registers set to their default values. The quiescent current is typically 16μA during the 8 seconds.

When the DIS[1:0] is set to 10, the BAT_FET is in the auto mode. The BAT-FET is controlled as an ideal diode with a 15mV forward regulation and a current limit. When the BAT-FET is turned on, the forward voltage across the BAT-FET will be dependent on the forward current passing through. The BAT-FET is firstly turned on fully so the voltage is the product of the forward current and the R_{DSON_BAT}. As the forward current reduces, the forward voltage reduces accordingly. As the forward voltage drops to 15mV, a forward-voltage regulation control loop will start to increase the R_{DSON_BAT} so the forward voltage remains regulated at 15mV. On the other hand, if it reaches a current limit (programmable with the IDIS_LIM[1:0] bits of the Control Register 0, default 440mA), the forward current will be regulated at the current limit. If the SYS-pin voltage falls below 1V, the LP4081B starts a hiccup operation, same as the SCP operation in the charge mode. The quiescent current is typically 16μA in this mode.

When the DIS[1:0] is set to 11, the chip enters the ship mode with the BAT-FET fully turned off after a typical 1s deglitch time. The quiescent current is minimized to only 0.4μA in this mode. Since the whole system is powered down, the system has no additional quescient current. The LP4081B exits the ship mode when the voltage at the BUS pin ramps higher than the V_{UVLO_BUS} threshold. All the registers are reset to the default values when entering the ship mode.

Table 1. BAT-FET operation modes with no BUS voltage

MODE / ITEM	DIS[1:0]=00	DIS[1:0]=01	DIS[1:0]=10	DIS[1:0]=11
Equivalent BAT-FET circuit				
Mode	Bypass mode	System reset mode	Auto mode	Ship mode
SYS pin voltage	$V_{SYS} = V_{BAT} - I_{sys}*R_{DSON,BAT}$	1. BAT-FET OFF 8s 2. SYS is pulled down by leakage 3. All registers are reset	$V_{SYS} = V_{BAT}$ - maximum(15mV, $I_{sys}*R_{DSON\_BAT}$)	BAT-FET OFF All registers are reset
Min iq	0.6μA battery current	16μA battery current	16μA battery current	0.4μA battery current

System Reset

The LP4081B offers two methods to reset the SoC system. The SoC can initiate the system reset mode by setting the DIS[1:0] to 01, as described earlier. In addition, the LP4081B offers a watchdog timer to automatically reset the SoC system. The watchdog timer has a 40s typical expiration time. The SoC should write 1 to the WTD bit before the time expires. When the watchdog timer expires, all the power FETs are forced to be turned off for 8 seconds to power down the SoC system. All registers are reset to the default values after the watchdog expires. The watchdog can be disabled to save quiescent current by setting the EN_WTD bit to 0.

Minimum Operating Current

When powered by the battery alone, the LP4081B can minimize its operating current by setting the BAT-FET in the bypass mode (DIS[1:0] = 00) and disabling the watchdog timer (EN-WTD = 0) at the same time. The LP4081B only consumes 0.6-μA quiescent current with such configuration. The I2C registers are still active.

Ship Mode

The LP4081B supporting ship mode by setting the SHIP bit (DIS[1:0] =11) by I2C when LP4081B is powered by the battery and the input is removed. The DIS[1:0] bits should be set to 10 first before entering ship mode. The LP4081B turns off all the active circuits after a typical 1s deglitch time. The LP4081B only consumes 0.4-μA in ship mode. Both a valid input power supply is plugged in and the IRQb pin is pulled from high level to low level for 2s can force the LP4081B exiting the ship mode.

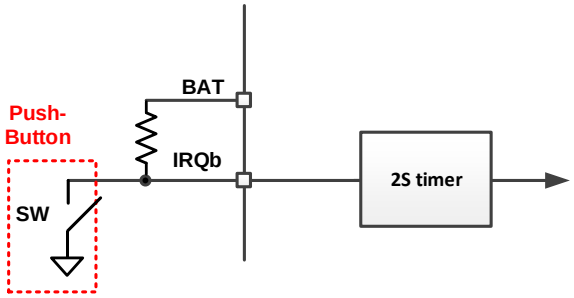


Figure 21. Exit ship mode by IRQb pin

All the registers are set to the default values after LP4081B enters ship mode.

Thermal Shutdown

When the internal junction temperature of LP4081B exceeds the thermal shutdown threshold of 150 °C, the LP4081B disables all the power paths. The LP4081B recovers to the default setting after the junction temperature falls to the 130 °C .

I2C BUS and Interrupt

The LP4081B has an I2C BUS and the interrupt IRQb pin. The LP4081B operates as a slave device with an address of 6BH (7bit, 1101011). A 1 or 0 should be placed at the end of the address that represents read or write operation. The VIO is power supply of the internal I2C circuits. The IRQb pin is an open-drain output. The SoC can pull up this pin to the digital IO power rail internally. The SDA and SCL are both pulled up to the VIO with 100kΩ resistor.

Interrupt

The interrupt pin IRQb pulls to low for 256us when an interrupt event happens in the chip. Those events include,

- Input power attaching or removal
- SYS pin shorting to GND
- Trickle charge timer expiration
- Fast charge timer expiration
- Watchdog timer expiration
- Charge status changing
- Battery being fully charged
- Battery voltage falling below the UVLO threshold
- Temperature sensed by the NTC circuit crossing thresholds

The interrupt events can be masked by the control bits in the Interrupt Mask Register.

I2C DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

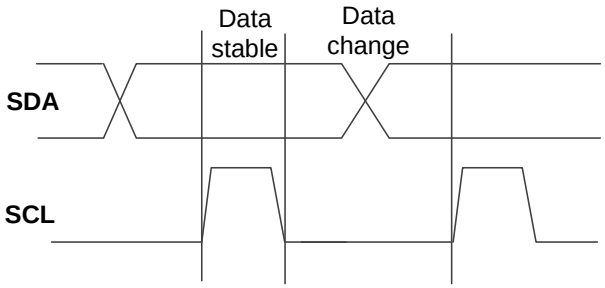


Figure 22. I2C Data validity

I2C Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the

SDA line while the SCL is high means a Start condition. A rising edge on the SDA line while the SCL is at high means a Stop condition.

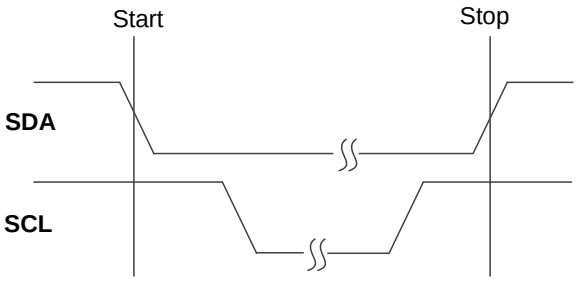


Figure 23. I2C Start and Stop Conditions

I2C Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

Single Byte Read and Write

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 24. Single-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK
							8 bit	1bit	1bit
							Data from Address	NACK	STOP

Figure 25. Single-byte Read

Multi-Read and Multi-Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit							
START	Slave address	0	ACK	Register address	ACK	START							
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit		
				Data to Address	ACK	Data to Address	ACK	.....	Data to Address	ACK	stop		

Figure 26. Multi-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit					
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1					
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit		
				Data from Address	ACK	Data from Address	ACK	.....	Data from Address	NACK	stop		

Figure 27. Multi-byte Read

Register Map

Table 2. Device Registers

Register Name	Address	Read/ Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status rgister 0	00H	RO	TRI_TE	TERM_TE	WTD_TE	BAT_UV	SCP	CHG	CHG	PGD
Status register 1	01H	RO	reserve	reserve	reserve	reserve	reserve	NTC	NTC	NTC
Mask register 00	02H	RW	reserve	mBAT_UV	mEOC	mSCP	mCHG	mPGD	mTimer	mNTC
Control register 0	03H	RW	BAT_UV	BAT_UV	ICC_EXT	IDSI_LIM	IDIS_LIM	IIN_LIM	DIS	DIS
Control register 1	04H	RW	ITERM	ITERM	ITERM	BAT_CV	BAT_CV	BAT_CV	BAT_CV	BAT_CV
Control register 2	05H	RW	EN_CHG	VTRI	ICC	ICC	ICC	ICC	ICC	ICC
Control register 3	06H	RW	WTD	EN_WTD	EN_NTC	EN_Tri_Timer	EN_Term	DPM	DPM	DPM

Note: **RO**: read only; **RC**: read and clear; **RW**: read and write

Status Register 0 /Address: 00H (default: 0x00)

Table 3. Status Register 0

Bit	Symbol	Description	Read/Write	Default
7	Trickle_TE	=1 Trickle charge timer expiration	RO	0
6	Term_TE	=1 Fast charge timer expiration	RO	0
5	WTD_TE	=1 Watchdog timer expiration	RO	0
4	BAT_UV	=1 Battery discharge UVLO	RO	0
3	SCP	=1 SYS is short circuit to ground	RO	0
2	CHG	00: Not in charging mode, 01: Trickle	RO	0
1	CHG	10: CC/CV 11: EOC	RO	0
0	PGD	=1 $V_{UVLO\_BUS} < V_{BUS} < V_{OVP\_BUS}$	RO	0

Status Register 1 /Address: 01H (default: 0x03)

Table 4. Status Register 1

Bit	Symbol	Description	Read/Write	Default
2	NTC	000: not valid, 001: <0 °C	RO	0
1	NTC	010:0-10 °C, 011: 10~45 °C	RO	1
0	NTC	100: >45 °C, 101/ 110/111: not valid	RO	1

Interrupt Mask Register/Address: 02H (default: 0x00)

Table 5. Interrupt Mask Register 0

Bit	Symbol	Description	Read/Write	Default
7		reserve	RW	0
6	mBAT_UV	Mask interrupt	RW	0
5	mEOC		RW	0
4	mSCP		RW	0
3	mCHG		RW	0
2	mPGD		RW	0
1	mTimer		RW	0
0	mNTC		RW	0

Control Register 0/Address: 03H (default: 0x00)

Table 6. Control Register0

Bit	Symbol	Description	Read/Write	Default
7	BAT_UV[1]	Battery UVLO rising edge threshold:		0
6	BAT_UV[0]	00:3.0V, 01:3.2V, 10:3.4V, 11:3.6V Battery UVLO falling edge threshold: 00:2.85V, 01:3.0V, 10:3.2V, 11:3.4V		0
5	ICC_EXT	=0, Normal charge related current setting, default setting =1, All the charge related current is extend to 2.5X of default, including: trickle/CC/termination current	RW	0
4	IDIS_LIM	discharge current limit	RW	0
3	IDIS_LIM	00: 400mA 01: 300mA 10:200mA 11: 100mA	RW	0
2	IIN_LIM	input current limit =1: 1.6A, =0: 700mA	RW	0
1	DIS[1]	BAT_FET operation mode control:	RW	0
0	DIS[0]	00: BAT_FET bypass mode, 01: system reset mode, 10: auto mode, 11: ship mode	RW	0

Control Register 1/Address: 04H (default: 0x24)

Table 7. Register 3

Bit	Symbol	Description	R/W	Default
7	ITERM[2]	Trickle and Termination current set: 000:1.1mA, 001:3.3 mA, 010:5.5 mA, 011:7.7 mA, 100:9.9 mA,101:12.1 mA, 110:14.3, 111:16.5mA All this current will be X 2.5 times if ICC_EXT = 1	RW	3.3mA 001
6	ITERM[1]		RW	
5	ITERM[0]		RW	
4	BAT_CV[4]	Battery CV voltage set: 00000:4.0V, 00001:4.05V, 00010:4.1V, 00011:4.15V, 00100:4.2V, 00101:4.22V, 00110:4.24V,00111:4.26V, 01000:4.28V, 01001:4.3V, 01010:4.32V,01011:4.34V, 01100:4.35V,01101:4.36V, 01110:4.38V 01111:4.4V,10000:4.42V,10001:4.44V, 10010:4.46V,10011:4.48V, 10100:4.5V, 10101~1111: not valid	RW	4.2V 00100
3	BAT_CV[3]		RW	
2	BAT_CV[2]		RW	
1	BAT_CV[1]		RW	
0	BAT_CV[0]		RW	

Control Register 2/Address: 05H (default: 0X44)

Table 8. Register 4

Bit	Symbol	Description	R/W	Default
7	EN_CHG	=1: Charge enable. =0: Charge disable	RW	0
6	VTRI	Trickle charge threshold set: =1: 3.0V =0:2.8V	RW	1
5	ICC[5]	Constant current set: 000000:6mA, 000001:11.5mA, 000010:17mA, 000011:22.5mA, 000100:28mA, 000101:33.5mA, 000110:39mA, 000111:44.5mA, 001000:50mA, 001001:55.5mA, 001010:61mA,001011:66.5mA 001100:72mA, 001101:77.5mA, 001110:83mA, 001111:88.5mA, 010000:94mA, 010001:99.5mA, 010010:105mA,010011:110.5mA,010100:116mA, 010101:121.5mA, 010110:127mA,010111:132.5mA 011000:138mA, 011001:143.5mA,011010:149mA, 011011:154.5mA,011100:160mA, 011101:165.5mA, 011110:171mA,11111:176.5mA,100000:182mA, 100001:187.5mA, 100010:193mA,100011:198.5mA 100100:209mA, 100101:220mA,100110:231mA, 100111:242mA, 101000:253mA, 101001:264mA, 101010:275mA,101011:286mA, 101100:297mA, 101101:308mA, 101110:319mA,101111:330mA 110000:341mA, 110001:352mA,110010:363mA, 110011:374mA, 110100:385mA, 110101:396mA, 110110:407mA,110111:418mA, 111000:429mA, 111001:440mA, 111010:451mA,111011:462mA 111100:473mA, 111101:484mA, 111110:495mA, 111111:506mA All the current is extended 2.5 times if ICC_EXT bit is set to 1	RW	28mA 000100
4	ICC[4]		RW	
3	ICC[3]		RW	
2	ICC[2]		RW	
1	ICC[1]		RW	
0	ICC[0]		RW	

Control Register 3/Address: 06H (default: 0x43)

Table 9. Register 5

Bit	Symbol	Description	R/W	Default
7	WTD	Write WTD 1 will reset watchdog timer SoC need write this bit to 1 before watchdog timer count out.	RW	0
6	EN_WTD	=1 Watchdog function is enabled =0 Watchdog function is disbaled	RW	1
5	EN_NTC	=1 NTC circuits are enabled =0 NTC circuits are disabled	RW	0
4	EN_Tri_Timer	=1 Enable 0.75Hr trickle charge safety timer =0 Disable 0.75Hr trickle charge safety timer	RW	0
3	EN_Term	=1 Stop charging after EOC, =0 Continue charging after EOC until 3.75Hr safety timer time expiration	RW	0
2	DPM[2]	VSYS DPM threshold: 000:3.0V, 001:3.2V, 010:3.4V, 011:3.6V, 100:3.8V, 101:4.0V, 110:4.2V, 111:4.4V	RW	011
1	DPM[1]		RW	
0	DPM[0]		RW	

Application Information

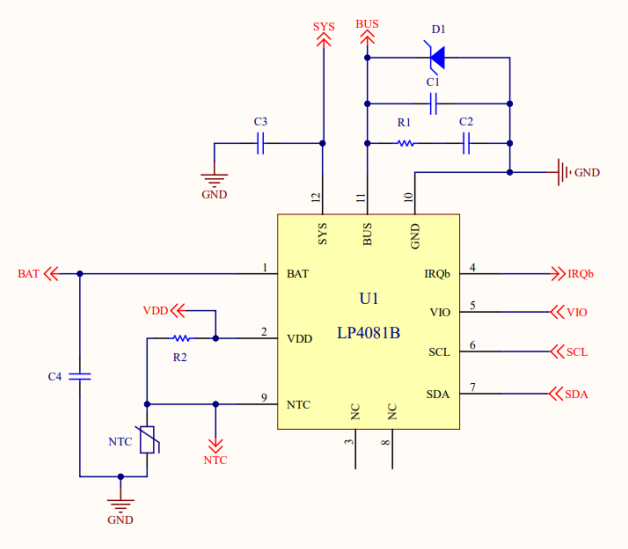


Figure 28. Typical Application Schematic

A typical application consists of the multi-function-in-one power management IC of LP4081B and the host SoC. When powering up in default mode, the battery CV voltage of LP4081B is 4.2V, the constant charging current is 28mA, the termination current and trickle charge current is 3.3mA. The system dynamic power management voltage is 3.6V. The SoC can change all the default values via the I2C interface.

Capacitor selection

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the BUS, BAT, and SYS pin to the GND pin. The BUS capacitor C_1 and C_2 should be 25V rating with minimum 1uF capacitance. The BAT capacitor C_4 should be at least 6.3V rating with minimum 10uF capacitance. The SYS capacitor C_3 should be at least 6.3V rating with minimum 10uF capacitance.

NTC Circuit Design

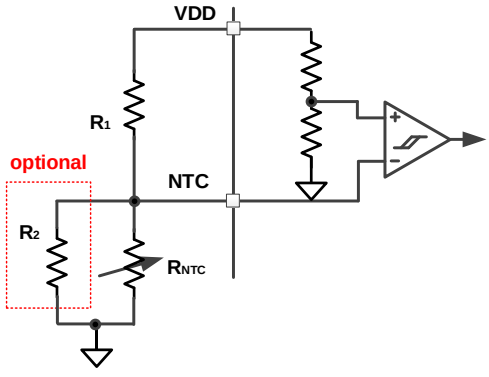


Figure 29. NTC circuit

All the trigger-point thresholds of the internal NTC comparators are designed with a 10-kΩ NTC resistor with 1% accuracy and a beta of 3435. R_1 should be set to 10-kΩ to cooperate with the 10-kΩ NTC resistor. All the thresholds can be found in the electrical characteristics table. An additional resistor in parallel with the NTC resistor can help adjusting the temperature thresholds. The following eqμAtions help calculating the temperature thresholds.

$$R2 = \frac{0.404 * R_{NTC_{HOT}} * R_{NTC_{COLD}}}{0.0878 * R_{NTC_{COLD}} - 0.4918 * R_{NTC_{HOT}}}$$

$$R1 = 0.364 * (\frac{R2 * R_{NTC_{COLD}}}{R2 + R_{NTC_{COLD}}})$$

For example, when the charge function is needed in the 0°C~60°C temperature range, the R_{NTC_HOT} is 3.02-kΩ while the R_{NTC_COLD} is 27.5-kΩ. The calculated R2 is 35.8-kΩ and the R1 is 5.66-kΩ.

PCB Layout Guidelines

Please follow the rules when designing the PCB layout.

1. The high frequency filtering capacitor should be placed as close to the pin and GND as possible, including the C_1, C_3, and C_4. 0603 size capacitors are recommended. The loop circumference formed by the capacitors and the pins should under 200 mils to minimize the parasitic inductance.(For example, the enclosed circumference via the C_1, the BUS pin and the GND pin should be controlled to less than 200 mils)
2. The BUS, VBAT and GND power paths should be wide and short to improve the system efficiency. As a recommendation, the trace path should be at least 40 mils to deliver 1.5A current with 1oz copper thickness.
3. C_2 and R_1 is recommended to be soldered in order to absorb the input spike caused by the long trace from the adapter to the BUS capacitors when USB plugs in and out. The C_2 and R_1 can greatly reduce the inpt spike.
4. The thermal pad should connected to the ground plane to help dissipating the power from the silicon.

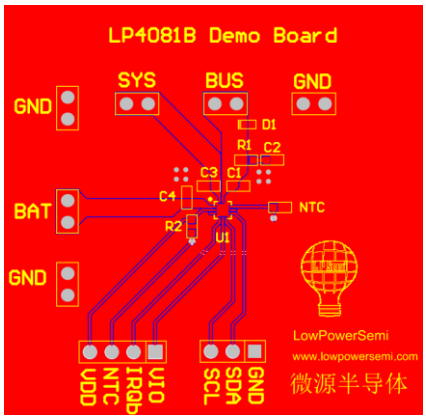


Figure 30. PCB Example (TOP LAYER)

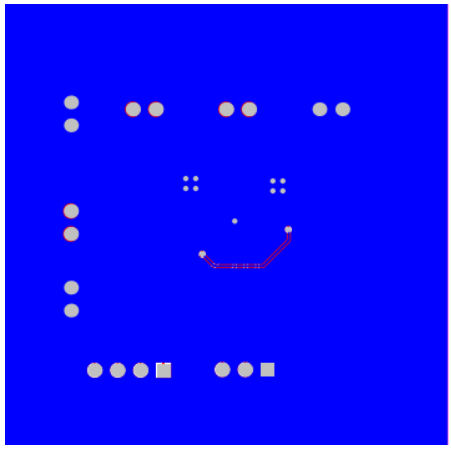
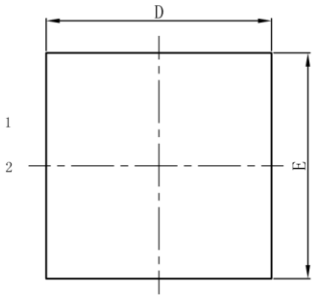


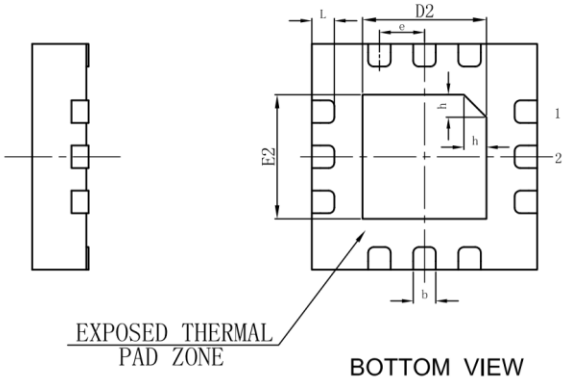
Figure 31. PCB Example (BOTTOM LAYER)

Packaging Information

2x2 QFN package

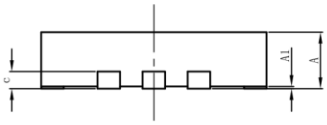


TOP VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.00	1.10	1.20
e	0.40BSC		
E	1.90	2.00	2.10
E2	1.00	1.10	1.20
L	0.15	0.20	0.25
h	0.15	0.20	0.25
L/F载体尺寸 (mil)	53X53		



SIDE VIEW

Revision History

Revision	Date	Change Description
Rev 1p0	10/5/2022	Release Version 1.0
Rev 1p1	3/5/2023	1. Update pinmap information 2. Add MSL information 3. Update Figure 5/11/12 1. Update battery UVLO description
Rev 1p2	5/5/2023	1. pin 5 information change from NC to VIO 2. Update block diagram 3. Update Figure 19 4. Add Table 1 in BAT-FET Control Section 5. New format