Features

- **Case Charging Management**
  - Support 4.1V to 6.2V input voltage with 30V absolute maximum input voltage rating
  - Programmable fast charge current up to 930mA
  - Programmable floating voltage with 0.5% accuracy
  - Automatic recharge function
  - 7.5% trickle charge current
  - 7.5% termination current
- **Smart Earphone Charging Management**
  - Independent earphone insert detection and charging path
  - Smart earphone ultra-low dropout charging to maximize battery run time
  - Programmable earphone fast charge current up to 250mA each channel
  - Programmable End of Charge (EEOC) current
  - Bi-directional communication to earphones
- 1-channel always-on Linear Regulator
- Temperature Management
  - JIETA standard NTC management during charging and discharging
  - Charging current thermal foldback
  - Thermal shutdown protection
- I2C interface with interrupt indication
- 4-uA ultra-low quiescent current
- 3mm X 3mm QFN-16 package
- RoHS Compliant and 100% Lead (Pb) free

Applications

- TWS charging case
- Wireless microphone
- Smart Glasses

General Description

The LP7810A is an advanced TWS charging case management IC targeting to improve the total battery run time of the TWS earphones. The IC features a linear charger protects up to 30V input voltage and digitally programmable up to 930mA charge current via an I2C bus. The smart discharge voltage management feature tries to maximize the battery run time. The VOL and the VOR outputs track the battery voltages of the earphones when operating together with the companion linear charger (LP4080) in the earphone, minimizing the power loss. An NTC interface is offered to manage the charge and discharge operation based on the battery temperature sensed by the NTC resistor. Additional silicon temperature management ensure the safe operation. Earphone insertion and removal detections simplify the design of the earphone detection. The LP7810A supports an independent bidirectional communication bus to the earphones. An I2C bus is offered for programmability and flexibility of the device. The typical quiescent current is 4-uA.

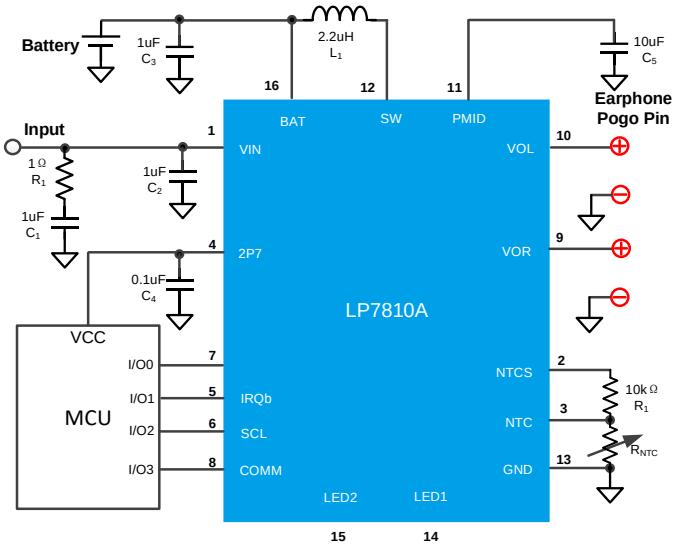
The whole system is in a small 16-pin 3x3 QFN package.

Order Information

LP7810A □□ □

- F: Green/Pb-Free
- Package Type
  - QV : QFN

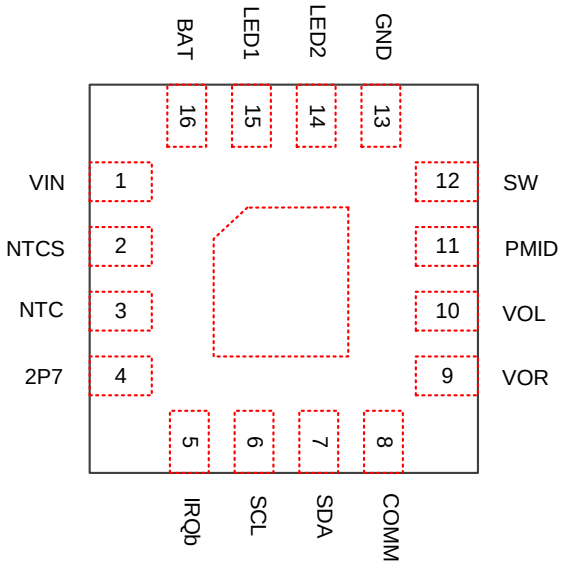
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	Note
LP7810AQVF	LPS 7810A YWX	QFN-16	5K/REEL	
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



LP7810A Pinout

Pin Description

Pin #	Name	Description
1	VIN	Input voltage that is connected to the VCC of the USB port. A 0.1uF or higher value input decoupling capacitor must be connected to this pin and the GND pin.
2	NTC	NTC input.
3	NTCS	Bias switch to the NTC input. The bias will be switched off during standby mode to reduce the quiescent current caused by the NTC resistor.
4	2P7	2.7V power supply to power an external MCU. This supply is also used to bias the NTC circuit and the communication signal to the earphones. A 0.47-μF ceramic capacitor should be placed between this pin and GND pin.
5	IRQb	Interrupt output to the external MCU. This pin is pulled up to 2P7 pin by a resistor internally.
6	SCL	Clock line of the I2C bus. This pin is pulled up to 2P7 pin by a resistor internally.
7	SDA	Data line of the I2C bus. This pin is pulled up to 2P7 pin by a resistor internally.
8	COMM	Communication input/output for the communication bus to earphones.
9	VOR	Output to the right earphone.
10	VOL	Output to the left earphone.
11	PMID	Output of the boost converter, which is also the power supply to the two current regulators to the left and the right earphones. A 10uF ceramic capacitor is required between this pin and the GND pin.
12	SW	Switching node of the boost converter.

13	GND	Ground
14	LED2	Open-drain LED output.
15	LED1	Open-drain LED output.
16	BAT	Battery pin of the linear charger.
Thermal PAD		Connect to ground panel for thermal dissipation.

Absolute Maximum Ratings (Note)

VIN to GND ---------- 0.3V to 30V
Others to GND ---------- 0.3V to 6.5V
Operating Ambient Temperature Range (TA) ---------- 40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 70℃/W

Recommended Operating Conditions

Notes:
(1) All the values are effective capacitance or inductance.
(2) X5R and 16V or higher voltage rating are recommended.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	4.1		6.0	V
I_{CC}	Fast Charge Current	0.03		0.93	A
T_J	Operating Junction Temperature Range (T_J)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃
L	Output Inductance(1)	0.7	2.2	6	μH
C_{IN}	Input Capacitance (1) (2)	0.6	1	4.7	μF
C_{PMID}	PMID Capacitance(1) (2)	4	10	30	μF
C_{BAT}	BAT Capacitance(1) (3)	4	10	20	μF

Electrical Characteristics

(The specifications are at V_{VIN} =5V , T_J = -40°C to +85°C and T_J = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{VIN}	VIN quiescent current	V_{BAT} = 4.5V , NTC=10kΩ, EN_BST=1		310		μA
I_{Q_BAT}	Battery quiescent current	V_{BAT} = 4.5V, VIN floating, EN_BST=0, PUP=00		4		μA
INPUT VOLTAGE						
V_{VIN}	VIN operation range		4.1		6.0	V
V_{VIN_UVLO}	VIN UVLO threshold	VIN falling	3.6	3.8	4.0	V
$V_{VIN\_UVLO\_HYS}$	VIN UVLO hysteresis	VIN rising	50	100	150	mV

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIN_OVP}	VIN OVP threshold	VIN rising	6.0	6.2	6.55	V
$V_{VIN\_OVP\_HYS}$	VIN OVP hysteresis	VIN falling	50	150	200	mV
V_{INDPM}	VIN DPM threshold	battery voltage falling		4.4		V
V_{POR}	POR threshold	battery voltage rising	2.0		2.6	V
V_{POR_HYS}	POR hysteresis	battery voltage falling		0.18		V
Charge Management						
V_{TRK}	Trickle charge voltage threshold	battery voltage rising	2.7	2.8	2.9	V
V_{TRK_HYS}	Trickle charge voltage hysteresis	battery voltage falling		100		mV
I_{TRK}	Trickle charge current	In percentage of I_{CC}	5	7.5	9.5	%
I_{CC}	CC current	From 0℃ to 125℃	378	420	462	mA
		At 25℃	400	420	440	mA
V_{CV}	CV voltage	From 0℃ to 50℃	-0.5		0.5	%
	Re-charge threshold	falling edge, Reference to CV voltage		-150		mV
I_{TERM}	Charge termination current	In percentage of I_{CC}	5	7.5	9.5	%
	Thermal foldback threshold		100	120	140	℃
Earphone charge						
$R_{on,HS}$	High-side FET on-resistance	PMID=5.0V		230		mΩ
$R_{on,LS}$	Low-side FET on-resistance	PMID=5.0V		180		mΩ
I_{peak}	Boost mode peak current limit	BAT=3.6V, boost mode	1.1	1.2		A
I_{byp}	Bypass mode current limit	0°C to 125°C, PMID loaded, bypass mode	550	900		mA
V_{PMID}	Boost output voltage accuracy	25℃	-1%		+1%	%
I_{PUP}	Insert detection current	1-μA pull up current, BAT=3.6V	0.9	1	1.1	uA
V_{INSERT}	Insert detection threshold	VIN floating, BAT=3.8V, BST_EN=0, reference to BAT voltage		-0.7		V
EICC	Earphone fast charge current	0℃ to 125℃, 250mA	225	250	275	mA
		0℃ to 125℃, 100mA	90	100	110	mA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		0℃ to 125℃, 40mA	36	40	44	mA
EEOC	Earphone end of charge current threshold	EICC=200mA, EEOC=2mA	1.6	3.2	4.8	mA
		EICC=200mA, EEOC=10mA	10.2	16	20.8	mA
		EICC=150mA, EEOC=2mA	1	2	3	mA
		EICC=150mA, EEOC=10mA	7	10	13	mA
NTC Management						
T_{-10}	NTC -10℃ threshold	V_{NTC} voltage rising	80.4	81.2	81.9	%
T_{-10_HYS}	NTC -10℃ hysteresis	V_{NTC} voltage falling		1.5		%
T_0	NTC 0℃ threshold	V_{NTC} voltage rising	72.4	73.3	74.2	%
T_{0_HYS}	NTC 0℃ hysteresis	V_{NTC} voltage falling		1.5		%
T_{15}	NTC 15℃ threshold	V_{NTC} voltage rising	58.5	59.5	60.5	%
T_{15_HYS}	NTC 15℃ hysteresis	V_{NTC} voltage falling		1.5		%
T_{45}	NTC 45℃ threshold	V_{NTC} voltage falling	32.1	32.9	33.7	%
T_{45_HYS}	NTC 45℃ hysteresis	V_{NTC} voltage rising		2		%
T_{60}	NTC 60℃ threshold	V_{NTC} voltage falling	22.5	23.2	23.8	%
T_{60_HYS}	NTC 60℃ hysteresis	V_{NTC} voltage rising		2		%
2.7V always-on linear regulator						
V_{2P7}	LDO output voltage accuracy	BAT=3.8V	2.56	2.7	2.84	V
I_{2P7}	LDO output current capability		15			mA
Digital						
R_{UP}	VOL/R pull up resistor	2.7V, 500ohm pull up resistor		500		Ω
I_{DOWN}	VOL/R pull down current capability	PMID=5V， VOL/VOR=0.4V	10			mA
I_{LED}	LED pull down current capability	PMID=5V， VLED=0.4V	10			mA
I_{irqb}	IRQb pull down current capability	PMID=5V， VIRQb=0.4V	0.5			mA

Typical Characteristics

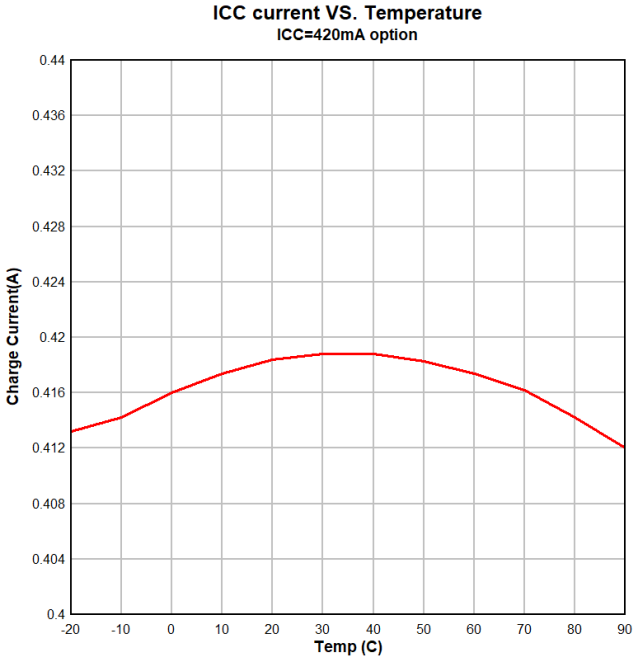


Figure 1. Fast charge current VS. Temperature.

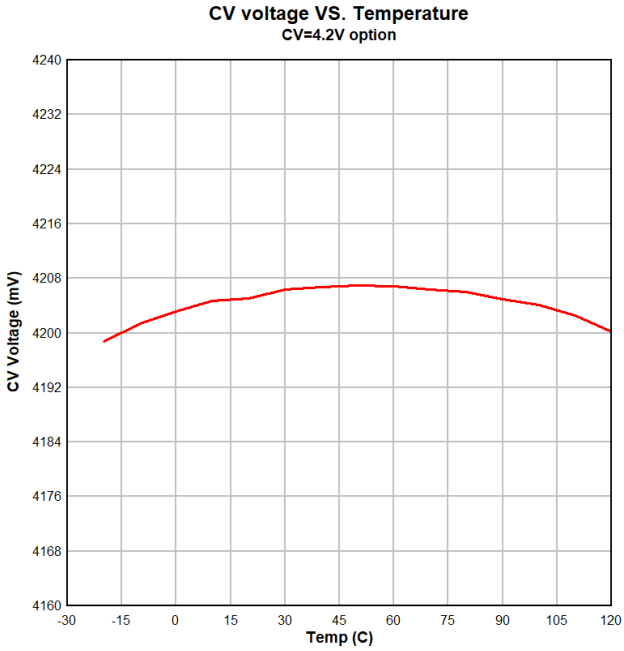


Figure 2. Floating voltage VS. Temperature.

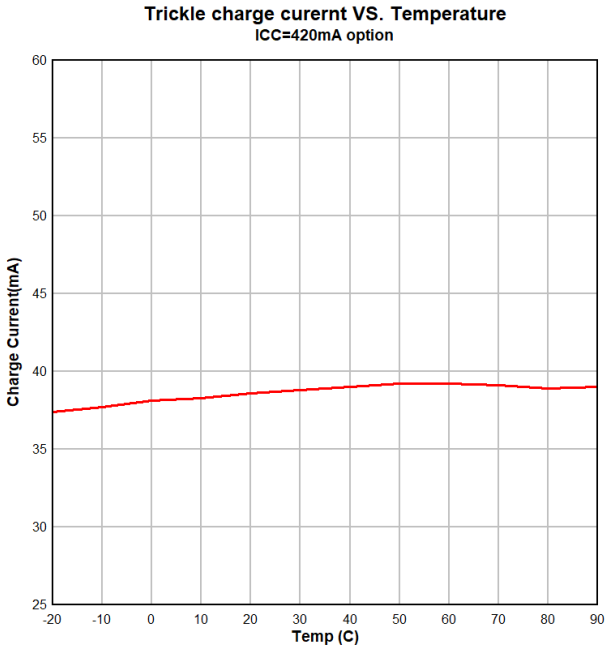


Figure 3. Trickle charge current VS. Temperature.

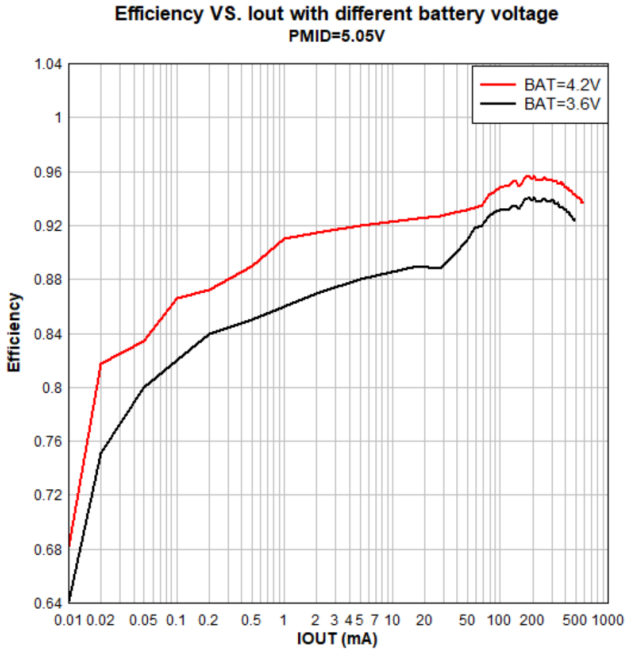


Figure 4. Boost converter efficiency

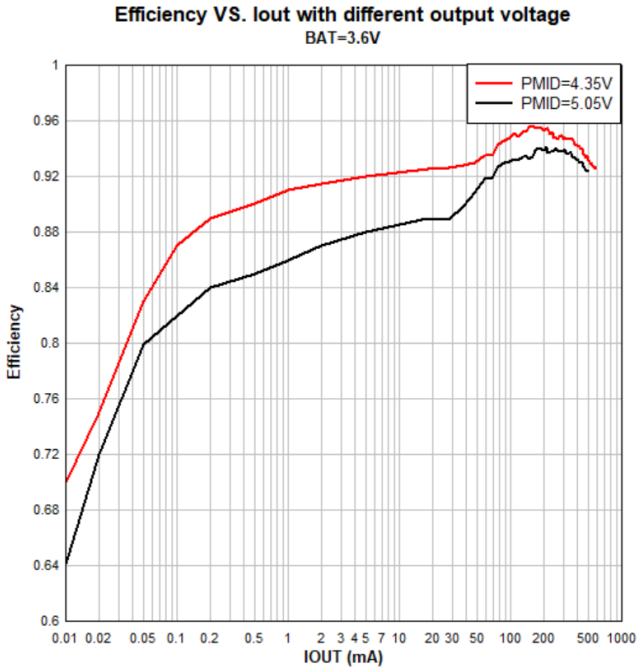


Figure 5. Boost Converter Efficiency.

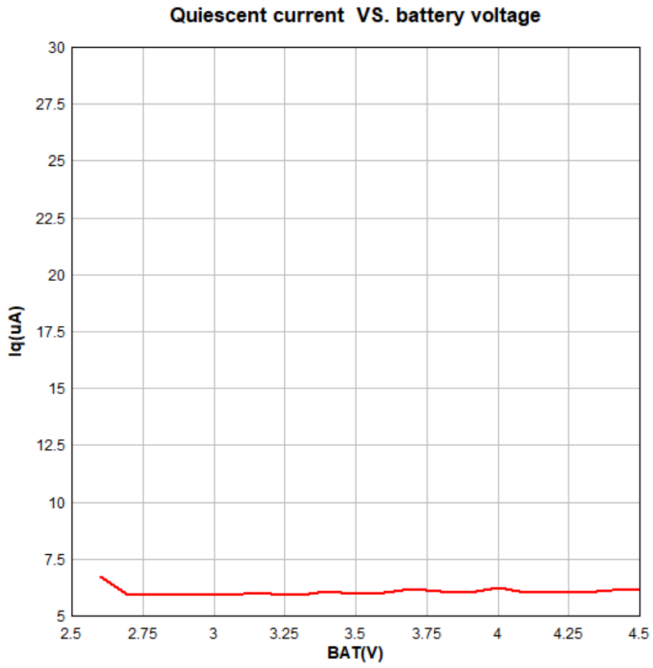
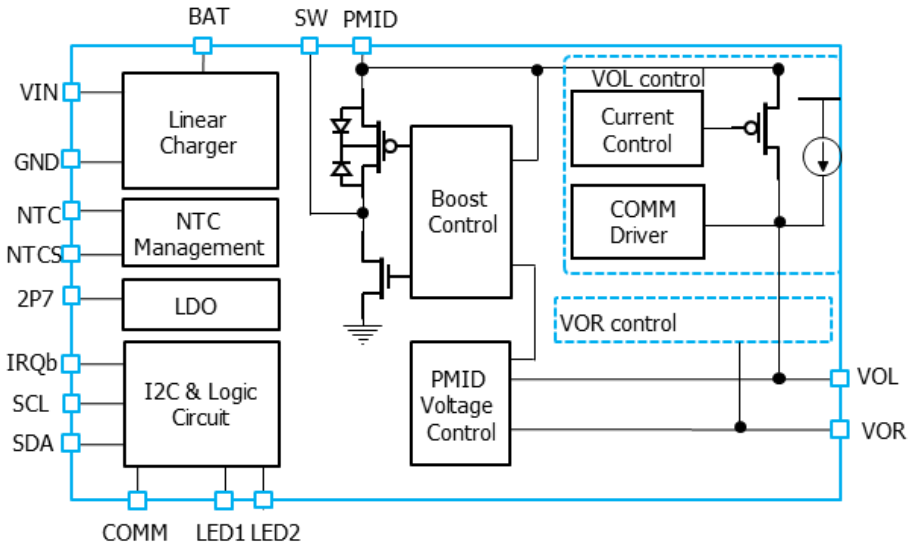


Figure 6. Quiescent current VS. Temperature.

Functional Block Diagram



Detailed Description

Overview

The LP7810A is a TWS charging case management IC that will extend the battery run time when worked together with dedicated battery chargers in the earphone (LP4080). When a power supply is connected to the VIN pin, an internal linear charger will charge the battery in the charging case. A boost regulator and two earphone chargers are offered to charge the earphones. Two earphone detection circuits allow an easy detection of the insertion of the left and the right earphones. A linear regulator is offered to power an external MCU. The 2.7V linear regulator will always be on as long as either the VIN or the BAT pin is powered. An NTC management circuit detects five thresholds to accommodate the compliance of the JEITA guidelines. The LP7810A supports bi-directional communication between the charging case and the earphones with both 5V or 2.7V logic. The LED1 and LED2 pins can be used to drive two external LEDs. Various charging parameters are programmable via an I2C bus and an IRQb interrupt output is provided to interrupt the MCU when an interruptible event occurs.

Power-on Reset (POR)

The LP7810A will perform a power-on reset with each one of the conditions below is met:

1. the BAT rises above the BAT_POR threshold with no VIN
2. the VIN rises above the VIN_UVLO threshold with no battery

All registers will be set to the default values. The external MCU can access all the registers after POR.

Input Section

The VIN voltage is monitored by the internal resistor divider. The linear charger will be shut down when the VIN falls below the under-voltage lockout (UVLO) threshold or rises above the over voltage protection (OVP) threshold. Both the UVLO and OVP comparators have a typical 100-mV hysteresis.

The LP7810A outputs a power good indication signal when the input voltage is below the OVP threshold but above the UVLO threshold. An interrupt is sent out on IRQb pin if VIN cross the UVLO or OVP threshold.

Charge Management

The charger is a typical linear charger with three charging modes, i.e., trickle, constant current (CC), and constant voltage (CV) modes. The EN_CHG can enable the charger. The default value at power-on reset is high to enable the charger.

The linear charger starts charging when all the conditions below are valid:

1. PGD=1.
2. The EN_CHG bit is set to 1.
3. BAT voltage not exceeds the CV voltage.
4. the NTC is in the range of 0℃ to 45℃

The LP7810A monitors the battery voltage and regulates charging current and voltage accordingly after start charging:

1. Trickle charge: The trickle-charge voltage threshold is fixed to 2.8V. The LP7810A starts trickle charging when the battery voltage is below the trickle threshold. The trickle-charge current is fixed to 10% of the CC current.

2. CC charge: The LP7810A starts CC charging when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The CC current is programmable via the I2C bus. Its value is determined by the Charge Current Control register.

3. CV charge: The LP7810A starts CV charging when the battery voltage rises above the CV threshold. The charging decreases gradually until the charging termination is triggered in this phase. The CV voltage is programmable via the Battery CV Voltage register.

4. Termination: The LP7810A terminates charging when the charge current reduces to 13% of the CC current and the battery voltage is higher than the recharge threshold.
5. Recharge: A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage.
6. NTC management:
   a) Charge function will be disabled when the temperature of the NTC circuit is outside 0℃ to 45℃ with 20-ms deglitch time typically.
   b) Discharge function will be disabled when the temperature of the NTC circuit is outside -10℃ to 60℃ with 20-ms deglitch time typically.
7. Charge current foldback： When the die temperature reaches 120oC, the charger current decreases until a new temperature balance is reached.
8. Battery voltage monitor: The LP7810A integrates a 4-bit ADC to convert the battery voltage every 100-ms. The internal register stores the battery voltage information in the Battery Voltage Monitor register. The ADC is disabled when the LP7810A is in standby mode.
9. VIN dynamic power management control (DPM): The charging current is regulated to avoid the VIN crash when the input power source is current limited at a low level. The VIN voltage decreases if the power source current capability is lower than the charging current. When the VIN voltage drops to the VIN_DPM threshold, the LP7810A reduces the charging current until the VIN voltage is kept at 4.4-V typical value. The charging current recovers automatically when the VIN rises above the VIN_DPM.

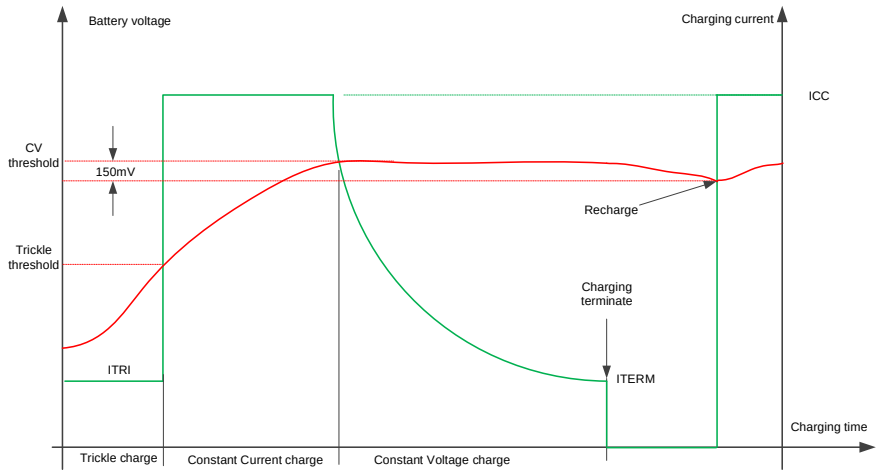


Figure 7. Charging Profile

Earphone Charger

Earphone Detection

An internal programmable 1uA to 20uA pull-up current source is offered for earphone insertion or removal detection.

Insertion detection: When the earphone is not in the charging case, the 1μA pull up current will pull the VOL/R pin to the higher voltage of BAT and PMID. The EN_VOL/R bit should be set to 0 when the pull up current is enabled. When an earphone is inserted, the input pull-down resistor or quiescent current in the earphone will pull the VOL/R pin to low. Once the VOL/R falls 0.7-V below the setting voltage after a 20ms deglitch time, the earphone insertion is detected and an interrupt (iL_inserted or iR_inserted) will be sent to the MCU through the IRQb pin.

Removal detection: The removal of the earphone can be achieved by MCU regular communication to the earphone charger (companion part LP4080). The earphone charger will not send back the acknowledge code which indicates the removal of the earphone. To designs with open-cover detection, once the cover is opened (sensed by Hall-effect sensor), the MCU can turn on the VOL/R again and the earphone can pull a 5-mA current. The LP7810Atriggers a EOC when

the earphone leaves the charging case. In this way, the EOC threshold can be used for removal detection as well.

Short Circuit detection: The short circuit interrupt can be achieved by reusing the COMM pin. The L_RX and R_RX can be enabled all the time when the LP7810A is not is in TX mode. The COMM pin is pulled to low voltage when short circuit happens at the VOL or VOR pins. The COMM pin can be connected to an interrupt input of the MCU.

Boost Regulator

The boost regulator is a 2-uA typical ultra-low quiescent current regulator. The maximum output current is limited to 600mA.

1. **Boost Converter Operation:** The boost regulator has two operation modes. It operates in the voltage step-up mode when the PMID voltage is required to be higher than the case battery voltage. It operates in a by-pass mode when the PMID voltage is required to be lower or equal to the battery voltage. The maximum boost regulator output voltage is programmed by the Maximum Output Voltage of Boost Converter register. The range is between 4.3V- 5.05V.
2. **Feedback selection:** The higher voltage of the VOL and VOR will be selected to set the reference for the PMID output, however, when either VOL or VOR channel is not in the charge mode, that channel of feedback can be disconnected. The disconnection can be performed by setting FBK_L or FBK_R bit to 0. The PMID is regulated at a voltage setting by the Maximum Output Voltage of Boost Converter register when both the FBK_L and FBK_R bit are set to 0.
3. **Battery Under Voltage Lockout (BAT_UV):** The LP7810A integrates battery over discharge protection as well. Discharge will stop when the battery voltage drops below the Battery Discharging Undervoltage Control register, this voltage is programmable in the register BAT_UV[2:0]. The LP7810A enters standby mode when the battery is under BAT_UV threshold and the VIN is not valid at the same time.
4. **Current Limit and Hiccup Operation:** The current flow the high-side FET of the boost regulator is limited to 900mA when the PMID is overloaded or short to ground. The LP7810A shuts down the boost converter if the overload condition lasts 1.2-ms typical time and the BST_OL bit will be set when 1.2-ms expires. After a 30ms hiccup time, the boost converter will perform a new startup.
5. **Enable and Disable:** The EN_BST bit in the Charge Control Register enables the boost regulator. When EN_BST is low, the boost regulator is disabled. When the boost regulator is enabled, it will go through a new soft-start.

Earphone fast charge (EICC) and EEOC

The VOL and the VOR pins provide power to charge the left and the right earphone batteries.

The charging of the earphones is enabled by the EN_VOL or EN_VOR bit. The EN_BST bit needs be set at the same time to enable the boost regulator. The charging current is programmed by the Earphone Charge Current Control Register EICC[4:0]. EOC_L or EOC_R bit will be cleared when charging starts with a 1ms deglitch time.

The EOC_L/R bit is set when the charging current of the earphone drops to 2mA or 10mA, programmable by the EEOC bit in the Earphone Charge Control register, if the VOL/R voltage is higher than a set threshold (4V typically) at the same time. The iEOC_L/R interrupt is sent to the MCU when the EOC_L/R happens.

The EOC_L/R bits are not valid and fixed at 0 when the LP7810A is in standby mode.

Bi-directional Communication

Bi-directional communication to the earphone is supported in the LP7810A. Two independent L_TX and R_TX bits enable the transmission of the signals to the earphones from the COMM pin to the VOL/R pins. L_RX and R_RX bots enable the receiving signals. The pull-up voltage for the communication is selectable by the I2C bus to the PMID voltage or the LDO output to support selectable 5V or 2.7V communication. The pull-up function is enabled by the L_PUP and the R_PUP bits.

To start a communication session, the EN_VOL/R is disabled first. A communication session is always started by the MCU in the charging case sending a request first. Typically, the MCU will first pull the COMM pin to low for certain amount of time (controlled by the MCU) to reset the VOL/R communication line. The duration of such a low signal allows the circuit in the earphone to stop charging on the earphone side. After the bus reset, the internal pull-up resistor in the LP7810A will pull the COMM pin high to start the STOP bit of the UART communication protocol. The COMM is pulled to 2P7 rail with a typical 10k resistor internally when in L_RX or R_RX mode.

The communication baud rate is configurable by setting different pull up resistor as shown in the table.

Table 1 UART communication baud rate configuration

VSEL	Pull-up resistor	Capacitor at VOL pin	Recommend baud rate
2.7V	500Ω	no connection	2Mbps
2.7V	1000Ω	no connection	1Mbps
PMID	2500Ω	no connection	500kbps

NTC Management

When the charging case is in the charge mode or discharge mode, the NTCS outputs the 2P7 bias voltage for the external resistive divider. An NTC resistor with 1% accuracy and with a beta of 3435 is recommended. The NTCS disables the output during the standby mode to reduce the quiescent current. Five thresholds are achieved: -10°C, 0°C, 15°C, 45°C, and 60°C temperature threshold detection. An iNTC interrupt will be sent when the temperature is crossing these thresholds for MCU to take actions according to the temperature.

The NTC [2:0] bits are used to indicate the temperature range in the status register. The MCU can change the charging parameters or disable the charging operations by using the control registers.

The linear charger is forced to be turned off when the temperature is outside the range of 0°C to 45°C.

The NTC[2:0] will be set to 011 when the LP7810A is in standby mode.

2P7 Output

The 2P7 output is an always-on linear regulator output that is powered by either the VIN or the BAT pin. This output is to power the external MCU, the NTC circuit, the internal logic circuit, and the 2.7V communication circuit. A 0.47-uF external ceramic capacitor is required.

Standby Mode

The LP7810A enters standby mode only when the USB is not valid and one of the following conditions is met:

1. EN_VOL and EN_VOR are both set to 0 when EN_BST=1.
2. EN_BST=0.
3. Battery voltage is below the BAT_UV threshold.

Most internal control circuit are disabled in standby mode to save power. The 2.7-V LDO and the communication interface are still available, including the I2C and UART communication.

The battery voltage monitor register and NTC monitor register will not be updated in this mode.

The total quiescent current is 4uA in standby mode. The MCU can decide whether to disable the boost converter, the boost quiescent current is excluded in the quiescent current. The quiescent current will increase 2uA if the boost is enabled. The pull up current of left channel and right channel are excluded in the quiescent current as well.

The LP7810A exits standby mode when each of the following conditions is met:

1. USB is inserted (PGD=1)
2. Battery voltage is above the BAT_UV threshold, EN_BST=1, and EN_VOL or EN_VOR is enabled if the USB is not valid (PGD=0)

LED Outputs

Two LED outputs are offered that can be controlled by the I2C bus. Each pin has 10mA current capability. The LED pins are open drain outputs.

Thermal Shutdown

When the internal junction temperature of LP7810A exceeds the thermal shutdown threshold of 150° C, the LP7810A disables all the power paths. The linear charger, boost converter and VOL/VOR all will be disabled.

I2C Bus and Interrupt

The LP7810A has an I2C bus with an interrupt IRQb pin and internal registers. The LP7810A operates as a slave device and the I2C slave address is 6BH (7bit, **1101011**), a 1 or 0 should be placed at the end of the address which represents read or write operation. The interrupt pin IRQb is an open-drain output that pulls to low when an interruptible event happens in the chip. All of the SDA, SCL and IRQb have internal pull up resistor and no external resistor is needed,

Receiving control inputs from the master device reads and writes the internal registers 00H through 09H. The LP7810A supports both standard mode(100kbps) and fast mode(1Mbps). Both SDA and SCL are pulled up to 2V7 pin with a typical 5.1-k ohm resistor internally.

DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

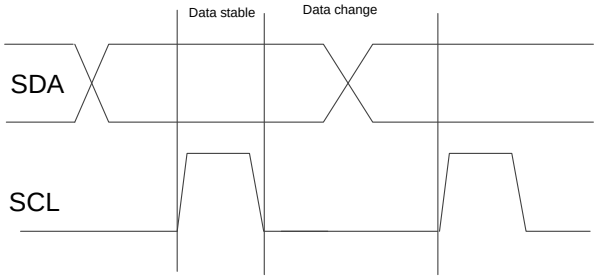


Figure 8. I2C Data validity

Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the SDA line while the SCL is high means a data transfer starts. A rising edge on the SDA line while the SCL is at high means a data transfer stops.

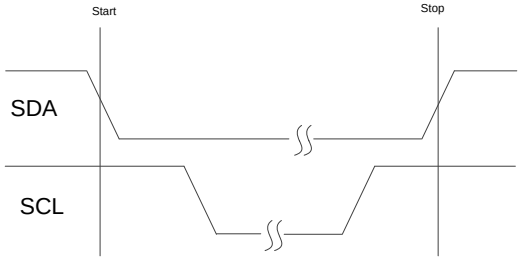


Figure 9. I2C Start and Stop Conditions

Byte format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 10. Single byte write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK
							8 bit	1bit	1bit
							Data from Address	NACK	STOP

Figure 11. Single byte read

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit						
START	Slave address	0	ACK	Register address	ACK	START						
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit	
				Data to Address	ACK	Data to Address	ACK	.....	Data to Address	ACK	stop	

Figure 12. Multi-byte write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit						
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1						
				8 bit	1bit	8 bit	1bit	.....	8 bit	1bit	1bit			
				Data from Address	ACK	Data from Address	ACK	.....	Data from Address	NACK	stop			

Figure 13. Multi-byte read

Register Maps

Table 2 Device Registers

Name	Addr		7	6	5	4	3	2	1	0	
Status register 0	00H	RO	NTC Monitor			BST_OL	EOC_R	EOC_L	CHG	PGD	0x60
Status register 1	01H	RO	BAT_UV	L_INSERT	R_INSERT	TSD	Battery Voltage Monitor				0x00
Interrupt register	02H	RC	iR_inserted	iL_inserted	iEOC_R	iEOC_L	iBST_OL	iNTC	iCHG	iPGD	0x00
Mask register	03H	RW	mR_inserted	mL_inserted	mEOC_R	mEOC_L	mBST_OL	mNTC	mCHG	mPGD	0x00
Control register 0	04H	RW	Battery Discharging Undervoltage Control			ICC: Charge Current Control					0xAE
Control register 1	05H	RW	Reserved								0x0F
Control register 2	06H	RW	Reserved	BYP	Battery CV voltage		Maximum Output Voltage of Boost Converter				0x1F
Control register 3	07H	RW	LED2	LED1	FBK_R	FBK_L	EN_VOR	EN_VOL	EN_BST	EN_CHG	0xF1
Control register 4	08H	RW	PUP_RES	R_PUP	L_PUP	VSEL	R_RX	L_RX	R_TX	L_TX	0x00
Control register 5	09h	RW	Pull-up Current Control		EEOC	EICC: Earphone Charge Current Control					0x44

Note:**RO**: read only; **RC**: read and clear; **RW**: read and write

Status Register 0 /Address: 00H (default: 0x60)

Register 00H monitors the NTC temperature, charging status and PMID overload condition.

The NTC[2:0] bits represent the NTC temperature range.

The BST_OL bit represent PMID is overloaded in bypass mode

The EOC_R and EOC_L bit represents the right earphone or the left earphone is end of charging.

The PGD bit is set when the input voltage is in the range of 4~6V.

Table 3 Status register 0

Bit	Symbol	Description	Read/Write	Default
7	NTC[2]	NTC temperature range: 000: <-10 °C, 001: -10 °C~0 °C, 010: 0 °C~15 °C, 011: 15 °C~45 °C, 100:45°C~60 °C, 101~111:>60 °C	r	011
6	NTC[1]		r	
5	NTC[0]		r	
4	BST_OL	=1 Boost regulator output over-loaded.	r	0
3	EOC_R	=1 when the right earphone is end of charge	r	0
2	EOC_L	=1 when the left earphone is end of charge	r	0
1	CHG	=1 when charger is in trickle, CC, or CV mode.	r	0
0	PGD	=1 when input is between UVLO and OVP.	r	0

Status Register 1 /Address: 01H (default: 0x 00)

Register 01H monitors the die temperature and battery voltage.

The TSD bit sets when the die temperature exceed 150 °C at rising edge and clears when the die temperature falls below 125 °C at falling edge.

The V_BATM[3:0] represents the voltage at BAT pin.

Table 4 Status register 1

Bit	Symbol	Description	Read/Write	Default
7	BAT_UV	Battery uvlo indication	r	000
6	L_INSERT	Left earphone is inserted indication,VOL is at least 700mV lower than the PMID.	r	
5	R_INSERT	Right earphone is inserted indication,VOL is at least 700mV lower than the PMID.	r	
4	TSD	=1 die temperature too high, thermal shutdown	r	0
3	V_BATM[3]	0000:<2.9V, 0001:3.0V, 0010:3.1V, 0011:3.2V 0100:3.3V, 0101:3.4V, 0110:3.5V, 0111:3.6V 1000:3.7V, 1001:3.8V, 1010:3.9V, 1011:4.0V 1100:4.1V, 1101:4.2V, 1110:4.3V, 1111:>4.4V	r	0
2	V_BATM[2]		r	0
1	V_BATM[1]		r	0
0	V_BATM[0]		r	0

Interrupt Register/Address: 02H (default: 0x00).

Register 02H represents the interrupt events.

The iR_inserted and iL_inserted bits represent the right earphone or the left earphone insert interrupt.

The iEOC_R and iEOC_L bits represent the right earphone or the left earphone ends of charge interrupt.

The iBST_OL bit represents the PMID overload interrupt.

The iNTC bit represents the NTC range change or TSD status change interrupt.

The iCHG bit represents the linear charger status change (starts charging or end of charging) interrupt.

The iPGD bit represents the input voltage status change (UVLO, PGD, OVP) interrupt.

Table 5 Interrupt register

Bit	Symbol	Description	Read/Write	Default
7	iR_inserted	right earphone insert interrupt	r/c	0
6	iL_inserted	left earphone insert interrupt	r/c	0
5	iEOC_R	Right earphone EOC interrupt, rising/falling edge	r/c	0
4	iEOC_L	Left earphone EOC interrupt, rising/falling edge	r/c	0
3	iBST_OL	PMID overload interrupt, rising/falling edge	r/c	0
2	iNTC	NTC cross range or thermal shutdown	r/c	0
1	iCHG	Case charging status change, rising/falling	r/c	0
0	iPGD	Input voltage status change, rising/falling	r/c	0

Interrupt Mask Register/Address: 03H (default: 0x00)

Register 03H sets masks for interrupts described in the interrupt register above.

Table 6. Interrupt mask register

Bit	Symbol	Description	Read/Write	Default
7	mR_ins		r/w	0
6	mL_ins		r/w	0
5	mEOC_R		r/w	0
4	mEOC_L		r/w	0
3	mBST_OL		r/w	0
2	mNTC		r/w	0
1	mCHG		r/w	0

0	mPGD		r/w	0

Control Register 0/Address: 04H (default: 0xAE)

Register 04H setting the battery charging current and discharge undervoltage threshold.

Table 7 Charging and Discharging Control Register1

Bit	Symbol	Description	Read/Write	Default
7	BAT_UV[2]	400mV	r/w	Offset: 2.8V. Range: 2.8V~3.5V (000~111) Default:3.3V (101)
6	BAT_UV[1]	200mV	r/w	
5	BAT_UV[0]	100mV	r/w	
4	ICC[5]	480mA	r/w	Offset: 0mA Range: 0~930mA (00000~11111) Default: 420mA (01110)
3	ICC[3]	240mA	r/w	
2	ICC[2]	120mA	r/w	
1	ICC[1]	60mA	r/w	
0	ICC[0]	30mA	r/w	

Control Register1 (Reserved) /Address:05H (default: 0x0F)

Control Register2 /Address: 06H (default: 0x0F)

Register 06H setting the battery charging CV voltage, maximum boost output voltage and bypass mode of VOL and VOR.

Table 8. Control Register 2

Bit	Symbol	Description	Read/Write	Default
7		reserved		
6	BYP	1: force bypass of VOL and VOR	r/w	0
5	BATCV[5]	battery charging CV voltage setting: 00:4.1V, 01:4.2V, 10:4.35V, 11:4.4V	r/w	Default:4.2V(01)
4	BATCV[4]		r/w	
3	V_ BST[3]	maximum voltage of the boost converter: 0000 4.3V, 0001:4.34V, 0010:4.4V, 0011:4.45V, …… 1101:4.95V, 1110:5.0V, 1111:5.05V	r/w	Offset: 4.3V Range: 4.3V~5.05V (0000~1111) Default:5.05V(1111)
2	V_BST[2]		r/w	
1	V_BST[1]		r/w	
0	V_BST[0]		r/w	

Control Register2 /Address: 07H (default: 0xF1)

Register 07H enable or disable the linear charger, boost converter, VOL/VOR and the LED.

Table 9. Control Register 3

Bit	Symbol	Description	Read/Write	Default
7	LED2	Open-drain output. 1=off, 0=on	r/w	1
6	LED1	Open-drain output. 1=off, 0=on	r/w	1
5	FBK_R	Right earphone feedback enable 0=off, 1=on	r/w	1
4	FBK_L	Left earphone feedback enable 0=off, 1=on	r/w	1
3	EN_VOR	1: Right earphone charging enable	r/w	0
2	EN_VOL	1: Left earphone charging enable	r/w	0
1	EN_BST	1: Boost regulator enable	r/w	0
0	EN_CHG	1: Charge enable.	r/w	1

Control Register 4 /Address: 08H (default: 0x00)

Register 08H control the communication interface with earphone.

Table 10 Control Register4

Bit	Symbol	Description	Read/Write	Default

7	PUP_RES	VOL/VOR communication pull-up resistor, 0=500ohm, 1=1000ohm when pull-up bias is set to 2.7V	r/w	0
6	R_PUP	1: VOR communication pull-up enabled.	r/w	0
5	L_PUP	1: VOL communication pull-up enabled.	r/w	0
4	VSEL	pull-up bias voltage: PMID or 2P7 voltage 0 = 2P7, 1=PMID	r/w	0
3	R_RX	1: right earphone receive data enable	r/w	0
2	L_RX	1: left earphone receive data enable	r/w	0
1	R_TX	1: right earphone transmit data enable	r/w	0
0	L_TX	1: left earphone transmit data enable	r/w	0

Earphone Charging Control Register/Address: 09H (default: 0x44)

Register 09H setting the earphone charging current and pull-up current of VOL and VOR.

Table 11. Control Register5

Bit	Symbol	Description	Read/Write	Default
7	PUP[1]	Pull up current. 00: off, 01: 1uA, 10: 7uA, 11: 20uA	r/w	0
6	PUP[0]		r/w	1
5	EEOC	0: 2mA or 1:10mA	r/w	0
4	EICC[4]	VO_L/VO_R current loop limitation: 00000: 30mA, ……, 01000:70mA ……, 01011:100mA, 01100:120mA, ……, 01111:150mA, 10000:200mA, 10001~11111:250mA	r/w	Offset: 30mA Range: 30~250mA (00000~11111) Default: 50mA (00100)
3	EICC[3]		r/w	
2	EICC[2]		r/w	
1	EICC[1]		r/w	
0	EICC[0]		r/w	

Application Information

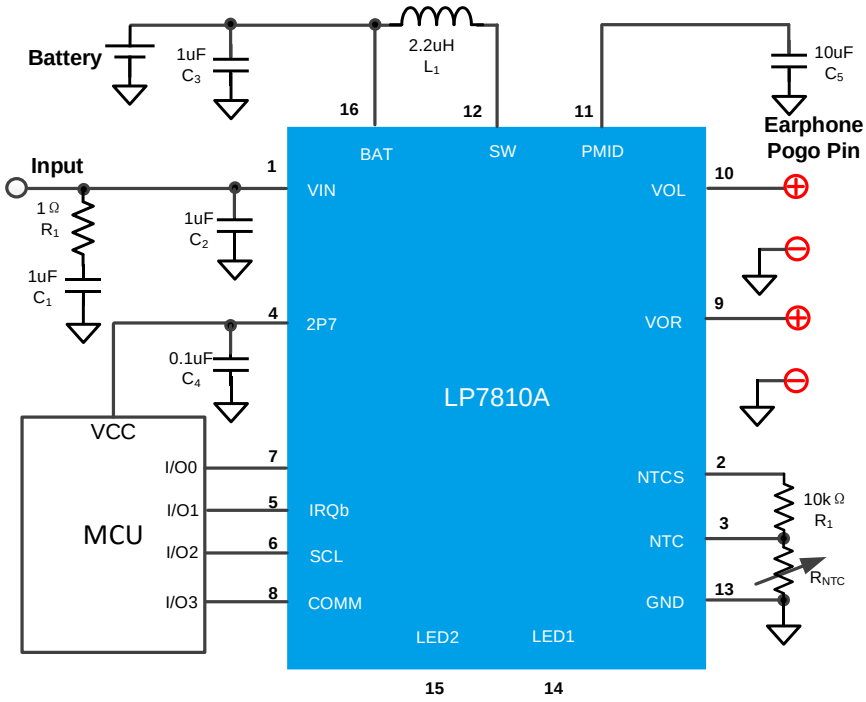


Figure 14. Typical Application circuit

A typical application consists of the multi-function-in-one power management IC of LP7810A and a host MCU. When powering up in default mode, the battery CV voltage of LP7810A is 4.2V, the constant charging current is 420mA, the termination current and trickle charge current is 10% of the constant current. The maximum output voltage of boost converter is 5.1V and the discharge undercharge threshold is 3.3V. The MCU can change all the default values by I2C interface.

Capacitor selection:

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the VIN, BAT, 2P7 and PMID pin to the GND pin. The VIN capacitor C1 should be 25V rating with minimum 1uF capacitance. The BAT capacitor C3 should be at least 6.3V rating with typical 10uF capacitance. The PMID capacitor C5 should be at least 6.3V rating with minimum 10uF capacitance, this capacitor influences the right-half-plane-zero location of the boost converter and should not be too small. The 2P7 linear regulator capacitor C4 should be 0.1uF to ensure the loop stability. All the capacitors should be placed as close as possible to the pins. A 1~10ohm resistor R1 should in series with C1 to help filter the hot-plug spike when USB insertion.

Inductor selection:

The LP7810A is optimized to work with inductor values between 1uH and 2.2uH. For best stability consideration, a 2.2-uH inductor is recommended. The peak current of the inductor should be higher than the saturation current from the inductor's datasheet. A low DCR inductor should be used to get a desired efficiency. As a recommendation, a 2.2-uH inductance with a 80mΩ DCR inductor is a good choice.

NTC design:

As all the trigger point thresholds of the internal NTC comparators are well design with a certain type of NTC resistor, an 10-kΩ NTC resistor with 1% accuracy and with a beta of 3435 is recommended. The R1 should be set to 10-kΩ to cooperate with the 10-kΩ NTC resistor. The following equation helps calculating the trigger point when the NTC resistor changes. All the trigger point thresholds can be found in the electrical characteristics table. The default NTC threshold indicates the temperature of -10 °C, 0 °C, 15 °C, 45 °C, 60 °C.

Typical Waveforms:

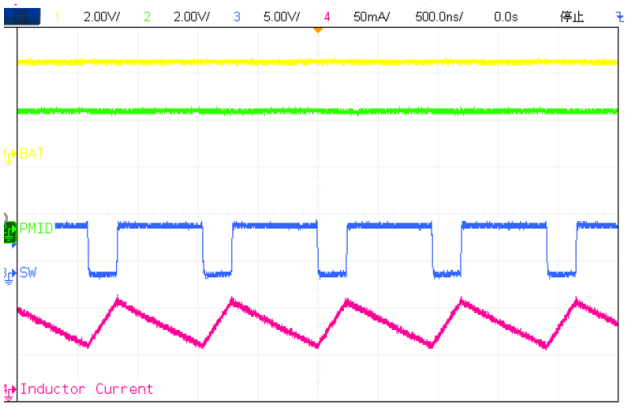


Figure 15. Switching waveform, VIN=4.0V, PMID=5.0V, Iout=0.5A

Figure 16. Switching waveform, VIN=4.0V, short circuit protection

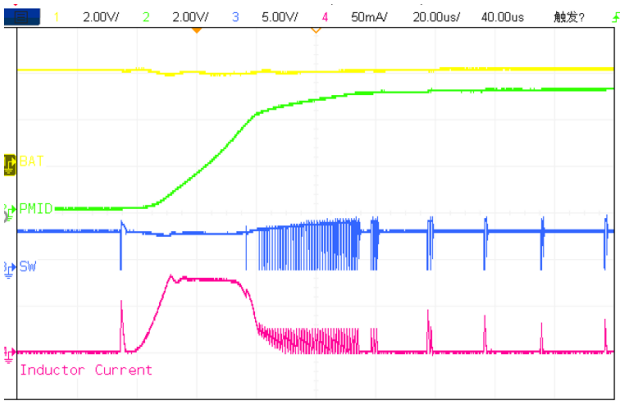


Figure 17. Startup waveform, VIN=4.0V, no load

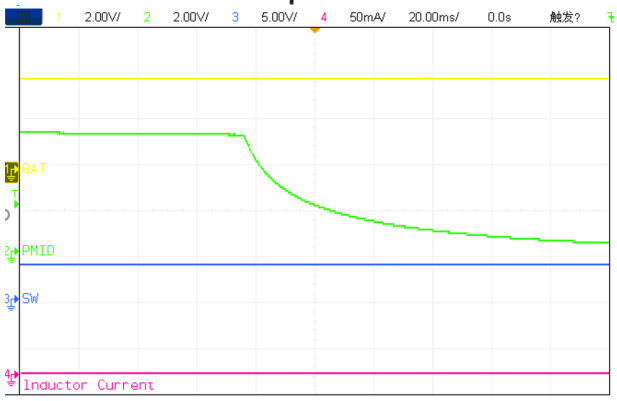


Figure 18. Shutdown waveform, VIN=4.0V, no load

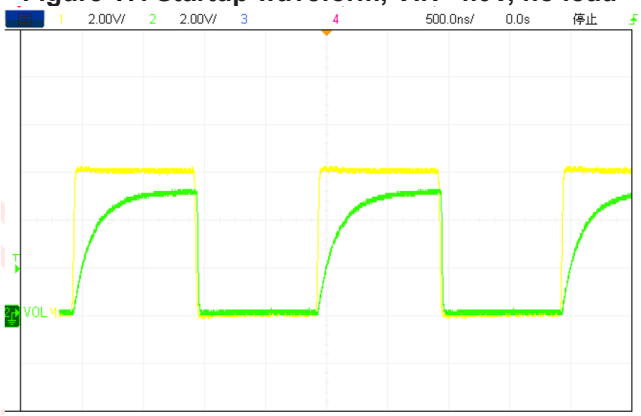


Figure 19. VOL UART TX,1.5Mbps, and COMM VOL

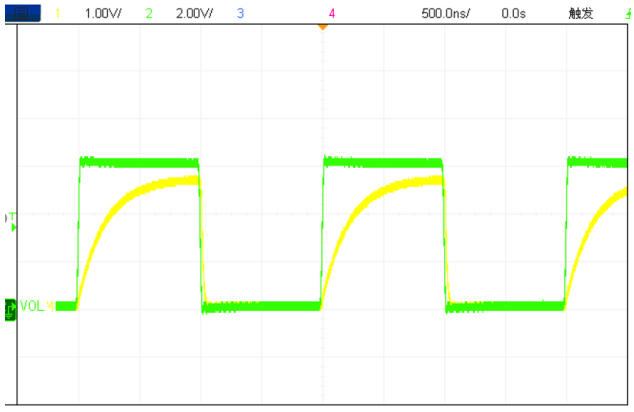


Figure 20. VOL UART RX,1.5Mbps, and COMM VOL

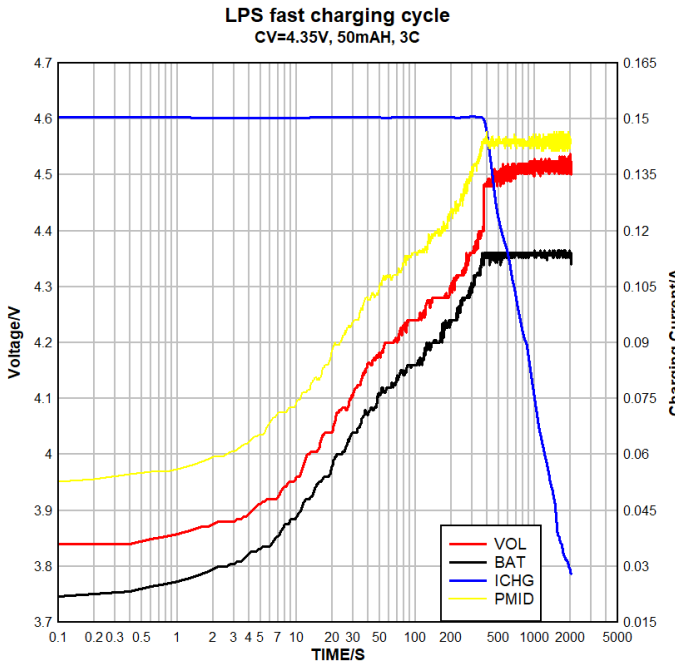


Figure 21. Charging Cycle, Case=3.6V

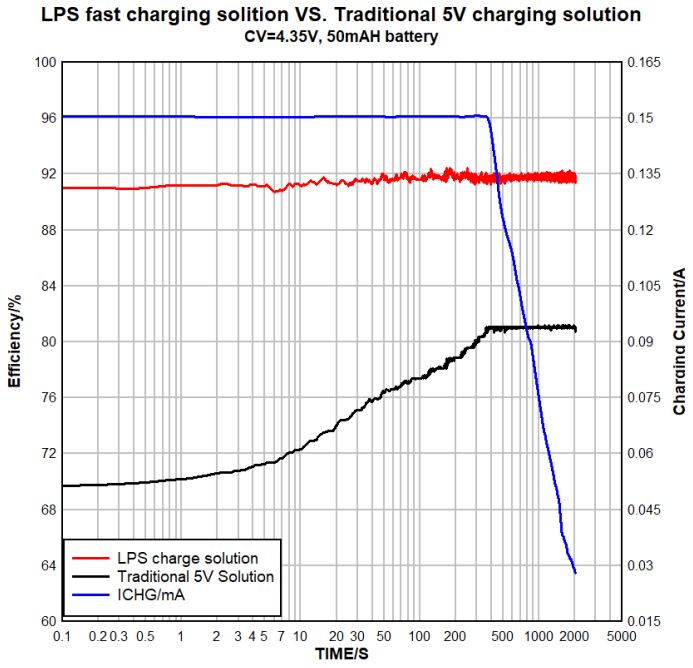


Figure 22. Charging Efficiency, Case=3.6V

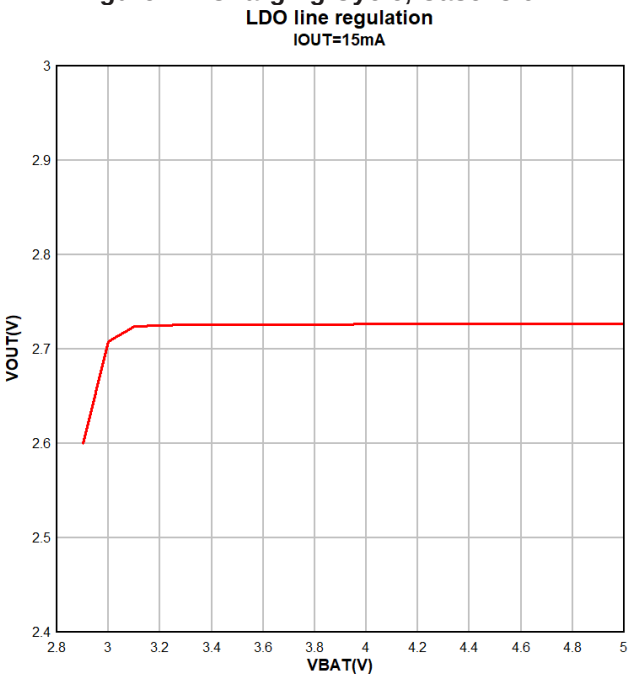


Figure 23. LDO line regulation

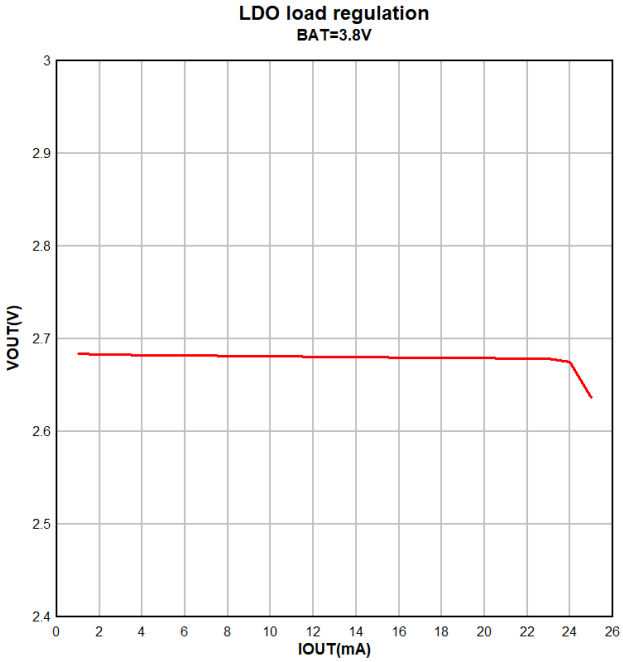


Figure 24. LDO load regulation

PCB Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- the high frequency filtering capacitor C1 C2 C3 C4 C5 should be placed as close to the pin and GND as possible. The C5 PMID capacitor is highlighted.
- both the VIN, VBAT and GND power paths should be wide and short to improve the system efficiency.
- no capacitors should be placed at the VOL and VOR pins to guarantee the UART communication speed.

- the thermal pad should connect to the ground plane to help dissipating the power from the silicon.

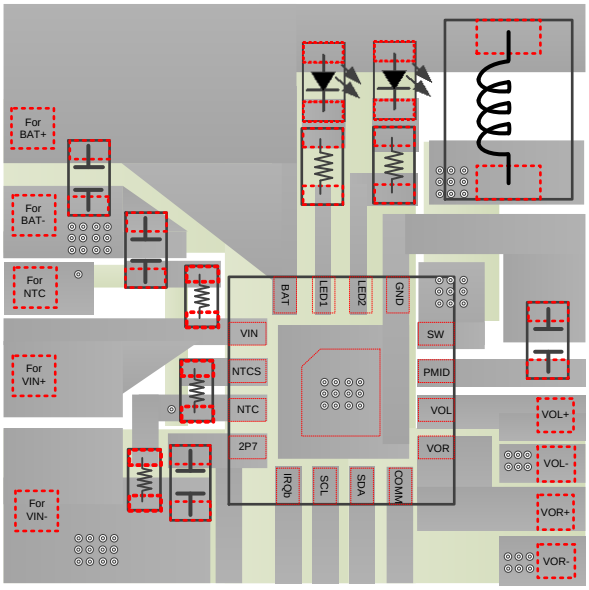
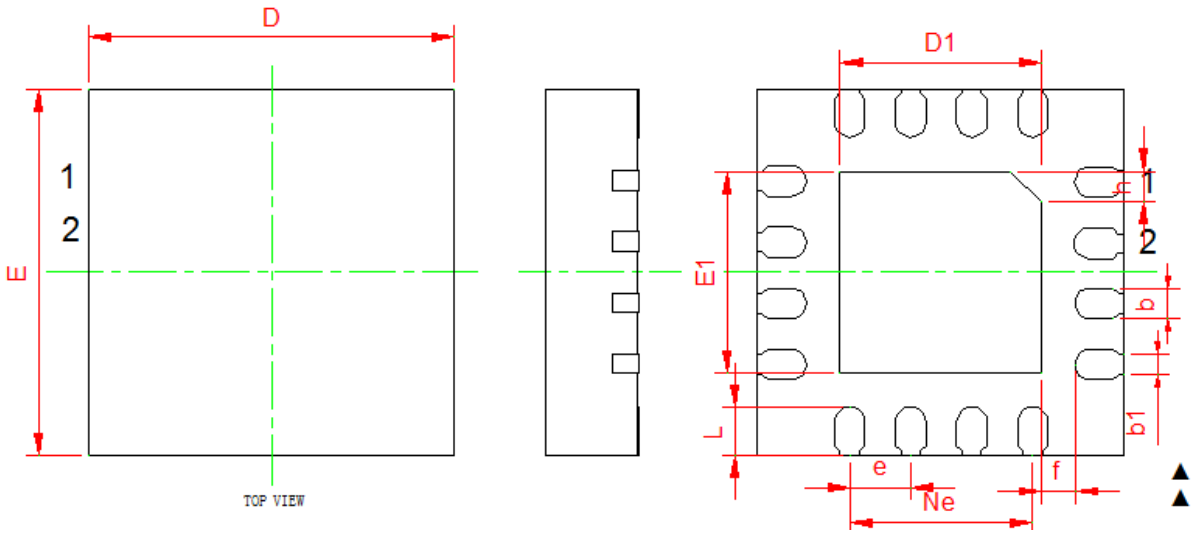
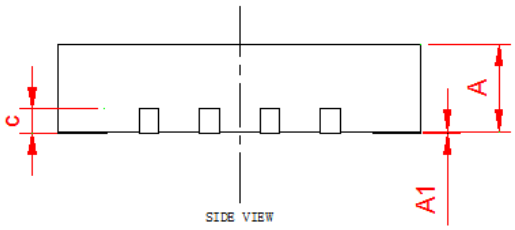


Figure 25. PCB layout example

Packaging Information

QFN-16





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.200	0.250	0.300
b1		0.160REF	
c	0.180	0.210	0.240
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	1.600	1.650	1.700
E1	1.600	1.650	1.700
e		0.500BSC	
Ne		1.500BSC	
f	0.225	0.275	0.325
h	0.200	0.250	0.300
L	0.350	0.400	0.450

Revision History

Revision	Date	Change Description
Rev 0.1p0	8/23/2021	Product Brief
Rev 1p0	1/11/2021	Initial Release
Rev 1p1	10/5/2022	Format update