



Multi-Channel DC-DC Converter for LCD Panels

General Description

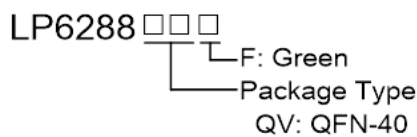
The LP6288 is a multi-channel converter that provides six regulated output voltage. It includes a boost and three buck regulators and VGH and VGL charge pump for TFT LCDs. All output can be programmable via IIC.

V_{AVDD} boost and V_{HAVDD} buck for the Source Driver and the Gamma Buffer. V_{IO} buck and V_{CORE} buck for T-CON. VGH and VGL dual charge pump for the Gate Driver or the Level Shifter. VGH rail can be temperature compensated with GIP technology.

Otherwise, High Voltage Stress Mode (HVS) for V_{AVDD} and V_{HAVDD} and the integrated V_{AVDD} Isolation Switch is implemented. V_{CORE}, V_{HAVDD}, VGH, VGL, GPM and the VGH temperature compensation can be enabled and disabled by IIC programming.

Other features include short circuit protection, thermal shutdown protection and under-voltage lockout (UVLO). The LP6288 is available in a space saving QFN-40 (0.5mm pitch) package.

Order Information



Features

- ◆ Wide V_{IN} Range: 8V to 14V
- ◆ Current-Mode Boost Regulator
 - Isolation Switch PMOS
 - 13.5 to 19.8 Programmable Output Voltage
 - Current Limit Protection
 - Internal Switching Power NMOS Control
- ◆ Buck Regulator for V_{IO}
 - 2.2V to 3.7V Programmable Output
 - 3A Current Limit Protection
- ◆ Buck Regulator for V_{CORE}
 - 0.8V to 3.3V Programmable Output
 - 2.5A Current Limit Protection
- ◆ Buck Regulator for V_{HAVDD}
 - 4.8V to 11.1V Programmable Output
 - 1.7A Current Limit Protection
- ◆ Positive Charge Pump for VGH
 - 20V to 40V Programmable Output
 - 0V to 15V Gate Shaping Voltage
 - Temperature Compensation
- ◆ Negative Charge Pump for VGL
 - -5.5V to -14.5V Output Voltage
- ◆ Reset Function for XAO
- ◆ Under-Voltage Protection
- ◆ Over-Temperature Protection
- ◆ IIC Compatible Interface for Register Control
- ◆ Available in QFN-40 (6x6mm)
- ◆ RoHS Compliant and Halogen Free
- ◆ Pb-Free Package

Applications

- ◆ TFT LCD TV
- ◆ TFT LCD Monitor
- ◆ TFT LCD Panel

Marking Information

Device	Marking	Package	Shipping
LP6288QVF	LPS LP6288 YWX	QFN6X6-40	3K/REEL
Y: Year code. W: Week code. X: Batch number.			



Typical Application Circuit

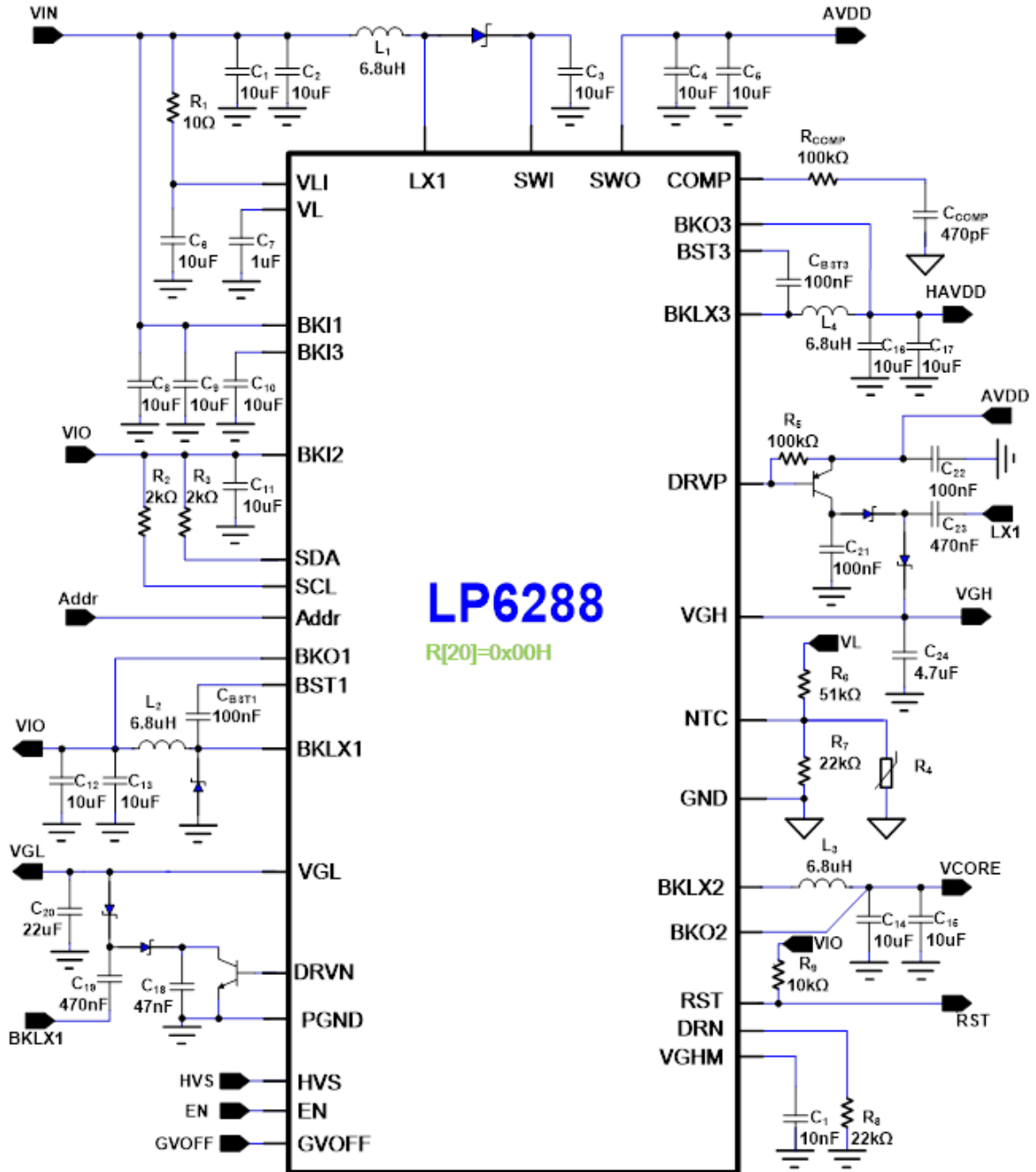


Figure 1. Typical Application Circuit of LP6288



Pin Configuration

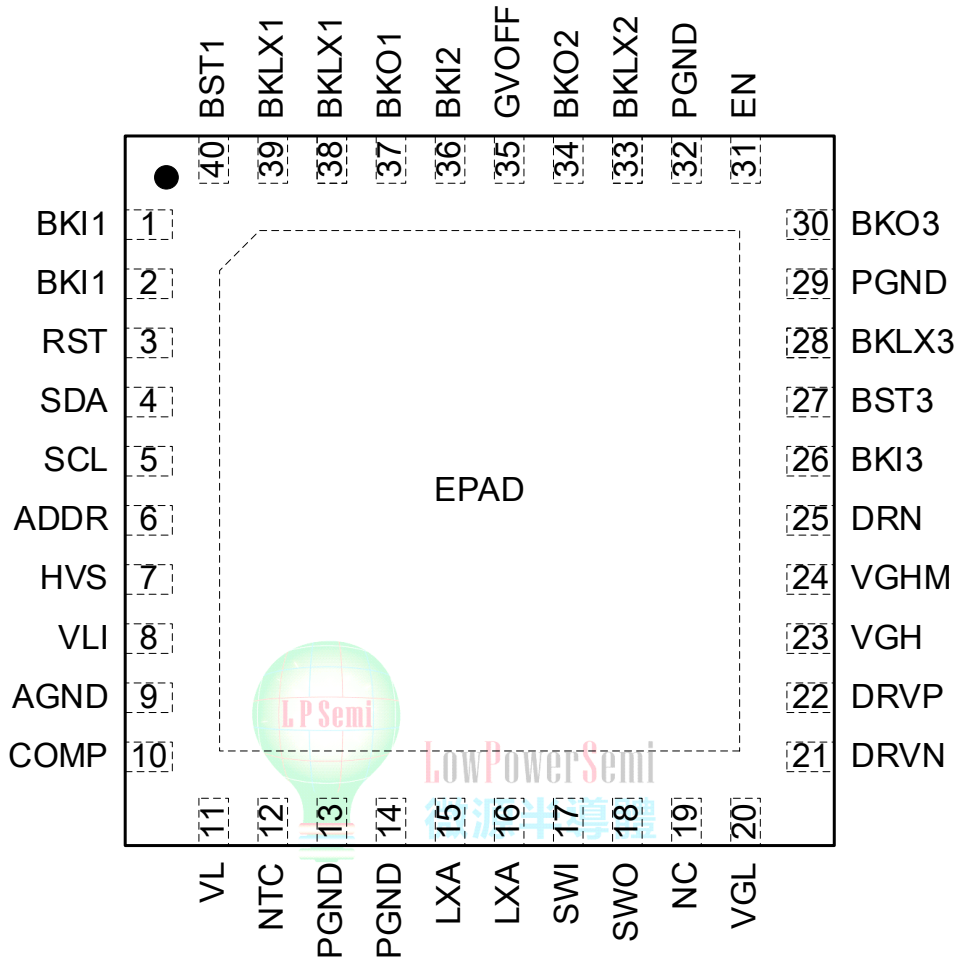


Figure 3. QFN-40 Package (6mm x 6mm) - Top View



Function Block Diagram

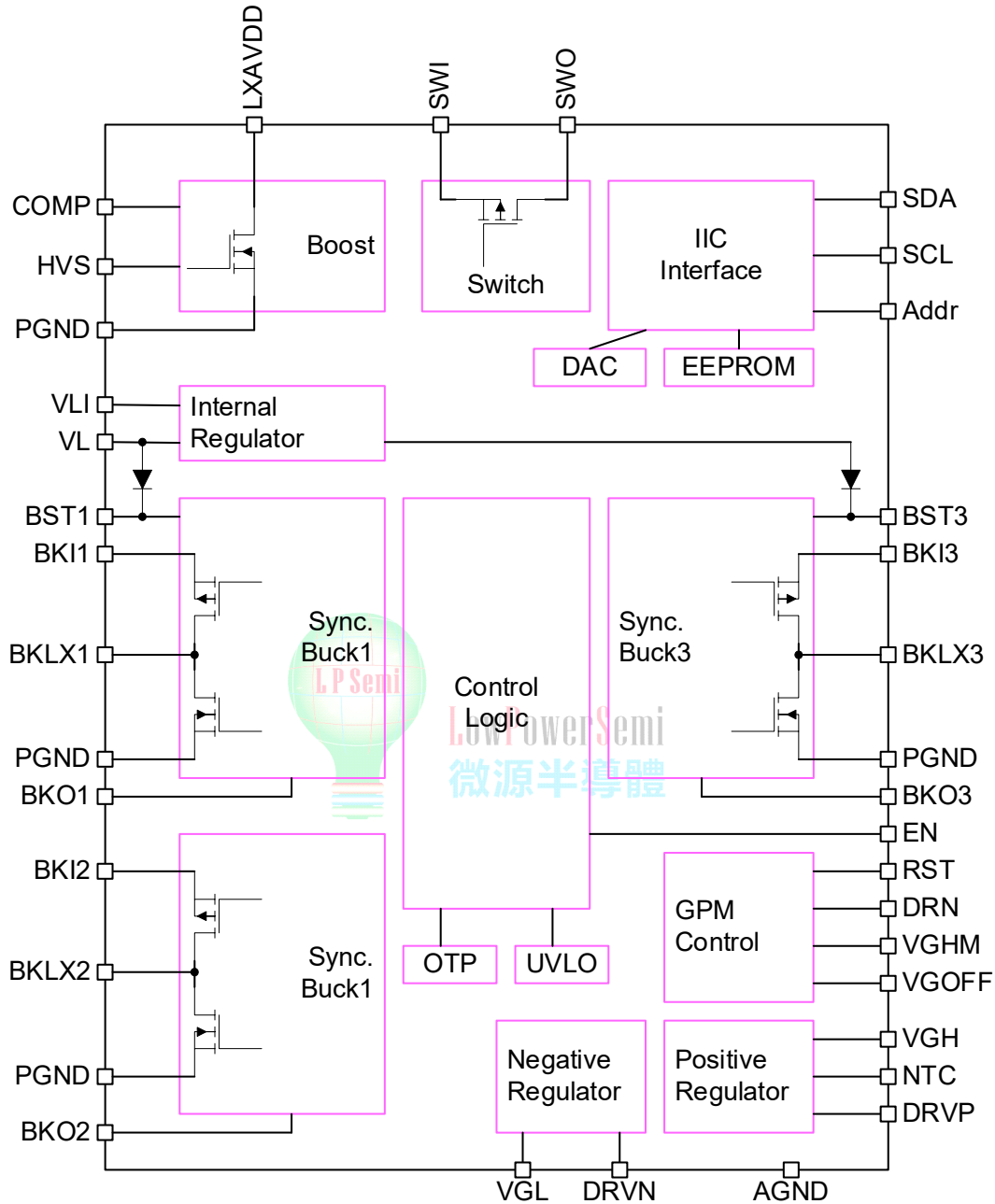


Figure 4. Function Block Diagram



Functional Pin Description

Pin NO.	Pin Name	Description
1, 2	BKI1	Buck1 Regulator Power Source Input Pin. BKI1 is internally connected to BKI3.
3	RST	Reset Function Output. Open drain.
4	SDA	IIC interface data signal.
5	SCL	IIC interface clock signal.
6	Addr	IIC interface Device Address Bit0.
7	HVS	Boost High Voltage Stress Enable.
8	VLI	Internal Regulator and Startup Circuitry Supply Input. Connect a Ceramic capacitor between VLI and GND.
9	AGND	Analog Ground.
10	COMP	Boost Regulator Error Amplifier Compensation Pin.
11	VL	Internal Regulator Output. Bypass VL to AGND a capacitor.
12	NTC	Temperature Compensation Pin.
13, 14, 29, 32	PGND	Power Ground.
15, 16	LXAVDD	Boost Regulator Switching Node. Connect the inductor and Schottky diode to LXAVDD.
17	SWI	Isolation Switch Input.
18	SWO	Isolation Switch Output.
19	NC	No Connection.
20	VGL	Negative Charge Pump Output Sense Pin.
21	DRVN	VGL Charge-Pump Regulator Driver Output.
22	DRVP	VGH Charge-Pump Regulator Driver Output.
23	VGH	Positive Charge Pump Output Sense Pin and Power Supply for GPM.
24	VGHM	GPM Output
25	DRN	GPM Discharge Pin. Connect a resistor between DRN and GND.
26	BKI3	Buck3 Regulator Power Source Input Pin. BKI3 is internally connected to BKI1.
27	BST3	Buck3 Bootstrap Pin. Connect a 0.1uF Ceramic capacitor from BKLX3 to BST3.
28	BKLX3	Buck3 Regulator Switching Node. Connect the inductor to BKLX3.
30	BKO3	Buck3 Regulator Output Sense Pin. Connect BKO3 to the HAVDD output.
31	EN	Enable Pin.
33	BKLX2	Buck2 Regulator Switching Node. Connect the inductor to BKLX2.
34	BKO2	Buck2 Regulator Output Sense Pin. Connect BKO2 to the VCORE output.
35	GVOFF	Gate Voltage Shaping Control Pin. When GVOFF is high: VGH and VGHM are ON and the VGHM and DRN are OFF. When GVOFF is low: VGH and VGHM are OFF and the VGHM and DRN are ON.
36	BKI2	Buck2 Regulator Power Source Input Pin.
37	BKO1	Buck1 Regulator Output Sense Pin. Connect BKO1 to the VIO output.
38, 39	BKLX1	Buck1 Regulator or Switching Node. Connect the inductor and Schottky diode to BKLX1.
40	BST1	Buck1 Bootstrap Pin. Connect a 0.1uF Ceramic capacitor from BKLX1 to BST1.
41(EP)	PGND	Exposed Pad. Power ground, connect this pin to AGND.



Absolute Maximum Ratings ^{Note 1}

◇ VLI, EN, SWI, SWO, BKI3, BKO3, LXAVDD to PGND	-----	-0.3V to +24V
◇ SWI to SWO	-----	-0.3V to +24V
◇ VL, NTC, COMP, BKO1, BKI2, BKO2, DRVN to PGND	-----	-0.3V to +6V
◇ SDA, SCL, Addr, HVS, GVOFF, RST to PGND	-----	-0.3V to +6V
◇ BKLX1, BKLX2, BKLX3 to PGND	-----	-0.3V to (BKIx +0.3V)
◇ BKLX1, BKLX2, BKLX3 to PGND (for 20ns)	-----	-2V to (BKIx +0.3V)
◇ BST1 to BKLX1, BST3 to BKLX3	-----	-0.3V to +6V
◇ VGH, VGHM, DRN, DRVP to PGND	-----	-0.3V to +40V
◇ VGL to VL	-----	-24V to +0.3V
◇ PGND to AGND	-----	-0.3V to +0.3V
◇ Operating Junction Temperature Range (T _J)	-----	-40°C to +150°C
◇ Operation Ambient Temperature Range (T _A)	-----	-40°C to +85°C
◇ Storage Temperature Range	-----	-65°C to +150°C
◇ Maximum Soldering Temperature (at leads, 10sec)	-----	+260°C
◇ Maximum Junction Temperature	-----	+150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. The functional operation of the device or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

◇ Thermal Resistance		
QFN-40 (6x6), θ_{JA}	-----	37.19°C/W
QFN-40 (6x6), θ_{JC}	-----	11.07°C/W



Electrical Characteristics

($T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
VLI Input Supply Voltage	V_{VLI}		8		14	V
Internal Oscillator Frequency	F_{OSC}		600	750	900	kHz
V_{IN} Supply Current	I_Q	All LX Not Switching		0.2		mA
		All LX Switching		7		mA
Input UVLO Threshold	V_{UVLO}	V_{IN} Rising		7.4		V
UVLO Threshold Hysteresis	ΔV_{UVLO}	Falling Hysteresis		400		mV
Maximum Duty Cycle	D_{MAX}			90		%
Fault Trigger Duration	T_{Fault}			50		ms
Thermal Shutdown Threshold	T_{SD}	Temperature Rising		150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	ΔT_{SD}			30		$^{\circ}\text{C}$
Internal Regulator						
VL Output Voltage	V_{VL}			5		V
VL Output Voltage Tolerance	ΔV_{VL}		-1		1	%
Logic Input (SDA, SCL, Addr, HVS, EN, GVOFF)						
Input Leakage Current (SDA, SCL, Addr, EN, GVOFF)	I_{IH}, I_{IL}	$V_{IN}=0\text{V}$ or $V_{IN}=3.3\text{V}$		0.1		μA
Input Threshold Voltage	V_{IH}	Logic High.	1.7			V
	V_{IL}	Logic Low			0.6	
IIC Output Low Voltage	V_{IIC}	$I_{sink} = 6\text{mA}$		0.3		V
Reset Function						
RST Output Voltage	V_{RST}	$I_{sink} = 1\text{mA}$		0.2	0.4	V
Voltage Detection Level	V_{RST}	V_{VLI} falling		8.9		V
		Rising Hysteresis		300		mV
Gate Pulse Modulator (GPM)						
Gate Shaping Lower Limit Voltage		Programmable Step 5V	0		15	V
VGHM Switch ON Resistance	R_{DS_GHM}	GVOFF = 'H'		3	5	Ω
DRN Switch ON Resistor	R_{DS_DRN}	GVOFF = 'L'		3	5	Ω
GVOFF to VGHM Delay Time			0.15	0.25	0.35	μs



Electrical Characteristics (Continued)

($T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Isolation Switch						
Switch Supply Voltage	V_{VLI}		8		20	V
SWI Over Voltage Protection	V_{OVP}		20.5	21.5	22.5	V
SWI OVP Hysteresis	ΔV_{OVP}			1.5		V
P-MOS Switch On Resistance	R_{DS_ISO}	$I_{LX} = 0.5\text{A}$		100	200	m Ω
Switch Current	I_{Limit}			3		A
Short Circuit Trigger Duration		$I_{SWI} \geq 2.5\text{A}$		1.5		ms
		$I_{SWI} \geq 4.5\text{A}$		100		us
Boost Regulator						
Switch Leak Current	I_{Leak}	$V_{LX} = 16.5\text{V}$		1	10	uA
SWO Regulation Voltage Range	V_{SWO}	$V_{HVS} = 0\text{V}$, Programmable Step 0.1V	13.5		19.8	V
SWO Regulation Voltage Tolerance			-1		+1	%
HVS Voltage	V_{HVS}	Programmable Step 0.2V	0		3	V
NMOS Switch-ON Resistance	R_{DS_BSTN}	$I_{LX1} = 0.5\text{A}$		100		m Ω
PMOS Switch-ON Resistance	R_{DS_BSTP}	$I_{LX1} = 0.1\text{A}$		10	15	Ω
Current Limit	I_{Limit}		4.25	5	5.75	A
Current Limit Negative Offset	I_{Limit_Offset}	Programmable Step -0.2A	0		2.8	A
Soft Start Time	T_{SS_BST}	Programmable Step 10ms		20	30	ms
SWO Line Regulation		$8\text{V} \leq V_{IN} \leq 14\text{V}$, $I_{Load} = 100\text{mA}$		0.005		%/V
SWO Load Regulation		$V_{IN} = 12\text{V}$, $1\text{mA} \leq I_{Load} \leq 2\text{A}$		0.25		%/A
SWO Fault Trip Level		V_{SWO} Falling	76	80	84	%
Transconductance	G_m	$\Delta I = 5\text{uA}$		240		uA/V
Voltage Gain	A_v			1000		V/V



Electrical Characteristics (Continued)

($T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Negative Charge Pump Controller (VGL)						
Charge Pump Soft Start Time	T_{SS_CPN}			3		ms
VGL Output Voltage Range	VGL	Programmable Step -0.5V	-14.5		-5.5	V
Regulation Voltage Tolerance			-1		+1	%
DRVN Source Current	I_{DRVN}	$V_{DRVN} = 0.6\text{V}$	5	8		mA
VGL Load Regulation Error		$V_{DRVN} = 0.6\text{V}$, $-50\mu\text{A} < I_{DRVN} < -1\text{mA}$		11	25	V/A
VGL Fault Trip Level		VGL Rising	75	80	85	%
Positive Charge Pump Controller (VGH)						
Charge Pump Soft Start Time	T_{SS_CPP}			3		ms
VGH Output Voltage Range	VGH	$V_{GH} = V_{GH_L} + V_{GH_H}$	20		40	V
VGH_L Regulation Voltage Range	VGH_L	Programmable Step 1V	20		35	V
VGH Offset Voltage	VGH_H	Programmable Step 1V	0		15	V
Regulation Voltage Tolerance			-2		+2	%
DRVP Source Current	I_{DRVP}	$V_{GH} = V_{GH} - 20\%$	5			mA
		$V_{GH} < 20\%$		80		μA
VGH Load Regulation Error		$V_{DRVP} = 16\text{V}$, $50\mu\text{A} < I_{DRVN} < 1\text{mA}$		11	25	V/A
VGH Fault Trip Level		VGH Falling	75	80	85	%



Electrical Characteristics (Continued)

($T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Buck1 Converter (VIO)						
Buck1 Soft Start Time	T_{SS_BK1}			3		ms
BKO1 Output Voltage Range	V_{BKO1}	Programmable Step 0.1V	2.2		3.7	V
Regulation Voltage Tolerance		$I_{Load} = 10\text{mA}$	-2		+2	%
H-Side NMOS On Resistance	R_{DS_BK1H}	$I_{LX} = 0.5\text{A}$		150		$\text{m}\Omega$
L-Side NMOS On Resistance	R_{DS_BK1L}	$I_{LX} = 0.5\text{A}$		6		Ω
Buck1 Current Limit	I_{Limit_BK1}		3	3.5	4	A
Buck1 Line Regulation		$8\text{V} \leq V_{IN} \leq 14\text{V}$, $I_{Load} = 10\text{mA}$		0.005		%/V
Buck1 Load Regulation		$V_{IN} = 12\text{V}$, $1\text{mA} \leq I_{Load} \leq 2.5\text{A}$		0.25		%/A
Buck1 Under Voltage Threshold		V_{BKO1} Falling	75	80	85	%
Buck2 Converter (VCORE)						
Operating Frequency	F_{BK2}			2		MHz
Maximum Duty Cycle	D_{MAX}				100	%
Buck2 Soft Start Time	T_{SS_BK2}			3		ms
Buck2 Output Voltage Range	V_{BKO2}	Programmable Step 0.1V	0.8		3.3	V
Regulation Voltage Tolerance		$I_{Load} = 10\text{mA}$	-2		+2	%
H-Side PMOS On Resistance	R_{DS_BK2H}	$I_{LX} = 0.5\text{A}$		160		$\text{m}\Omega$
L-Side NMOS On Resistance	R_{DS_BK2L}	$I_{LX} = 0.5\text{A}$		160		$\text{m}\Omega$
Buck2 Current Limit	I_{Limit_BK2}		2.5	3	3.5	A
Buck2 Line Regulation		$8\text{V} \leq V_{IN} \leq 14\text{V}$, $I_{Load}=10\text{mA}$		0.1		%/V
Buck2 Load Regulation		$V_{IN}=12\text{V}$, $1\text{mA} \leq I_{Load} \leq 1\text{A}$		0.1		%/A
Buck2 Under Voltage Threshold		V_{BKO2} Falling	70	75	80	%
Buck3 Converter (HAVDD)						
Buck3 Output Voltage Range	V_{BK3}	Programmable Step 0.1V	4.8		11.1	V
Regulation Voltage Tolerance		$I_{Load} = 10\text{mA}$	-1		+1	%
H-Side NMOS On Resistance	R_{DS_BK3H}	$I_{LX} = 0.5\text{A}$		200		$\text{m}\Omega$
L-Side NMOS On Resistance	R_{DS_BK3L}	$I_{LX} = 0.5\text{A}$		200		$\text{m}\Omega$
Buck3 Current Limit	I_{Limit_BK3}		1.7	2.0	3.5	A
Buck3 Line Regulation		$8\text{V} \leq V_{IN} \leq 14\text{V}$, $I_{Load} = 10\text{mA}$		0.1		%/V
Buck3 Load Regulation		$V_{IN} = 12\text{V}$, $1\text{mA} \leq I_{Load} \leq 1\text{A}$		0.1		%/A
Buck3 Over Voltage Threshold	V_{OVP_BK3}	V_{BKO3} Rising	115	120	125	%
Buck3 Under Voltage Threshold	V_{UVP_BK3}	V_{BKO3} Falling	75	80	85	%



Electrical Characteristics (Continued)

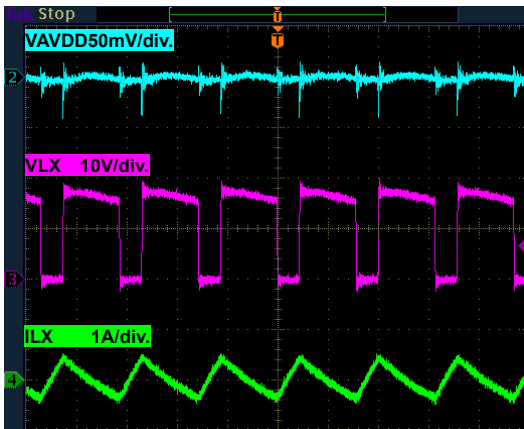
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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
IIC Timer Characteristics						
Serial Clock Frequency	F _{SCL}		0		1	MHz
Bus Free Time Between STOP and START Conditions	t _{BUF}		1.3			us
Hold Time (Repeated) START Condition	t _{HD, DAT}		0.6			us
SCL Pulse-Width Low	t _{LOW}		1.3			us
SCL Pulse-Width High	t _{HIGH}		0.6			us
Setup Time for a Repeated START Condition	t _{SU, STA}		0.6			us
Data Hold Time	t _{HD, DAT}				800	ns
Data Setup Time	t _{SU, DAT}		100			ns
SDA and SCL Receiving Rise Time	t _r		20+0.1 CB		300	ns
SDA and SCL Receiving Fall Time	t _f		20+0.1 CB		300	ns
SDA Transmitting Fall Time	t _{fF}		20+0.1 CB		250	ns
Setup Time for STOP Condition	t _{SU, STO}		0.6			us
Bus Capacitance	C _B				400	pF
Pulse Width of Suppressed Spike	t _{SP}				50	ns
EEPROM Start Up Blanking Time		IC power up initialize	--	2	10	ms
Program EEPROM Blanking Time			350	--	--	ms
Read EEPROM Blanking Time			--	1.5	5	ms



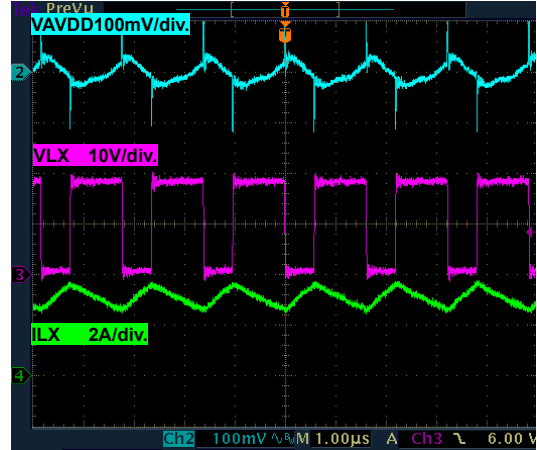
Typical Performance Curves

$T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified.



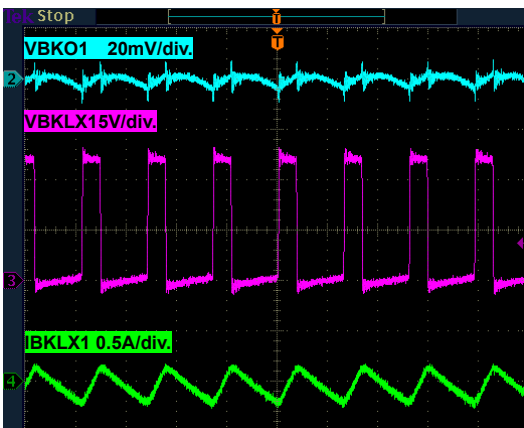
1us/div.

Figure 5. Boost Steady State Light Load (50mA)



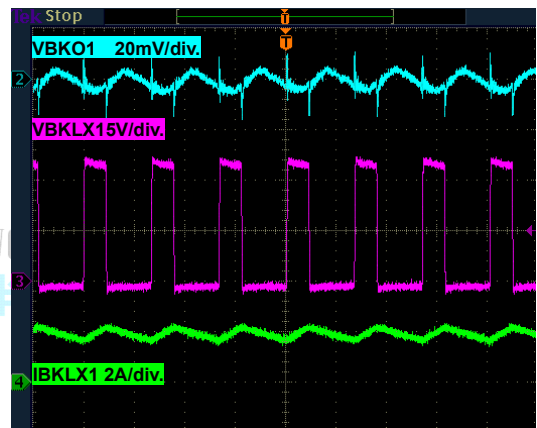
1us/div.

Figure 6. Boost Steady State Heavy Load (1.6A)



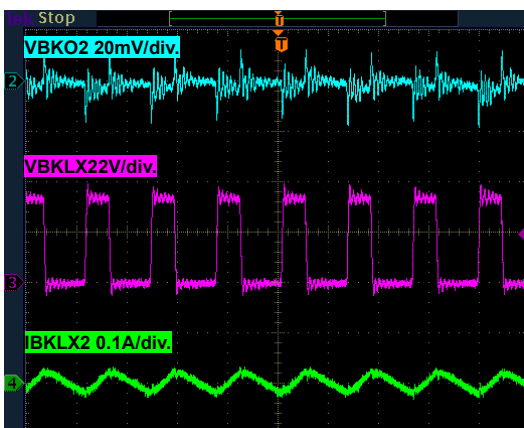
1us/div.

Figure 7. Buck1 Steady State Light Load (50mA)



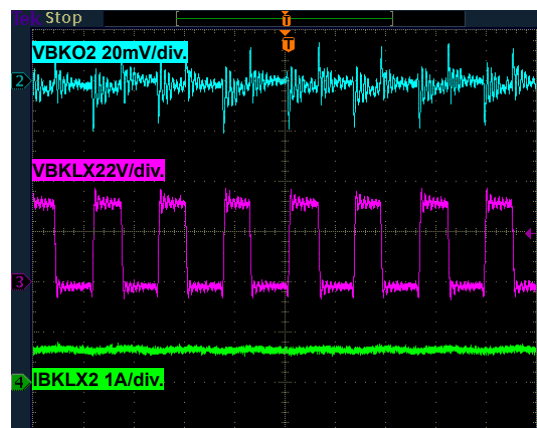
1us/div.

Figure 8. Buck1 Steady State Heavy Load (2A)



400ns/div.

Figure 9. Buck2 Steady State Light Load (50mA)



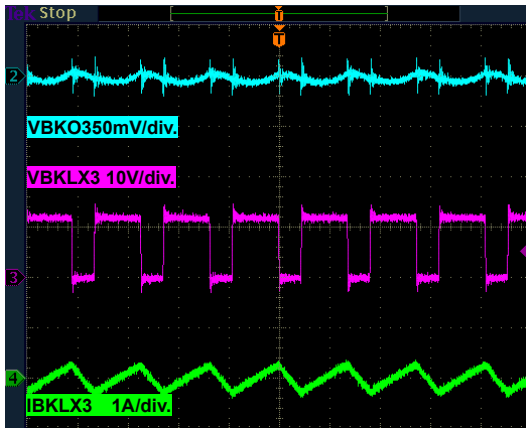
400ns/div.

Figure 10. Buck2 Steady State Heavy Load (0.8A)



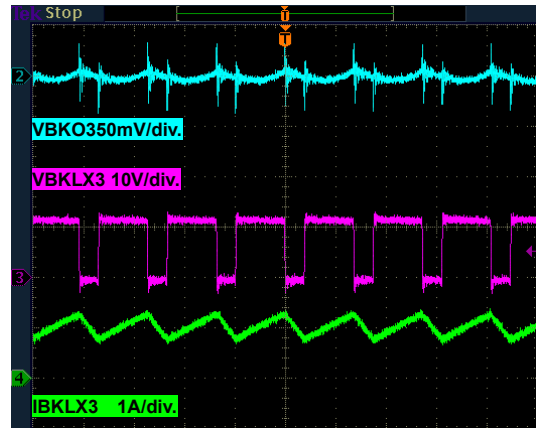
Typical Performance Curves (Continued)

$T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified.



1us/div.

Figure 11. Buck3 Steady State Light Load (50mA)



1us/div.

Figure 12. Buck3 Steady State Heavy Load (1A)

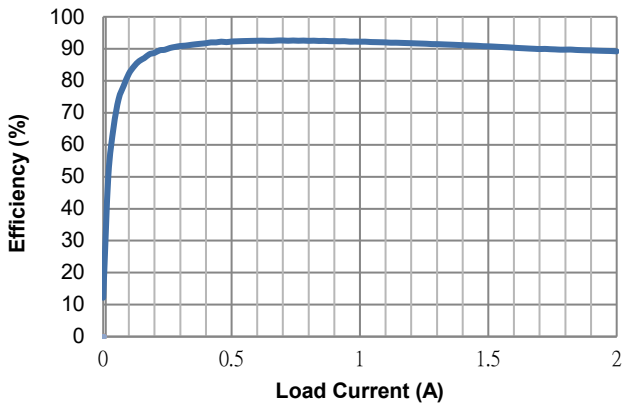


Figure 13. Boost Efficiency (Internal MOS)

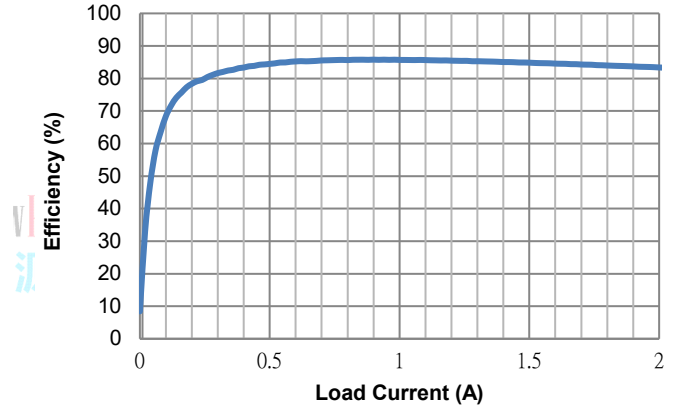


Figure 14. BK1 Efficiency

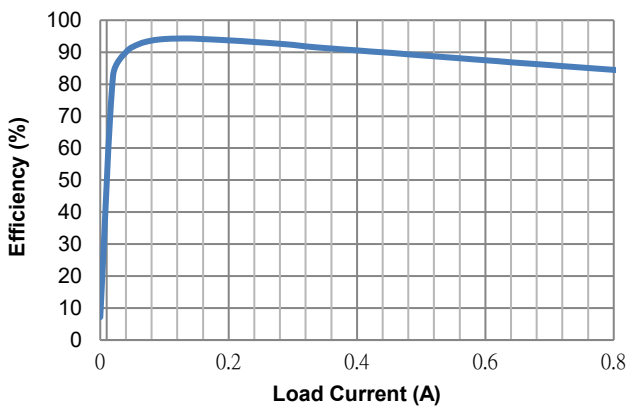


Figure 15. BK2 Efficiency

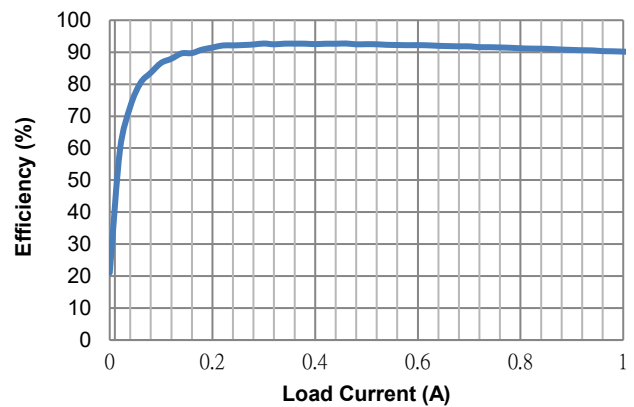
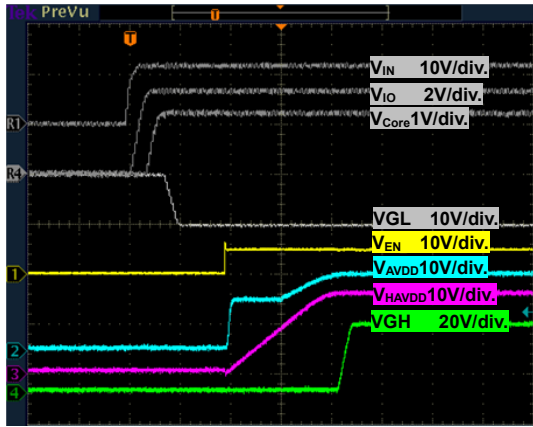


Figure 16. BK3 Efficiency



Typical Performance Curves (Continued)

$T_A=25^{\circ}\text{C}$, $V_{LI}=V_{BK1,3}=12\text{V}$, $V_{AVDD}=16.8\text{V}$, $V_{IO}=3.3\text{V}$, $V_{CORE}=1.2\text{V}$, $V_{HAVDD}=8.1\text{V}$, $V_{GH}=28\text{V}$, $V_{GL}=-10.3\text{V}$, unless otherwise specified.



10ms/div.

Figure 17. Power On Sequence





Power On/Off Sequence

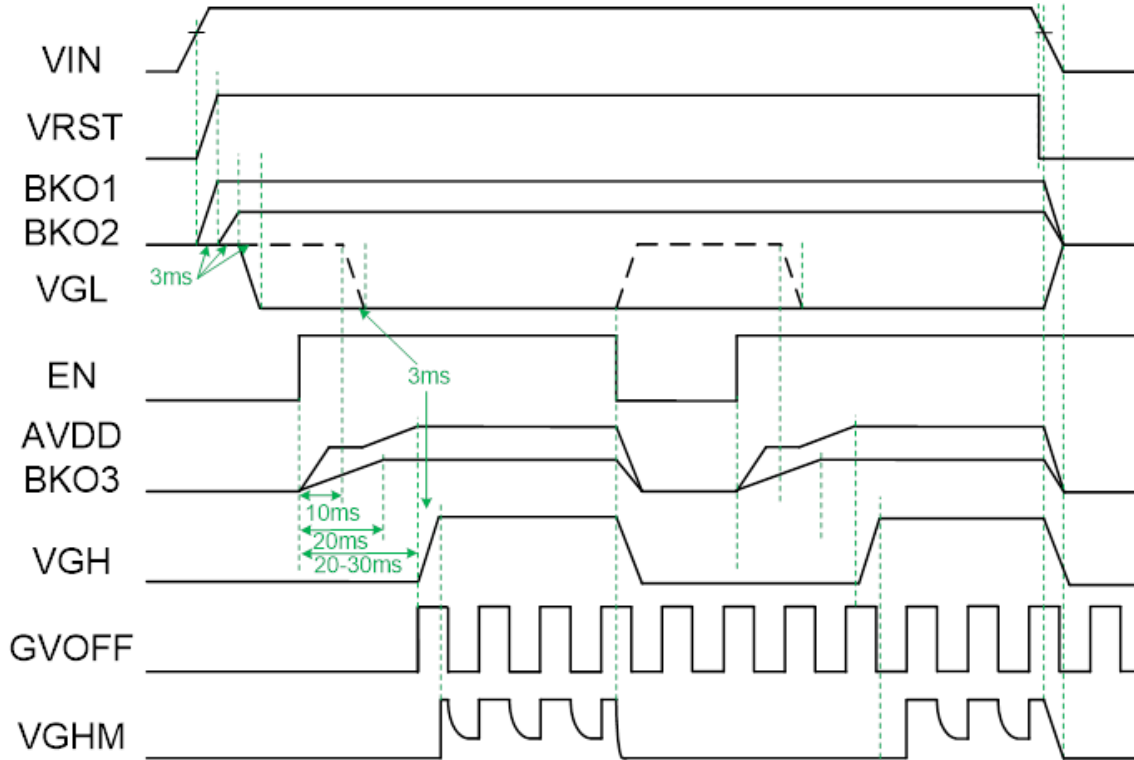
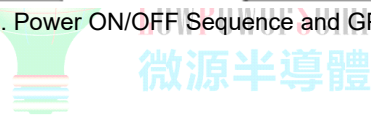


Figure 18. Power ON/OFF Sequence and GPM Control



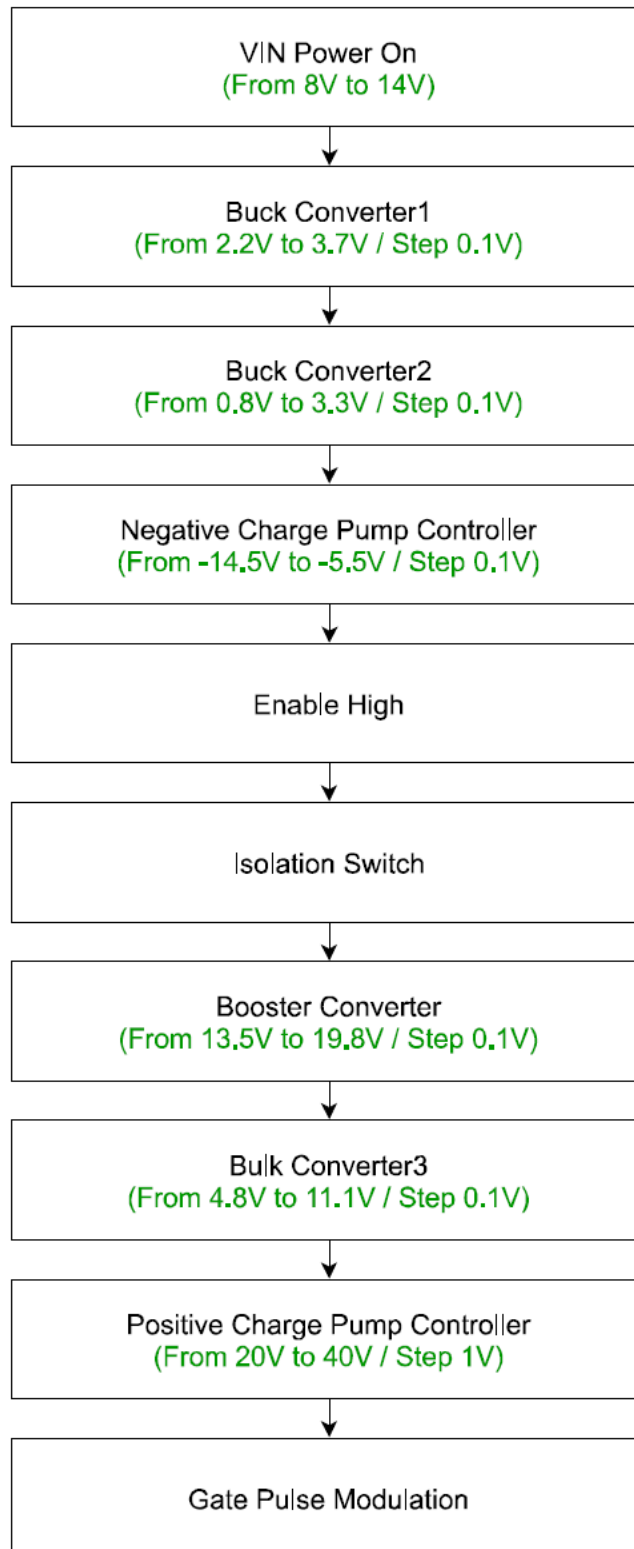


Figure 19. Power On Sequence and Function Step



Application Information

The LP6288 is a multi-channel power supply for TFT LCD panels. It contains a boost regulator, three buck regulators, a positive charge pump and a negative charge pump, GPM, and temperature compensation for positive voltage.

Under Voltage Lockout (UVLO)

The LP6288 had an UVLO internal circuit that enables the device once the voltage on the VIN voltage exceeds the UVLO threshold voltage.

Boost Converter (AVDD)

The LP6288 uses fixed-frequency, current mode architecture to regulate the output voltage. The output voltage and soft start time can be adjustable by internal register R[04h].

Boost Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisted of Rcomp, Ccomp (As Figure 1, 2). Choosing Rcomp to set high frequency integrator gain for fast transient response and Ccomp to set the integrator zero to maintain loop stability.

Boost Over Voltage Protection

The boost converter has an over voltage protection to protect the switch at the SWI pin. When the SWI voltage rises above 21.5V (Typ.), the boost converter will turn the MOS off and stop switching. Until the output voltage falls below the over voltage threshold, the converter will resume operation.

Boost Over Current Protection

The internal power MOS switch current is monitored cycle-by-cycle and it's limited to set by R[03h] that the value does not exceed 3.4A (Typ.). But in external mode R[20h] = 0x01, the OCP level can be set by Rcs (As Figure 2) and senses inductor current to compare with current limit value. When the inductor current exceeds the current limit, the switching will turn off immediately. It prevents large current damaging the external component.

Boost Under Voltage Protection

When SWO voltage is under 80% of the setting, the LP6288 activation an internal timer. If the fault status continues for 50ms, LP6288 will be shut down.

Boost Short Circuit Protection

The LP6288 incorporates a short circuit protection to protect itself and external component. In case Any voltage sense is lower than 40% of the setting voltage level, it will be shut down immediately until VIN power cycled.

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 20μF input capacitor is sufficient for most applications. For a lower output power requirement application, this value can be decreased.

Boost Diode Selection

To achieve high efficiency, Schottky diode is good choice for low forward drop voltage and fast switching time. The output diode rating should be able to handle the maximum output voltage, average power dissipation and the pulsating diode peak current.

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitors are recommended. The tantalum capacitors can be used as well, but the ESR is bigger than ceramic capacitor. The output voltage ripple consists of two components: one is the pulsating output ripple current flows through the ESR, and the other is the capacitive ripple caused by charging and discharging.

$$V_{\text{RIPPLE}} = V_{\text{RIPPLE(ESR)}} + V_{\text{RIPPLE(C)}} \\ \cong I_{\text{PEAK}} \times R_{\text{ESR}} + \frac{I_{\text{PEAK}}}{C_{\text{OUT}}} \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}} \times F_{\text{OSC}}}$$

Inductor Selection

For a better efficiency in high switching frequency converter, the inductor selection has to use a proper core material such as ferrite core to reduce the core loss and choose low-ESR wire to reduce copper loss. The most important point is to prevent the core saturated when handling the maximum peak current. Using a shielded inductor can minimize radiated noise in sensitive applications. The maximum peak inductor current is the maximum input current plus the half of inductor ripple current. The calculated peak current has to be smaller than the current limitation in the electrical characteristics. A typical setting of the inductor ripple current is 20% to 40% of the maximum input current. If the selection is 40%, the maximum peak inductor current is

$$I_{\text{PEAK}} = I_{\text{IN(MAX)}} + 0.5 \times I_{\text{RIPPLE}} = 1.2 \times I_{\text{IN(MAX)}} \\ = 1.2 \times \left[\frac{I_{\text{OUT(MAX)}} \times V_{\text{OUT}}}{\eta \times V_{\text{IN(MIN)}}} \right]$$

The minimum inductance value is derived from the following equation:

$$L = \frac{\eta \times V_{\text{IN(MIN)}}^2 \times [V_{\text{OUT}} - V_{\text{IN(MIN)}}]}{0.4 \times I_{\text{OUT(MAX)}} \times V_{\text{OUT}}^2 \times F_{\text{OSC}}}$$

Depending on the application, the recommended inductor value is 6.8μH.



Application Information (Continued)

Buck1 Converter (V_{IO})

The non-synchronous current mode buck1 converter operates with PWM architecture with 750kHz operation frequency and fast transient response. The converter drivers an internal N-MOS, it need connect a 100nF ceramic capacitor between the BST1 and BKLX1 to provide gate driver voltage. It's necessary to connect a Schottky diode between BKLX1 to GND. The output voltage can be adjustable by internal register. The converter has an internal soft start 3ms (Typ.).

Buck1 Over Current Protection

The Buck1 offers cycle-to-cycle and peak 3.5A (typ.) current limit for high-side MOS. The current limit is relatively constant regardless of duty cycles.

Buck1 Over Voltage Protection

The buck converter has an over voltage protection. When the BKO1 voltage rises above 110%, the Buck1 converter turn off the BKLX1. Until the voltage sense falls below the over voltage threshold, the converter will resume operation.

Buck1 Under Voltage Protection

When the BKO1 drop below 80% of its nominal output, and the status continues for 50ms, LP6288 will be shut down until VIN power restart.

Buck1 Short Circuit Protection

The LP6288 provides short circuit protection function to prevent the device damage from short condition. When the BKO1 sense is lower than 40% of the setting voltage level, the LP6288 will be shut down immediately until VIN power cycled.

Buck1 Diode Selection

When the power MOS turns off, the path of the current is through the diode connected between the switch output and ground. This diode must have a minimum voltage drop and quick recovery time, therefore the Schottky diodes are recommended. Whatever make sure the Schottky diode's reverse voltage rating is greater than the maximum voltage, and the current rating is greater than the maximum current.

Buck2 Converter (V_{CORE})

The synchronous current mode buck2 converter operates with PWM architecture with 2MHz operation frequency and fast transient response. The converter drivers an internal High site P-MOS and Low site N-MOS. The output voltage can be adjustable by internal register. The converter has an internal soft start 3ms (Typ.).

Buck2 Over Current Protection

The Buck2 offers cycle-to-cycle and peak 3A (typ.) current limiting for high-side MOS. The current limit is relatively constant regardless of duty cycles.

Buck2 Over Voltage Protection

The buck converter has an over voltage protection. When the BKO2 voltage rises above 110%, the Buck2 converter turn off the BKLX2. Until the voltage sense falls below the over voltage threshold, the converter will resume operation.

Buck2 Under Voltage Protection

When the output voltage drops below 80% of its nominal output, and the status continues for 50ms, LP6288 will be shut down until VIN power restart.

Buck2 Short Circuit Protection

The LP6288 provides short circuit protection function to prevent the device damage from short condition. When the BKO2 sense is lower than 40% of the setting voltage level, the LP6288 will be shut down immediately until VIN power cycled.



Application Information (Continued)

Buck3 Converter (V_{HAVDD})

The synchronous current mode buck3 converter operates with PWM architecture with 750kHz operation frequency and fast transient response. The converter drives an internal N-MOS, it need connect a 100nF ceramic capacitor between the BST3 and BKLX3 to provide gate driver voltage. The converter drives an internal High site and Low site N-MOS. The output voltage can be adjustable by internal register. The converter has an internal soft start 20ms.

Buck3 Over Current Protection

The Buck3 offers cycle-to-cycle and peak ±2.0A (typ.) current limit for its internal MOS. The current limit is relatively constant regardless of duty cycles.

Buck3 Over Voltage Protection

The buck converter has an over voltage protection. When the BKO3 voltage rises above 120%, the Buck3 converter turn off the BKLX3. Until the voltage sense falls below the over voltage threshold, the converter will resume operation.

Buck3 Under Voltage Protection

When the output voltage drops below 80% of its nominal output, and the status continues for 50ms, LP6288 will be shut down until VIN power restart.

Buck3 Short Circuit Protection

The LP6288 provides short circuit protection function to prevent the device damage from short condition. When the BKO3 sense is lower than 40% of the setting voltage level, the LP6288 will be shut down immediately until VIN power cycled.

Buck Input Capacitor Selection

The use of the input capacitor is filtering the switch spike voltage and the input voltage ripple. For better input bypassing, low-ESR ceramic capacitors are recommended. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

This formula has a maximum at $V_{IN} = 2 \times V_{OUT}$, where $I_{IN(RMS)} = I_{OUT}/2$. For the input capacitor, a 20μF low-ESR ceramic capacitor is recommended.

Buck Output Capacitor Selection

The output capacitor is used to keep the output voltage and source the load transient current. When operating in constant current mode, the output ripple can analysis by two components:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

The following equation shows the form of the ripple contributions.

$$V_{RIPPLE(ESR)} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times ESR$$

$$V_{RIPPLE(C)} = \frac{V_{OUT}}{8 \times F_{OSC}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the main frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, ESR is the equivalent series resistance value of the output capacitor, and the C_{OUT} is the output capacitor.

Buck Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. A nice compromise value between size and efficiency is to set the peak-to-peak ripple current ΔI_L between 20%~40% of the maximum current. Then the inductance can be calculated with the following equation:

$$\Delta I_L = 0.3 \times I_{OUT(MAX)}$$

$$L = \frac{V_{OUT}}{F_{OSC} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

To guarantee enough output current, peak inductor current must be lower than the high-side MOSFET current limit.



Application Information (Continued)

Positive Charge Pump (VGH)

The gate-high regulator is to provide the TFT-LCD gate on voltage. The charge pump can provide a programmable output voltage by register R[08h] and R[09h]. A temperature compensation for VGH is implemented. The charge pump has an internal soft start 3ms (Typ.).

VGH Temperature Compensation

When temperature compensation function is enabled, the VGH voltage is dependent on V_{TC} , and adjustable from 20V to 40V. The V_{TC} value can calculation as below equation:

$$V_{TC} = V_L \times \frac{(R_4 // R_7)}{(R_4 // R_7) + R_6}$$

$$V_{GH} = \begin{cases} V_{GH_L} & , V_{TC} \leq 1V \\ V_{GH_L} + V_{GH_H} \times (V_{TC} - 1), & 1V < V_{TC} < 2V \\ V_{GH_L} + V_{GH_H} & , V_{TC} \geq 2V \end{cases}$$

Figure 20 exhibited the VGH temperature compensation curve. When V_{TC} under 1V, the VGH voltage will be equal VGH_L register R[08h] setting voltage, and V_{TC} large than 2V, the VGH voltage will be equal VGH_L register add VGH_H register R[09h] setting voltage.

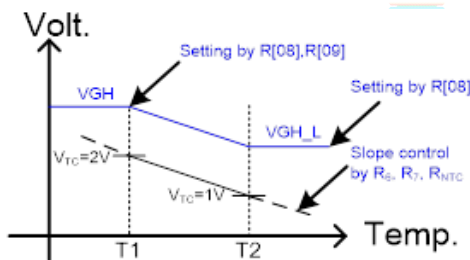


Figure 20. VGH Temperature Compensation

Negative Charge Pump (VGL)

The gate-low regulator is to provide the TFT-LCD gate on voltage. Operation of the negative linear regulator is similar to the positive linear regulator. The charge pump can provide a programmable output voltage by internal register R[0Bh]. The charge pump has an internal soft start 3ms (Typ.).

Gate Pulse Modulator (GPM)

The GPM is controlled by the frame signals from timing controller to modulate the Gate-On voltage, VGHM, which acts a flicker compensation circuit to reduce the coupling effect between gate lines and pixels. It also can delay the Gate-On voltage while power on for achieving a correct power on sequence for gate driver ICs. Both of the power on delay time and the falling time of the Gate-On voltage are programmable by external capacitor and resistor.

The start-up delay of high voltage switch control block is controlled by VGH power ready signal. The discharge slope is control by the VGHM pin gate capacitance and the DRN pin external resistor. LP6288 can set the gate pulse modulation stop level by register. When the stop level voltage is reached the DRN function will stop, and VGHM output is high impedance until GVOFF goes high again.

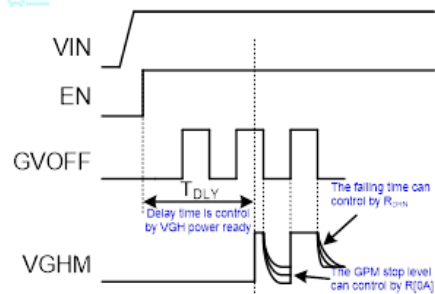


Figure 21. GPM Function

Over Temperature Protection

The LP6288 device enters over temperature protection (OTP) if its junction temperature exceeds 150°C (Typ.). During over temperature protection none of the device's functions are available. To resume normal operation, the junction temperature needs to cool down then the outputs will restart.



Application Information (Continued)

1. IIC Interface Specification

The LP6288 can easily modify the parameters by IIC bus, that slave address is show below:

Slave Address							
A6	A5	A4	A3	A2	A1	A0	W/R
0	1	0	0	0	0	Addr	0/1

IIC is a two-wire serial interface developed, the bus consists of a clock line (SCL) and a data line (SDA) with pull-up structures. The LP6288 works as a slave mode, and address can set by Addr pin. The data transfer protocol follows IIC Bus Specification's standard mode (100kbps) and fast mode (400kbps).

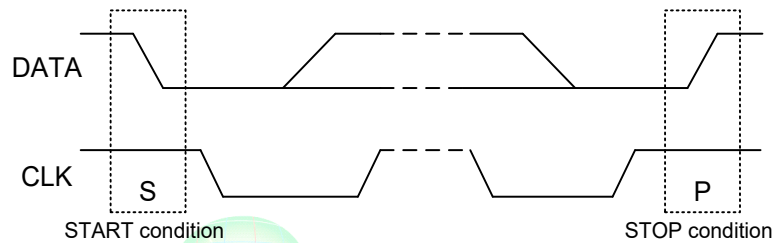


Figure 23. START and STOP Conditions

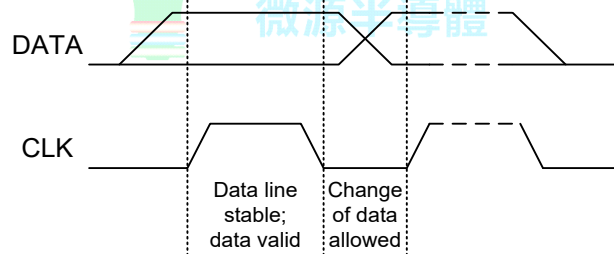


Figure 24. Bit transfer on the Serial Interface



Application Information (Continued)

2. Write Data to Register

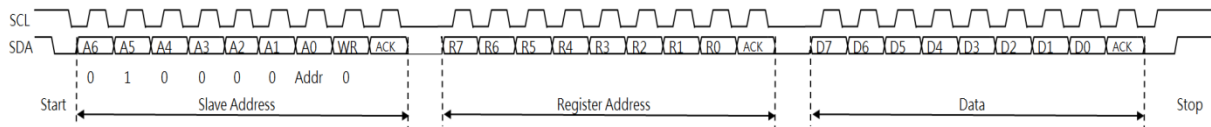


Figure 25. Write Single Byte Data to Register

3. Read Data to Register

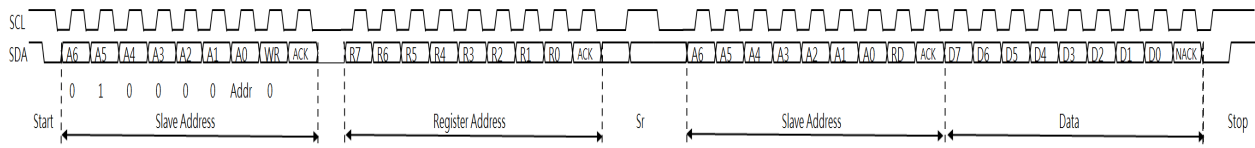


Figure 26. Read Single Byte Data from Register

4. IIC REGISTER MAP



Function	Parameter	Symbol	Address	Range	Resolution	EEPROM Factory Value	BIT(Step)
Channel	Disable Channel Output	Dis_CH	00h	0x00 - 0x3F	--	0x00	6bits
Boost	Boost Output Voltage	BST_O	01h	0x00 - 0x3F (13.5V - 19.8V)	0.1V	0x21 (16.8V)	6bits (64 Steps)
	HVS Voltage	BST_HVS	02h	0x00 - 0x0F (0V - 3V)	0.2V	0x08 (1.6V)	4bits (16 Steps)
	Current Limit	BST_ILIM	03h	0x00 - 0x07 (0A - 2.8A)	0.4A	0x04 (1.6A)	3bits (8 Steps)
	Soft Start Time	BST_SST	04h	0x00 - 0x01 (10ms - 20ms)	10ms	0x00 (10ms)	1bit (2 Steps)
Buck	Buck1 Output Voltage	BKO1	05h	0x00 - 0x0F (2.2V - 3.7V)	0.1V	0x0B (3.3V)	4bits (16 Steps)
	Buck2 Output Voltage	BKO2	06h	0x00 - 0x19 (0.8V - 3.3V)	0.1V	0x04 (1.2V)	5bits (32 Steps)
	Buck3 Output Voltage	BKO3	07h	0x00 - 0x3F (4.8V - 11.1V)	0.1V	0x21 (8.1V)	6bits (64 Steps)
VGH	VGH Output Voltage	VGH_L	08h	0x00 - 0x0F (20V - 35V)	1V	0x08 (28V)	4bits (16 Steps)
	VGH Output Offset	VGH_H	09h	0x00 - 0x0F (0V - 15V)	1V	0x08 (8V)	4bits (16 Steps)
	GPM Stop Level	VGPM	0Ah	0x00 - 0x03 (0V - 15V)	5V	0x03 (15V)	2bits (4 Steps)
VGL	VGL Output Voltage	VGL	0Bh	0x00 - 0x0F (-5.5V - -14.5V)	0.6V	0x08 (-10.3V)	4bits (16 Steps)
Memory	Write Remain Time	MRT	FEh	0x0F (Fixed)	--	0x0F	4bits
Control	Control Register	Ctrl_Reg	FFh	0x00, 0x01, 0x80	--	0x00	8bits



Application Information (Continued)

Set Channel Output (Register Address – 00h)

Disable Channel Output							
REG ADDR 00h	Default Value: Dis_CH = 0x00. All Channel Enable.						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	BK2	BK3	VGH	VGL	VGHM	NTC

Disable Channel Output	
Register	Bit Description
0	Enable Channel Output
1	Disable Channel Output

Set Boost Output Voltage (Register Address – 01h)

Boost Output Voltage							
REG ADDR 01h	Default Value: BST_O = 0x21. AVDD = 16.8V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	BST_O [5]	BST_O [4]	BST_O [3]	BST_O [2]	BST_O [1]	BST_O [0]

BST_O [5:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
000000	13.5	010000	15.1	100000	16.7	110000	18.3
000001	13.6	010001	15.2	100001	16.8	110001	18.4
000010	13.7	010010	15.3	100010	16.9	110010	18.5
000011	13.8	010011	15.4	100011	17.0	110011	18.6
000100	13.9	010100	15.5	100100	17.1	110100	18.7
000101	14.0	010101	15.6	100101	17.2	110101	18.8
000110	14.1	010110	15.7	100110	17.3	110110	18.9
000111	14.2	010111	15.8	100111	17.4	110111	19
001000	14.3	011000	15.9	101000	17.5	111000	19.1
001001	14.4	011001	16.0	101001	17.6	111001	19.2
001010	14.5	011010	16.1	101010	17.7	111010	19.3
001011	14.6	011011	16.2	101011	17.8	111011	19.4
001100	14.7	011100	16.3	101100	17.9	111100	19.5
001101	14.8	011101	16.4	101101	18.0	111101	19.6
001110	14.9	011110	16.5	101110	18.1	111110	19.7
001111	15.0	011111	16.6	101111	18.2	111111	19.8

Set Boost HVS Output Voltage (Register Address – 02h)

HVS Voltage							
REG ADDR 02h	Default Value: BST_HVS = 0x08. HVS=1.6V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	BST_HVS [3]	BST_HVS [2]	BST_HVS [1]	BST_HVS [0]

BST_HVS [3:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
0000	0.0	0100	0.8	1000	1.6	1100	2.4
0001	0.2	0101	1	1001	1.8	1101	2.6
0010	0.4	0110	1.2	1010	2.0	1110	2.8
0011	0.6	0111	1.4	1011	2.2	1111	3.0



Application Information (Continued)

Set Boost Current Limit (Register Address – 03h)

Current Limit (Negative Offset)							
REG ADDR 03h	Default Value: BST_ILIM = 0x04H. ILIM = 1.6A						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	BST_ILIM [2]	BST_ILIM [1]	BST_ILIM [0]

BST_ILIM [2:0]							
Register	Current (A)	Register	Current (A)	Register	Current (A)	Register	Current (A)
000	0.0	010	0.8	100	1.6	110	2.4
001	0.4	011	1.2	101	2	111	2.8

Set Boost Soft Start Time (Register Address – 04h)

Soft Start Time (Base on 10ms)							
REG ADDR 04h	Default Value: BST_SFT = 0x00. TSS = 10ms.						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	BST_SST [0]

BST_SST [0]			
Register	Time (ms)	Register	Time (ms)
0	10	1	20

Set BKO1 Output Voltage (Register Address – 05h)

BKO1 Voltage							
REG ADDR 05h	Default Value: BKO1 = 0x0B. VBKO1 = 3.3V.						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	BKO1 [3]	BKO1 [2]	BKO1 [1]	BKO1 [0]

BKO1 [3:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
0000	2.2	0100	2.6	1000	3	1100	3.4
0001	2.3	0101	2.7	1001	3.1	1101	3.5
0010	2.4	0110	2.8	1010	3.2	1110	3.6
0011	2.5	0111	2.9	1011	3.3	1111	3.7



Application Information (Continued)

Set BKO2 Output Voltage (Register Address – 06h)

BKO2 Voltage							
REG ADDR 06h	Default Value: BKO2 = 0x04. VBKO2 = 1.2V.						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	BKO2 [4]	BKO2 [3]	BKO2 [2]	BKO2 [1]	BKO2 [0]

BKO2 [5:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
00000	0.8	01000	1.6	10000	2.4	11000	3.2
00001	0.9	01001	1.7	10001	2.5	11001	3.3
00010	1	01010	1.8	10010	2.6		
00011	1.1	01011	1.9	10011	2.7		
00100	1.2	01100	2	10100	2.8		
00101	1.3	01101	2.1	10101	2.9		
00110	1.4	01110	2.2	10110	3		
00111	1.5	01111	2.3	10111	3.1		

Set BKO3 Output Voltage (Register Address – 07h)

BKO3 Voltage							
REG ADDR 07h	Default Value: BKO3 = 0x21. VBKO3 = 8.1V.						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	BKO3 [5]	BKO3 [4]	BKO3 [3]	BKO3 [2]	BKO3 [1]	BKO3 [0]

BKO3 [5:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
000000	4.8	010000	6.4	100000	8	110000	9.6
000001	4.9	010001	6.5	100001	8.1	110001	9.7
000010	5	010010	6.6	100010	8.2	110010	9.8
000011	5.1	010011	6.7	100011	8.3	110011	9.9
000100	5.2	010100	6.8	100100	8.4	110100	10
000101	5.3	010101	6.9	100101	8.5	110101	10.1
000110	5.4	010110	7	100110	8.6	110110	10.2
000111	5.5	010111	7.1	100111	8.7	110111	10.3
001000	5.6	011000	7.2	101000	8.8	111000	10.4
001001	5.7	011001	7.3	101001	8.9	111001	10.5
001010	5.8	011010	7.4	101010	9	111010	10.6
001011	5.9	011011	7.5	101011	9.1	111011	10.7
001100	6	011100	7.6	101100	9.2	111100	10.8
001101	6.1	011101	7.7	101101	9.3	111101	10.9
001110	6.2	011110	7.8	101110	9.4	111110	11
001111	6.3	011111	7.9	101111	9.5	111111	11.1



Application Information (Continued)

Set VGH Low Level Output Voltage (Register Address – 08h)

VGH_L Voltage							
REG ADDR 08h	Default Value: VGH_L = 0x08. VGH_L=28V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	VGH_L [3]	VGH_L [2]	VGH_L [1]	VGH_L [0]

VGH_L [3:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
0000	20	0100	24	1000	28	1100	32
0001	21	0101	25	1001	29	1101	33
0010	22	0110	26	1010	30	1110	34
0011	23	0111	27	1011	31	1111	35

Set VGH_H Output Voltage (Register Address – 09h)

VGH High Level Offset Voltage							
REG ADDR 09h	Default Value: VGH_L = 0x08. VGH_H = 8V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	VGH_H [3]	VGH_H [2]	VGH_H [1]	VGH_H [0]

VGH_H [3:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
0000	0	0100	4	1000	8	1100	12
0001	1	0101	5	1001	9	1101	13
0010	2	0110	6	1010	10	1110	14
0011	3	0111	7	1011	11	1111	15

Set GPM Stop Level Voltage (Register Address – 0Ah)

VGPM Voltage							
REG ADDR: 0Ah	Default Value: VGHM = 0x03. VGPM = 15V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	VGPM [1]	VGPM [0]

VGPM [1:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
00	0	01	5	10	10	11	15



Application Information (Continued)

Set VGL Output Voltage (Register Address – 0Bh)

VGL Voltage							
REG ADDR: 0Bh	Default Value: VGL = 0x08. VGL = -10.3V						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	VGL [3]	VGL [2]	VGL [1]	VGL [0]

VGL [3:0]							
Register	Volt (V)	Register	Volt (V)	Register	Volt (V)	Register	Volt (V)
0000	-5.5	0100	-7.9	1000	-10.3	1100	-12.7
0001	-6.1	0101	-8.5	1001	-10.9	1101	-13.3
0010	-6.7	0110	-9.1	1010	-11.5	1110	-13.9
0011	-7.3	0111	-9.7	1011	-12.1	1111	-14.5

Control Register Function (Register Address – FFh)

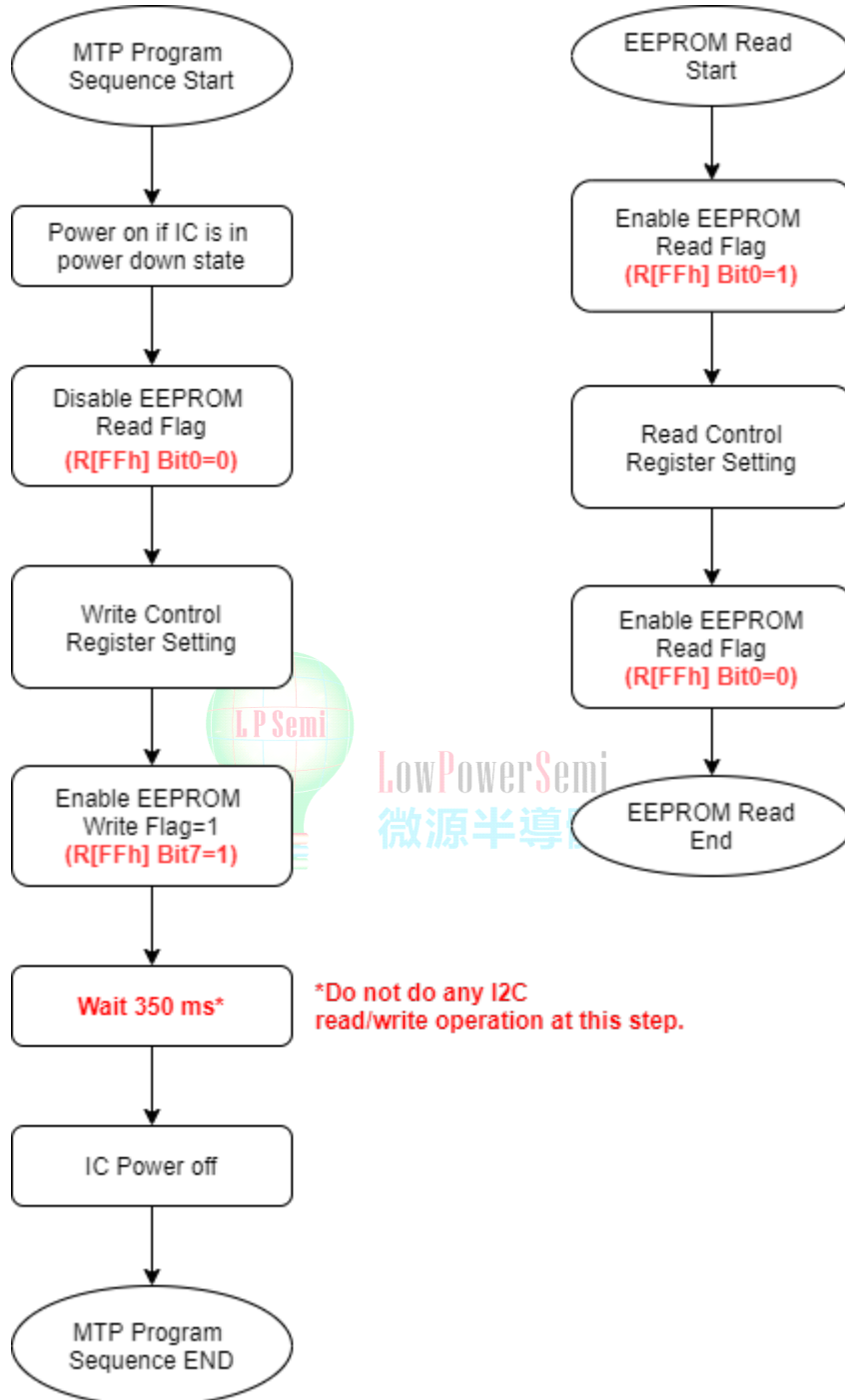
Control Function Select							
REG ADDR: FFh	Default Value: Ctrl = 0x00. Read data from DAC register.						
D7	D6	D5	D4	D3	D2	D1	D0
W	R	R	R	R	R	R	R/W
Ctrl [7]	0	0	0	0	0	0	Ctrl [0]

Write Data to EEPROM Function Ctrl [7]	
Register	Bit Description
0	Read back value.
1	Write register value to EEPROM.

Read Data from Register or EEPROM Select Ctrl [0]	
Register	Bit Description
0	Read data from register.
1	Read data from EEPROM.



5. IIC Programming Flow Chart





Application Information (Continued)

Layout Guideline

The proper PCB layout and component placement are critical for all circuit. The careful attention should be preventing electromagnetic interference (EMI) problems. Here are some suggestions to the layout of LP6288 design.

1. Connected all ground together with one uninterrupted ground plane, which include power ground and analog ground.
2. The input capacitor should be located as closed as possible to the VIN and ground plane.
3. Minimize the distance of all traces that connected to all LX nodes. Shorten the traces length and route width to obtain optimum efficiency.
4. All output capacitor must be closed to ground plane. The ground terminal of COUT must be located as closed as possible to ground plane.
5. The exposed pad of the chip should be connected to ground plane for maximum thermal consideration.

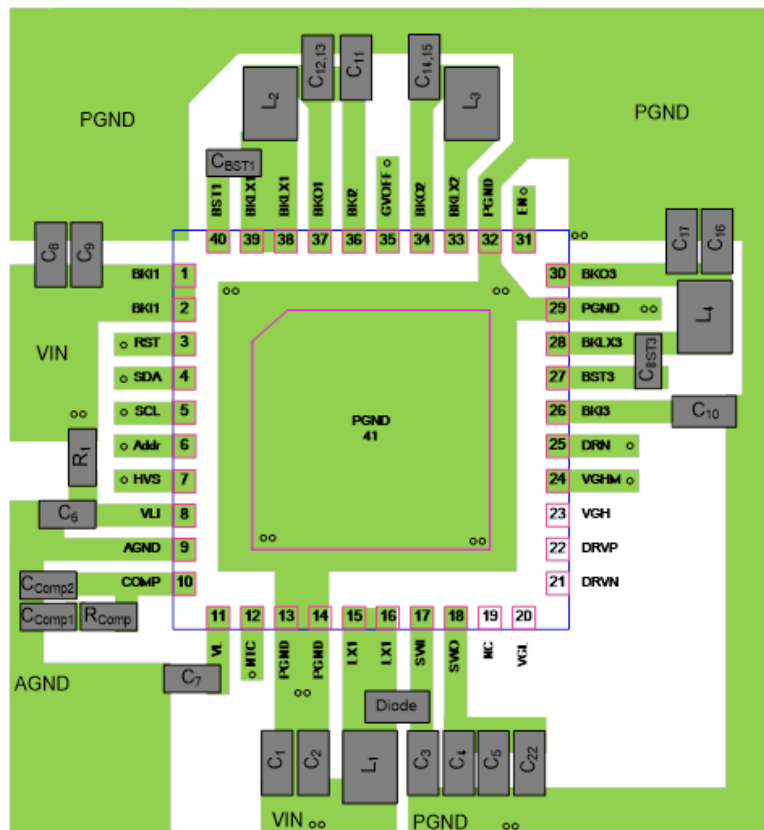
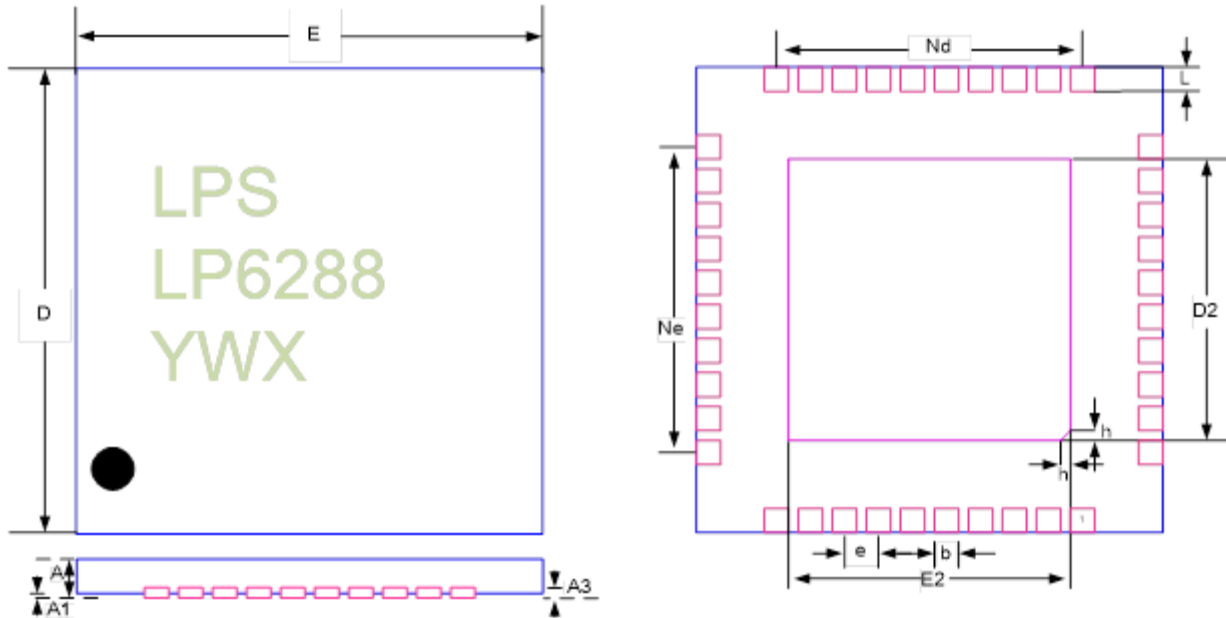


Figure 22. Recommended PCB Layout Diagram



Package Information

QFN-40 Package (6x6) pitch 0.5 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.180	0.250	0.300
A3	0.180	0.200	0.250
D	5.900	6.000	6.100
D2	4.100	---	4.550
E	5.900	6.000	6.100
E2	4.100	---	4.550
e	0.500 BSC		
Nd	4.500 BSC		
Ne	4.500 BSC		
L	0.300	0.400	0.450
h	0.300	0.350	0.400