LowPowerSemi 微源半导体

# LP4022H

## Compact 2A Sensorless Buck Switching Charger

## Features

- Compact high-efficiency 1-cell switching charger
  - Proprietary sensorless charge current control
  - 4.1V to 6.2V input voltage with 28V absolute maximum input voltage rating
  - Charge voltages: 4.20V / 4.35V
  - 2.0A continuous fast charge current
  - 1.2MHz switching frequency
  - 93.5% high efficiency @ VBAT=4V, ICHG=1A
  - 89% high efficiency @ VBAT=4V, ICHG=2A
  - Input voltage regulation to allow weak input power source to charge battery (VINDPM)
  - Support trickle charge, precharge, Constant Current (CC) charge, Constant Voltage (CV) charge, charge termination and recharge
- High charge accuracy
  - +/- 0.5% charge voltage regulation
  - +/- 10% charge current regulation
- High integration
  - Integrated all MOSFETs
  - Internal loop compensation
  - LED charge indication driver
- Protections
  - Cycle-by-cycle current limit protection
  - Input over-voltage protection (OVP)
  - Cold/hot battery temperature monitoring
  - Junction temperature thermal regulation (TREG)
  - ISET pin short and open protection
- Packaging
  - DFN2x2-8L
  - RoHS compliant and halogen free
  - 100% lead (Pb) free

## Applications

- IoT devices
- Wearable devices
- Gaming devices
- Portable electronics
- E-Cigarette

## General Description

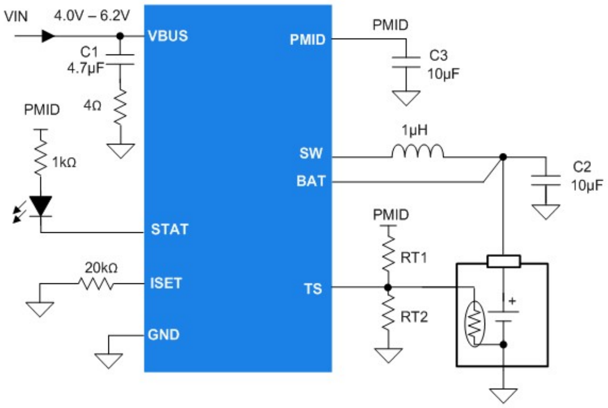
The LP4022H is a standalone 1-cell switching battery charger that delivers up to 2A of charge current from a 4.1V to 6.2V input voltage. The charge current is programmable via a resistor connected between the ISET pin and GND. Charging can be enabled or disabled through the ISET pin or TS pin. Operating at a 1.2MHz switching frequency, the LP4022H supports the use of a compact 2.0 × 1.6 mm, 1-μH inductor for fast 2A charging. LPS's patented integrated current sensing and control technology eliminates the need for an external sensing resistor, enabling high charge efficiency, low BOM cost, and a small form factor. The LP4022H is offered in a DFN2×2-8L package, providing one of the most compact switching charging solutions available on the market, ideal for space-constrained systems.

## Order Information

LP4022H □□ □ □□□

Battery Voltage
F: Pb-Free
Package Type
QV: DFN -8

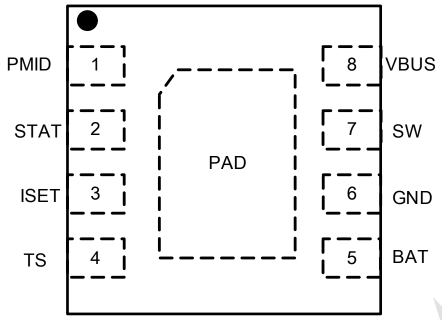
## Application Circuit



## Device Information

| Part Number | Battery Voltages | Top Marking | Package | Moisture Sensitivity Level | Shipping |
|---|---|---|---|---|---|
| LP4022HQVF | 4.2V | LPS<br>BpYWX | DFN2x2-8 | MSL3 | 4K/REEL |
| LP4022HQVF-435 | 4.35V | LPS<br>BQYWX | DFN2x2-8 | MSL3 | 4K/REEL |
| Marking indication: Y: Year code. W: Week code. X: Batch numbers.<br>MSL: Moisture Sensitivity Level according to JEDEC Standard | | | | | |

## Pin Diagram



DFN 2x2 – 8L
(Top View)

## Pin Description

| Pin Name | Pin Number | **Description** |
|---|---|---|
| PMID | 1 | Output of the source of over voltage protection N-channel MOSFET (OVPFET) and the source of high-side P-channel MOSFET (HSFET). Place ceramic 10μF on PMID to GND and place it as close as possible to IC. PMID voltage is clamped once VBUS over voltage is detected. |
| STAT | 2 | Charge status indication output. Connect a LED from PMID pin to STAT pin via a current limiting resistor. The STAT pin indicates charger status:<br>Charge in progress: STAT pin is pulled LOW<br>Charge complete or charger in SLEEP mode: STAT pin is OPEN |
| ISET | 3 | Charge current program input. Connect a 1% resistor RISET from this pin to ground to program the charge current. If ISET pin is floating, charge current is minimized. If ISET pin is pulled higher than 1V or below 0.35V, charge is disabled. ISET can be used to enable and disable charge. |
| TS | 4 | Battery temperature sense thermistor input. Charge is suspended if the battery thermistor temperature is out of range. Leave the TS pin floating if TS pin function is not used. |
| BAT | 5 | Battery connection pin. Connect this pin to node of inductor output terminal and battery pack positive terminal. ≥10uF capacitor is recommended to connect to this node. |
| GND | 6 | Power ground and analog ground. |
| SW | 7 | Switching node. Internally SW node is connected to the source of the P-channel HSFET and the drain of the N-channel LSFET. Connect this pin to a terminal of external inductor. |
| VBUS | 8 | Charger input connection. The internal over voltage protection N-channel MOSFET (OVPFET) is connected between VBUS and PMID with VBUS on drain. Place a 4.7uF or higher ceramic capacitor from VBUS to GND and place it as close as possible to the device. |
| PAD | 9 | Thermal pad. Connected to GND on top layer and connected to ground plane by multiple vias for heat dissipation. |

## Absolute Maximum Ratings (1)

VBUS voltage to GND---------------------------------------- -0.3V to 28V
PMID, SW Voltage to GND ----------------------------------------0.3V to 7V
BAT Voltage to GND ----------------------------------------0.3V to 6V (2)
STAT, ISET, TS Voltages to GND ----------------------------------------0.3V to 6V
STAT Sink Current---------------------------------------- 6mA
Maximum Junction Temperature (Tj)---------------------------------------- 150℃
Storage Temperature Range-----------------------------------------40℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec)---------------------------------------- 260℃

**Note1**: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: Surge protection is internally built in at BAT pin to stand voltage surge at this pin.

## ESD Ratings

HBM (Human Body Model) ---------------------------------------- 2kV
MM (Machine Model)----------------------------------------200V
CDM (Charge Discharge Model) ---------------------------------------- 500V

## Thermal Information

$\theta_{JA}$ (Junction-to-Ambient Thermal Resistance) ----------------------------------------50℃/W

## Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | 4.1 | | 6.2 | V |
| $I_{CHG}$ | Fast Charge Current | 0.35 | | 2.0 | A |
| $V_{BAT}$ | Battery Charge Voltage | | 4.2 / 4.35 | | V |
| $T_J$ | Operating Junction Temperature Range ($T_J$) | -40 | | 125 | ℃ |
| $T_A$ | Ambient Temperature Range | -40 | | 85 | ℃ |
| L | Output Inductance | 0.7 | 1 | 2.64 | μH |
| $C_{IN}$ | Input Capacitance at VBUS | 1.4 | 4.7 | | μF |
| $C_{PMID}$ | PMID Capacitance | 3 | 10 | | μF |
| $C_{BAT}$ | BAT Capacitance | 3 | 10 | | μF |

**Notes:**

(1) The values recommended in the table are effective inductance and capacitance.

(2)

## Electrical Characteristics

(The (The specifications are at $V_{VBUS\_LOWV}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$ and $V_{VBUS}$ > $V_{BAT}$ + $V_{SLEEP}$, L=1uH, $T_J$ = 25°C unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| QUIESCENT CURRENT | | | | | | |
| $I_{Q\_BAT}$ | Battery reverse current | VBAT= VSW = 4.35V,<br>VBUS pin is floating | | | 1 | μA |
| $I_{Q\_BAT}$ | Battery leak current | Charge is terminated,<br>$V_{BAT}$=4.35V | | | 5 | μA |
| $I_{Q\_BAT}$ | Battery leak current | ISET pin short to GND,<br>VBAT=4.35V | | | 5 | μA |
| OVER VOLTAGE PROTECTION | | | | | | |
| $V_{VBUS\_OVP\_RISE}$ | VBUS input overvoltage threshold | $V_{VVBUS}$ rising | 6.2 | 6.4 | 6.6 | V |
| $V_{VVBUS\_OVP\_HYS}$ | VBUS input overvoltage threshold hysteresis | $V_{VVBUS}$ falling | | 0.5 | | V |
| $V_{PMID\_CLAMP}$ | PMID voltage | PMID voltage at $V_{VBUS}$=12V | | 5 | | V |
| MOSFETS | | | | | | |
| $R_{DSON\_Q1}$ | OVPFET on-resistance | $V_{VVBUS}$=5V | | 75 | | mΩ |
| $R_{DSON\_Q2}$ | HSFET on-resistance | $V_{VVBUS}$=5V | | 80 | | mΩ |
| $R_{DSON\_Q3}$ | LSFET on-resistance | $V_{VVBUS}$=5V | | 180 | | mΩ |
| INPUT VOLTAGE | | | | | | |
| $V_{VBUS}$ | VBUS operation range | | 4.1 | | 6.2 | V |
| $V_{UVLO\_RISE}$ | Under voltage lock out(UVLO) voltage | $V_{VBUS}$ rising | 3.65 | 3.75 | 3.85 | V |
| $V_{UVLO\_FALL}$ | UVLO voltage | $V_{VBUS}$ falling | | 300 | | mV |
| $V_{SLEEP}$ | Into sleep mode threshold | $V_{VBUS}$ falling, $V_{BAT}$ - $V_{VBUS}$ | 30 | 60 | 90 | mV |
| $V_{SLEEPZ}$ | Exit sleep mode threshold | $V_{VBUS}$ rising, $V_{VBUS}$-$V_{BAT}$ | 140 | 180 | 230 | mV |
| $V_{INDPM\_MIN}$ | Minimum VINDPM at VBUS | $V_{BAT}$=3.5V<br>Regulated at VBUS pin | 3.9 | 4.0 | 4.1 | V |
| ISET Pin | | | | | | |
| $V_{ISET}$ | ISET pin voltage | | 0.985 | 1 | 1.015 | V |
| $K_{ICHG}$ | Charge current ratio | $R_{ISET}$ = 23.2kΩ, 40.2kΩ<br>ICHG=$K_{ICHG}$/$R_{ISET}$ | 10% | 40 | 10% | AxkΩ |
| $K_{ICHG}$ | Charge current ratio | $R_{ISET}$ = 78.7kΩ<br>ICHG=$K_{ICHG}$/$R_{ISET}$ | 15% | 40 | 15% | AxkΩ |
| $V_{ISET\_LOW}$ | ISET voltage low | | | 0.35 | | V |

## Electrical Characteristics

(The specifications are at $V_{VBUS\_LOWV}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$ and $V_{VBUS}$ > $V_{BAT}$ + $V_{SLEEP}$, L=1uH, $T_J$ = 25°C unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BATTERY CHARGER** | | | | | | |
| $V_{BATREG}$ | Charge voltage | CV regulation voltage at BAT pin | 4.179 | 4.2 | 4.221 | V |
| | | | 4.328 | 4.35 | 4.372 | V |
| $I_{CHG}$ | Fast charge current | $I_{CHG}$=2A, $V_{VBUS}$=5V, $V_{BAT}$=3.8V<br>$R_{ISET}$=20kΩ | 1800 | 2000 | 2200 | mA |
| $I_{CHG}$ | Fast charge current | $I_{CHG}$=1A, $V_{VBUS}$=5V, $V_{BAT}$=3.8V<br>$R_{ISET}$=40kΩ | 900 | 1000 | 1100 | mA |
| $I_{PRECHG}$ | Precharge current | $I_{CHG}$=2A, $V_{VBUS}$=5V, $V_{BAT}$=2.5V<br>$R_{ISET}$=20kΩ | 140 | 200 | 260 | mA |
| $I_{PRECHG}$ | Precharge current | $I_{CHG}$=1A, $V_{VBUS}$=5V, $V_{BAT}$=2.5V<br>$R_{ISET}$=40kΩ | 50 | 100 | 150 | mA |
| $I_{BAT\_SHORT}$ | Trickle charge current | $V_{VBUS}$=5V, $V_{BAT}$=1.0V | 45 | 60 | 75 | mA |
| $I_{TERM}$ | Termination current | $I_{CHG}$=2A, $V_{BATREG}$=4.2V<br>$R_{ISET}$=20kΩ | 140 | 200 | 260 | mA |
| $I_{TERM}$ | Termination current | $I_{CHG}$=1A, $V_{BATREG}$=4.2V<br>$R_{ISET}$=40kΩ | 50 | 100 | 150 | mA |
| $V_{BAT\_SHORT\_RISE}$ | $V_{BAT}$ short rising threshold | From battery short to precharge | 1.85 | 2.00 | 2.15 | V |
| $V_{BAT\_SHORT\_FALL}$ | $V_{BAT}$ short falling threshold | From precharge to battery short | 1.65 | 1.80 | 1.95 | V |
| $V_{BAT\_LOWV\_RISE}$ | $V_{BAT}$ fast charge rising threshold | Precharge to fast charge | 2.9 | 3.0 | 3.1 | V |
| $V_{BAT\_LOWV\_FALL}$ | $V_{BAT}$ fast charge falling threshold | Fast charge to precharge charge | 2.6 | 2.7 | 2.8 | V |
| $V_{RECHG\_HYS}$ | Recharge threshold | $V_{BAT}$ falling | 120 | 150 | 180 | mV |
| **STAT** | | | | | | |
| $I_{STAT\_PD}$ | STAT pull-down current | | | | 6 | mA |

## Electrical Characteristics

(The specifications are at $V_{VBUS\_LOWV}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$ and $V_{VBUS}$ > $V_{BAT}$ + $V_{SLEEP}$, L=1uH, $T_J$ = 25°C unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SWITCHING CONVERTER | | | | | | |
| $F_{SW}$ | Switching Frequency | | | 1210 | | kHz |
| $I_{HSFET\_OCP}$ | HSFET Over Current Protection | | | 3.3 | | A |
| $D_{MAX}$ | Maximum duty cycle | | | | 100 | % |
| COLD/HOT THERMISTOR COMPARATOR | | | | | | |
| $V_{T1}$% | $T_{COLD}$ (0°C) threshold, charge suspend if $V_{TS}$ is above the threshold | $V_{TS}$ rising, as percentage of $V_{PMID}$ | 73 | 73.5 | 74 | % |
| $V_{T1}$% | | $V_{TS}$ falling, as percentage of $V_{PMID}$ | | 71.5 | | % |
| $V_{T3}$% | $T_{HOT}$ (45°C) threshold, charge suspend if $V_{TS}$ is below the threshold | $V_{TS}$ falling, as percentage of $V_{PMID}$ | 47 | 47.25 | 47.5 | % |
| $V_{T3}$% | | $V_{TS}$ rising, as percentage of $V_{PMID}$ | | 48.25 | | % |
| THERMAL REGULATION AND THERMAL SHUTDOWN | | | | | | |
| $T_{REG}$ | Thermal regulation | | | 130 | | °C |
| $T_{SHUT\_RISE}$ | Thermal shut down | Temperature rise | | 150 | | °C |
| $T_{SHUT\_FALL}$ | Thermal shut down | Temperature fall | | 120 | | °C |

## Typical Characteristics

(L=1μH, CPMID=10μF, CIN= 2.2μF and $T_J$ = 25°C unless otherwise noted)

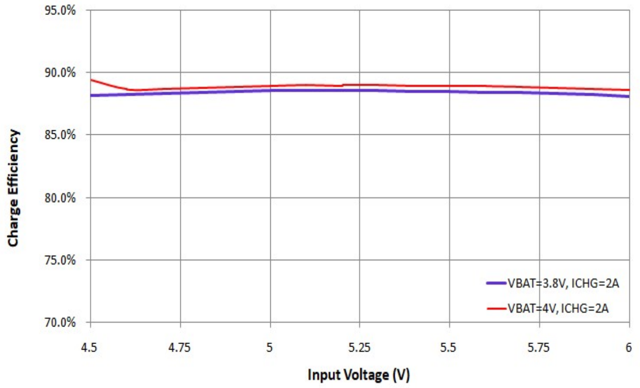


Figure 1. Charge Efficiency vs. Vin

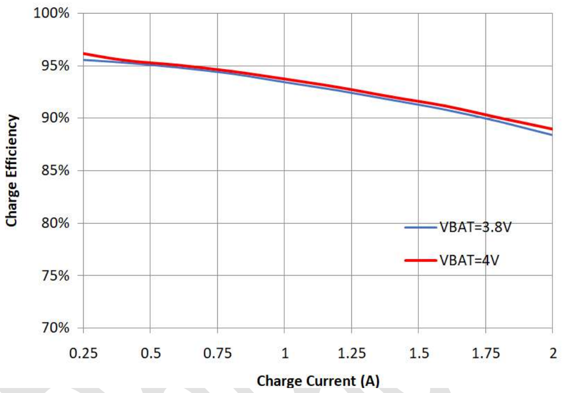


Figure 2. Charge Efficiency vs. Charge Current ($V_{IN}$=5V)

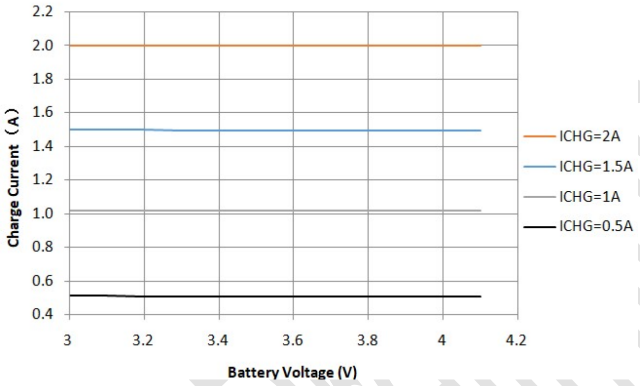


Figure 3. Charge Current vs. Battery Voltage

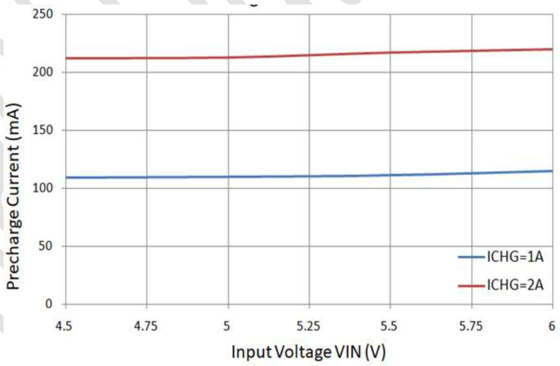


Figure 4. Precharge current vs. Input Voltage

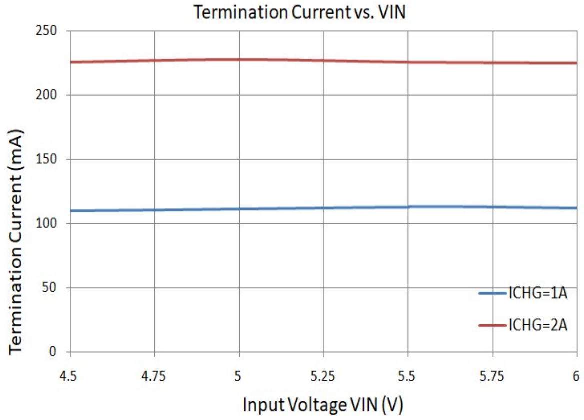


Figure 5. Termination Current vs. Input Voltage

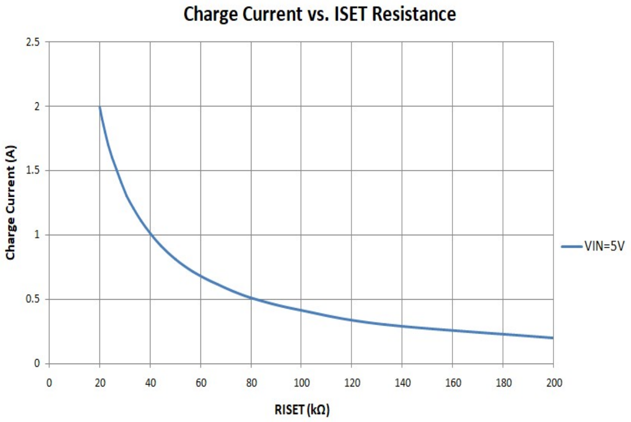
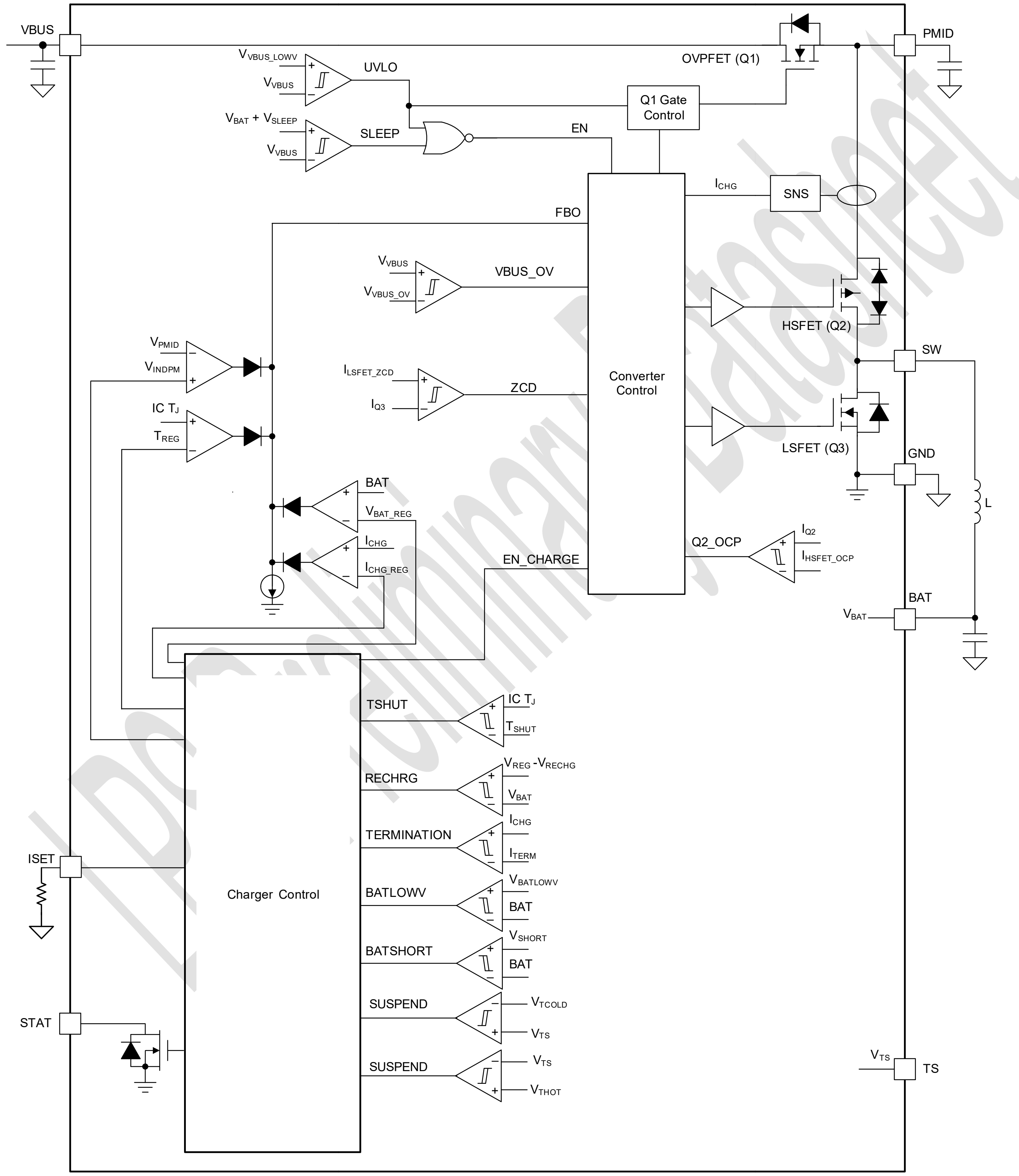


Figure 6. Charge Current vs. $R_{ISET}$

## Functional Block Diagram



# Detailed Description

## Input Over Voltage Protection (OVP)

The LP4022H comprises of input over voltage protection followed by a Buck charger. During power-up from VBUS, OVPFET soft-start after $V_{VBUS}$ reaches UVLO threshold $V_{UVLO\_RISE}$ for a delay time. Following the OVPFET soft-start, charger is enabled if charge mode condition is met. If the input voltage $V_{VBUS}$ exceeds the OVP threshold, the P-channel OVPFET gate voltage is pulled to a reference voltage such that PMID voltage is clamped at $V_{PMID\_CLAMP}$. Buck charger is connected between PMID and a battery.

## Charger Power-up

If ISET pin is not shorted, internal LDO successful power-up, if there is no faults detected, the device powers up and charge is enabled. The faults include:

- Input OVP fault: $V_{VBUS} > V_{VBUS\_OVP}$
- TS cold/hot fault
- Junction temperature is above $T_{SHUT}$

## Device Functional Mode

The device operates in different modes depending on VBUS voltage, battery voltage and ISET pin connection. The functional modes are listed in the following table.

Table 1: Device Functional Mode

| MODE | CONDITIONS | CHARGE | STAT |
|---|---|---|---|
| ISET Pin High | ISET pin open or pulled higher than 1V | NO | PULLED LOW |
| ISET Pin Short | ISET pin is shorted to GND | NO | OPEN |
| HiZ Mode | $V_{VBUS} < V_{UVLO}$ | NO | OPEN |
| Sleep Mode | $V_{VBUS} > V_{UVLO}$<br>$V_{VBUS} < V_{BAT} + V_{SLEEP\_Z}$ | NO | OPEN |
| Charge Mode | $V_{VBUS} > V_{UVLO}$<br>$V_{VBUS} > V_{BAT} + V_{SLEEP\_Z}$<br>$V_{VBUS} < V_{VBUS\_OVP\_RISE}$ | YES | PULLED LOW |
| Charge Termination Mode | $V_{VBUS} > V_{UVLO}$<br>$V_{VBUS} > V_{BAT} + V_{SLEEP\_Z}$<br>$V_{VBUS} < V_{VBUS\_OVP}$<br>No faults and charge is terminated | NO | OPEN |
| Fault Mode | • Input OVP<br>• TS Cold/Hot<br>• Thermal Shutdown | NO | OPEN |

## Battery Charge Profile

In Charge Mode as shown in the table of Device Functional Mode, the devices charge the battery in four sub-charge-modes: trickle charge, pre-charge, Constant Current (CC) charge and Constant Voltage (CV) charge as shown in Figure 7. If the battery voltage falls below $V_{BAT\_SHORT\_FALL}$, the battery charge battery with trickle charge current $I_{BAT\_SHORT}$, when the battery voltage rises above $V_{BAT\_SHORT\_RISE}$ and below $V_{BAT\_LOWV\_RISE}$, the charger charges battery in precharge mode with charge current at $I_{PRECHG}$. Fast charge starts once battery voltage rises above $V_{BAT\_LOWV\_RISE}$. When battery voltage is close to battery charge voltage $V_{BATREG}$, the charger goes into CV mode and charge current starts to decreases. When charge current decreases below termination current $I_{TERM}$, charge is terminated and charge cycle ends. Following charge termination, if the battery voltage follows below ($V_{BATREG}$ – $V_{RECHG\_HYS}$), a new charge cycle restarts.

## Trickle Charge

Under battery short condition, the device charges the battery at a fixed charge current $I_{BAT\_SHORT}$ if the battery is below $V_{BAT} < V_{BAT\_SHORT}$. VINDPM and thermal regulation is enabled during trickle charge.

## Precharge

The device charges the battery at 10% of programmed fast charge current $I_{CHG}$ in precharge mode. Precharge is enabled in charge mode when the precharge condition $V_{BAT\_SHORT\_RISE} < V_{BAT} < V_{BAT\_LOWV\_RISE}$ is met.

## Constant Current (CC) Charge

CC charge is also called fast charge. The device charges the battery from Buck converter at current level of $K_{ICHG}$ / $R_{ISET}$, where $K_{ICHG}$ is the gain of charge current setting.

## Constant Voltage (CV) Charge

With the battery voltage charged up, the BAT pin voltage reaches the battery regulation voltage $V_{BATREG}$ and the charge current starts to decrease from fast charge current $I_{CHG}$. The actual battery voltage keeps increasing until charge termination is triggered.

## Charge Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold ($V_{BATREG}$ - $V_{RECHG\_HYS}$) and the charge current is below termination current $I_{TERM}$ for deglitch time $t_{TERM}$. The termination current threshold $I_{TERM}$ is 10% of fast charge current $I_{CHG}$, which is set by the RISET resistor connected at ISET pin.

## Battery Recharge

Once a charge cycle is terminated, if battery voltage $V_{BAT}$ decreases below the recharge threshold ($V_{BATREG}$ - $V_{RECHG\_HYS}$) and the charge mode conditions are met, the charger is enabled again. In addition to recharge, charge cycle starts if $V_{VBUS}$ voltage is recycled or fault conditions are cleared or ISET pin is released from a short condition even with the battery voltage above the recharge threshold.

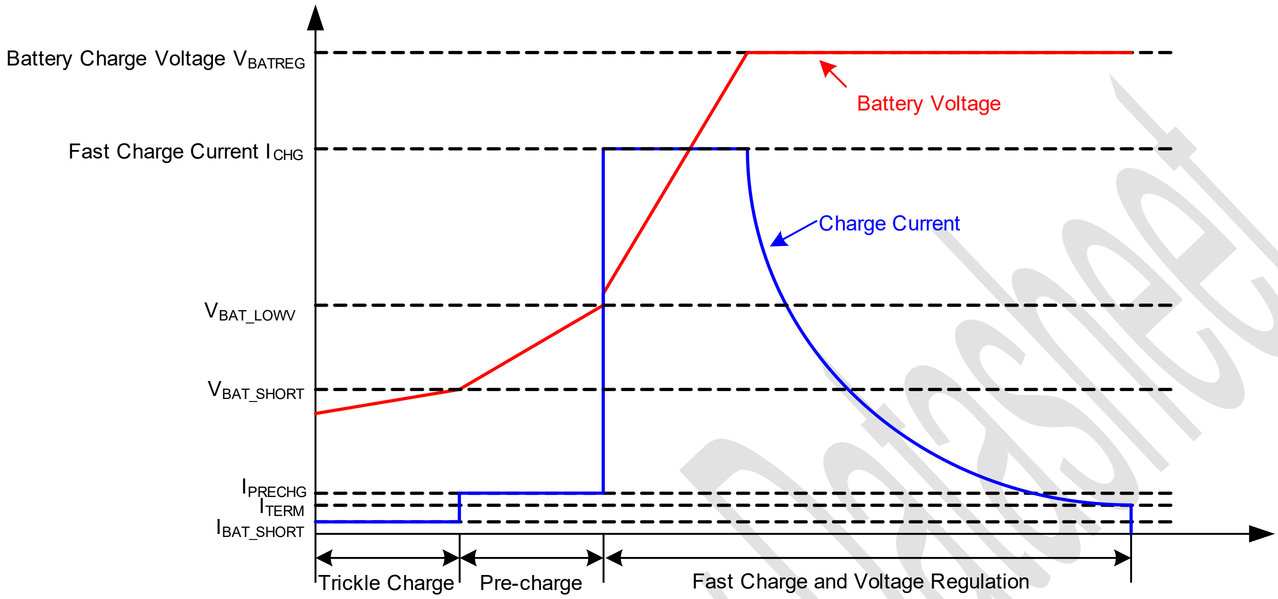


Figure 7. Battery Charge Profile

Table 2. Charge Current in Charge Mode

| CHARGE MODE | BATTERY VOLAGE $V_{BAT}$ | CHARGE CURRENT | TYPICAL VALUES |
|---|---|---|---|
| Trickle Charge | $V_{BAT} < V_{BAT\_SHORT\_FALL}$ | $I_{BAT\_SHORT}$ | 60mA |
| Precharge | $V_{BAT\_SHORT\_RISE} < V_{BAT} < V_{BAT\_LOWV}$ | $I_{PRECHG}$ | 10% of $I_{CHG}$ |
| Fast Charge | $V_{BAT\_LOWV} < V_{BAT} < V_{BATREG}$ | $I_{CHG}$ | $K_{ICHG} / R_{ISET}$ |
| CV Charge | $V_{BAT\_LOWV} < V_{BAT} < V_{BATREG}$ | $< I_{CHG}$ | Variable |

## Battery Temperature Monitoring

The charger device provides a single NTC thermistor input TS pin for battery temperature monitor. RT1 and RT2 resistor programs the cold temperature T1 and hot temperature T3. In the Equations (1) and (2), RNTC,T1 is NTC thermistor resistance value at temperature T1 and RNTC,T3 is NTC thermistor resistance values at temperature T3. VT1% and VT3% can be found n the Electronic Characteristics table. Select 0°C to 45°C for battery charge temperature range, then NTC thermistor 103AT-2 resistance are RNTC,T1 = 27.28 kΩ ( at 0°C) and RNTC,T3 = 4.91 kΩ (at 45°C). From Equation (1) and Equation (2), RT1 and RT2 are derived as below, which is the resistance to set the charge temperature range 0 to 45°C.

- RT1 = 4.52 kΩ
- RT2 = 23.2 kΩ

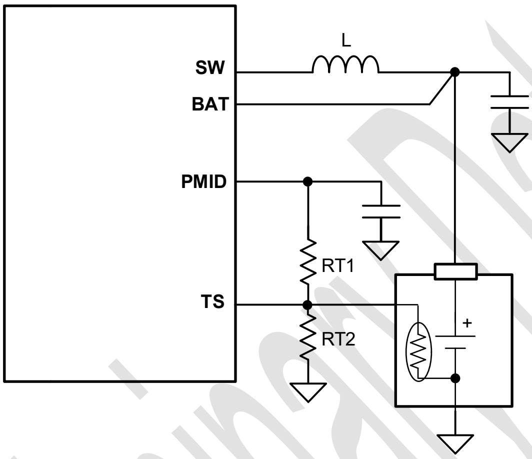


Figure 8. Battery Temperature Monitoring

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{V_{T3\%}} - \frac{1}{V_{T1\%}}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1\%}} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{V_{T3\%}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1\%}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

If TS is open, TS function is disabled. If TS function is not used, just leave TS pin open.

## Fault Mode

Any fault below triggers the charger into fault mode:

- Input OVP
- TS Cold/Hot
- Thermal Shutdown

In fault mode, the device stops charging. Once a fault is cleared, the charger goes back to charge mode if charge conditions are met.

## ISET Pin

If ISET pin is open or pulled above higher than 1V, the charge current is near zero. If the ISET pin is pulled below 0.35V, the charge is disabled and STAT pin is open. ISET pin can be used as enable/disable input for charge current by pulling up or down ISET pin.

## Input Voltage Dynamic Power Management (VINDPM)

When the input current of the device exceeds the current capability of the power supply, the charger device regulates VBUS voltage by reducing charge current to avoid crashing the input power supply. To charge a battery, the input voltage must be higher than actual $V_{INDPM}$ threshold. In VINDPM regulation, termination is temporarily disabled.

## Maximum Duty Cycle Dmax and 100% Duty Cycle

The Buck converter implemented HSFET maximum duty cycle and 100% duty cycle. When a weak input source(due to long input cable or lower power level of an adaptor) is connected at VBUS, the HSFET duty cycle increases, If Dmax is reached and the closed-loop regulation still cannot regulate current or voltage, then HSFET turns on with 100% duty cycle. By implementing 100% duty cycle, the Buck converter operates in pass-though mode and charge current is maximized and efficiency jumps to higher level.

## Thermal Regulation (TREG)

The device monitors the junction temperature $T_J$ to avoid overheating the chip and limit the device surface temperature. When the internal junction temperature exceeds thermal regulation limit $T_{REG}$, the device lowers down the charge current. During thermal regulation, the average charging current is reduced below the programmed battery charging current. In thermal regulation, termination is temporarily disabled.

## Thermal Shutdown (TSHUT)

The devices have thermal shutdown built in to turn off the charger when device junction temperature exceeds $T_{SHUT}$. The charger is re-enabled when the junction temperature is 25°C below $T_{SHUT}$. During thermal shutdown, charge is suspended and the charger goes into fault mode.

# Application and Implementation

## Application Information

The device can be used for general purpose high efficiency fast charger. The charge current is programmable by a resistor from ISET pin to GND. The charge can be enabled or disabled by a MCU GPIO connected to ISET pin or TS pin as shown in Figure 9 and Figure 10.

## Application Schematic

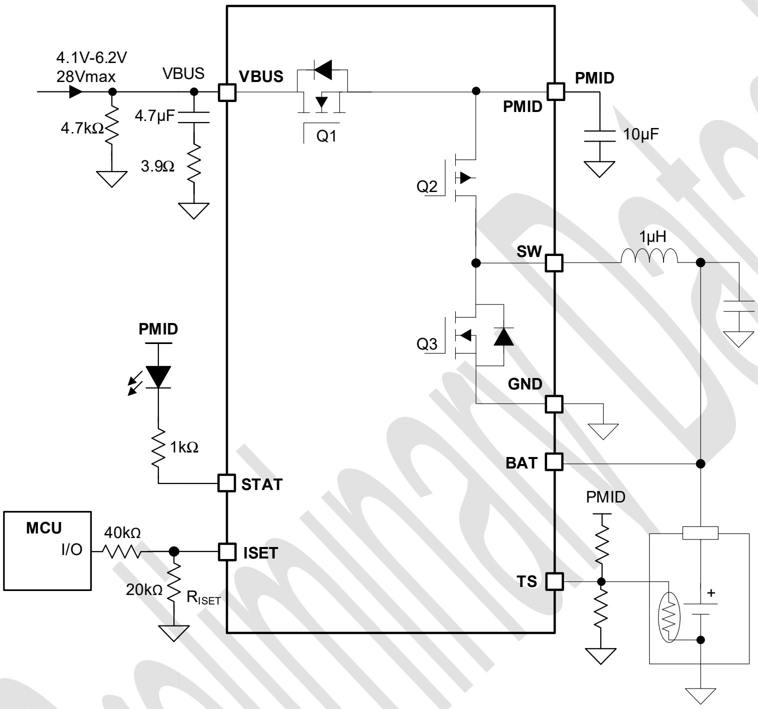


Figure 9: Typical Applications Schematic
(MCU enable/disable charge with ISET pin pulled high)

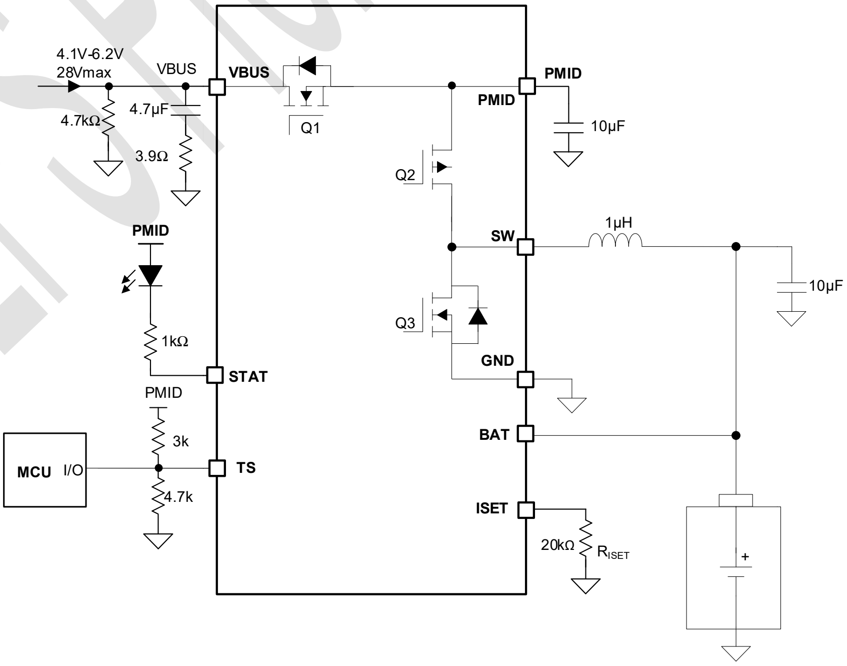


Figure 10: Typical Applications Schematic
(MCU enable/disable charge with TS pin pulled low)

## Charge Current Setting

The charger current is set by the resistor value at the ISET pin according to the equation below:

$$I_{CHG}\ (A) = K_{ICHG}\ (A{\cdot}k\Omega)\ /\ R_{ISET}(k\Omega) \qquad (3)$$

$K_{ICHG}$ is current setting gain that is listed in Electrical Characteristics table and $R_{ISET}$ is the resistor value from ISET pin to GND. $K_{ICHG}$ is typically 40 (A·kΩ).

## Input Hot Plug-In

To attenuate potential input voltage spike caused by cable parasitic inductance during adaptor hot plug-in, there is a 3.9Ω resistor is in series with the 4.7μF input capacitor. 4.7kΩ is used to discharge the input capacitor in case there is contact bounce.

## Application Curves

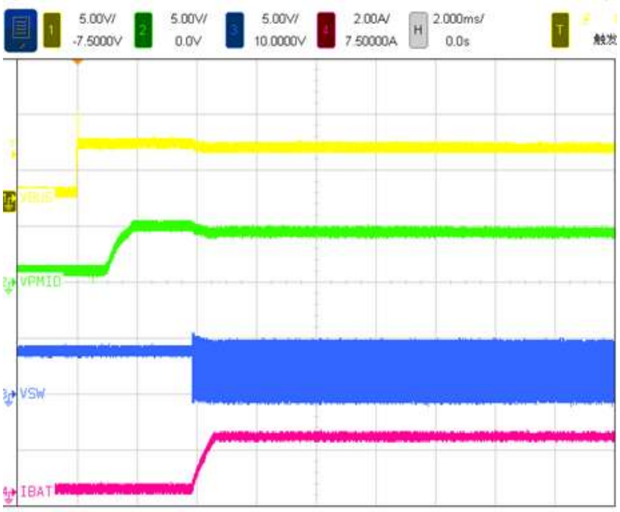


Figure 11. Power-up from VBUS
($V_{VBUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

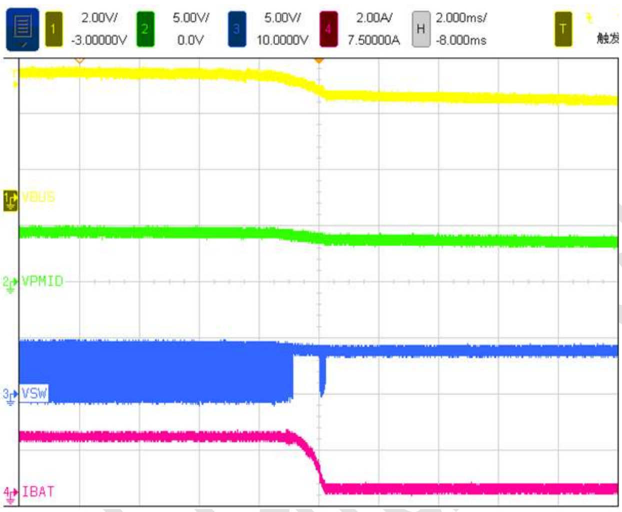


Figure 12. Power-down from VBUS
($V_{VBUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

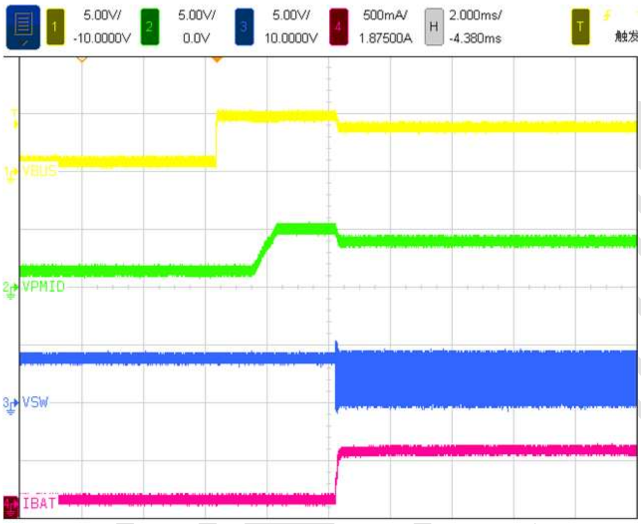


Figure 13. Power-up into VINDPM
($V_{VBUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

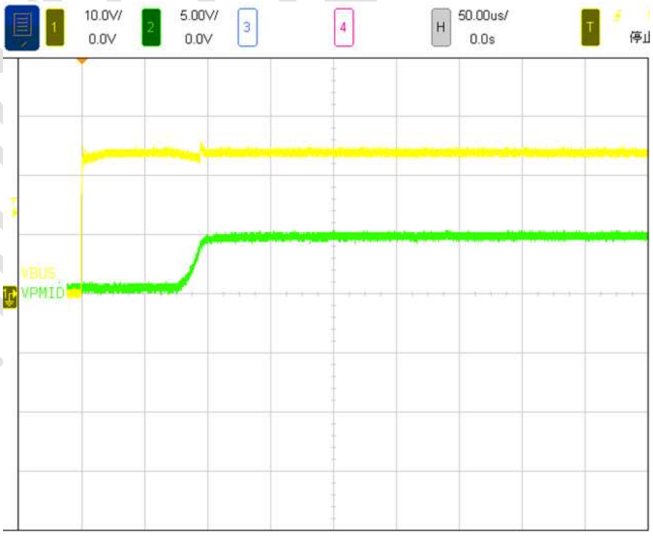


Figure 14. VBUS hot plug-in
($V_{VBUS}$=24V, $V_{BAT}$=3.8V, $I_{CHG}$=2A

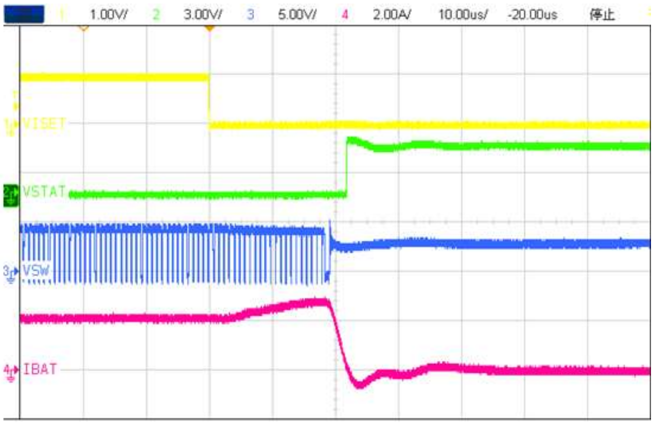


Figure 15. ISET Short
($V_{VBUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

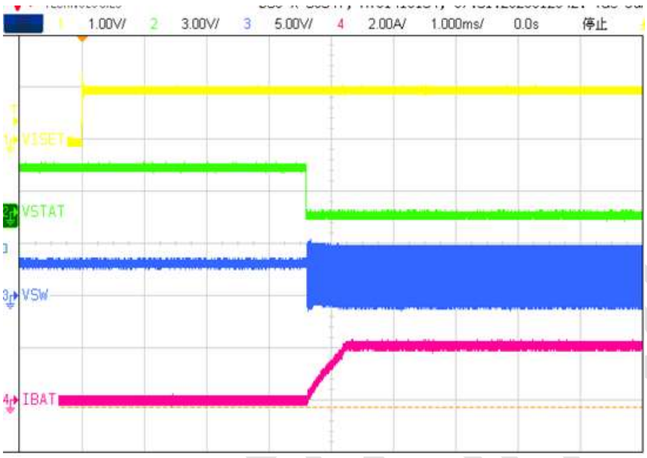


Figure 16. ISET Released from Short
($V_{VBUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

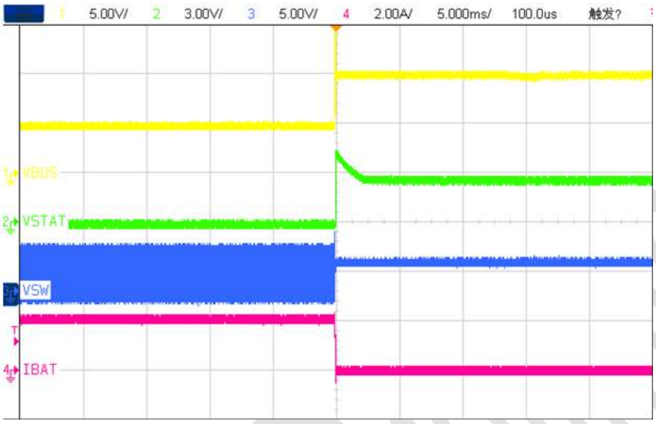


Figure 17. Input Over Voltage
($V_{VBUS}$=5V to 15V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

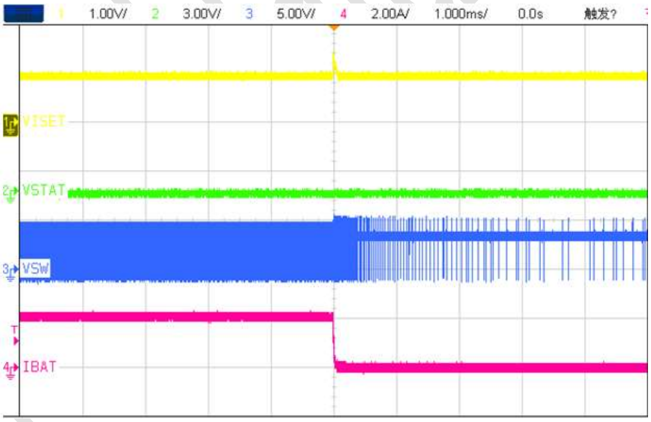
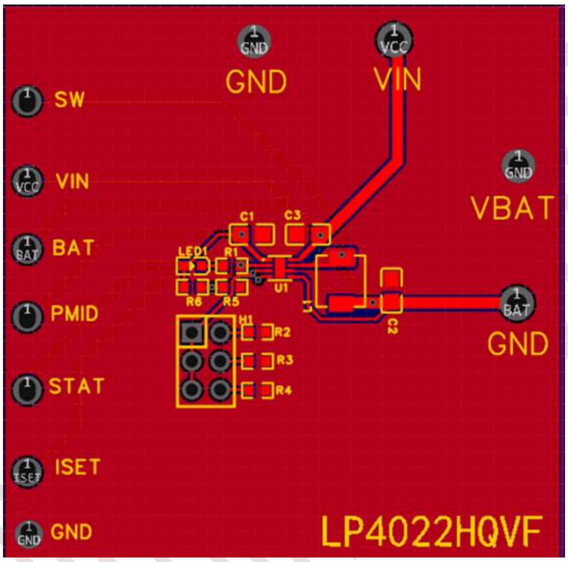


Figure 18. RISET Floating or Pulled High
($V_{VBUS}$=5V, $V_{BAT}$=3.8V, $I_{CHG}$=2A)

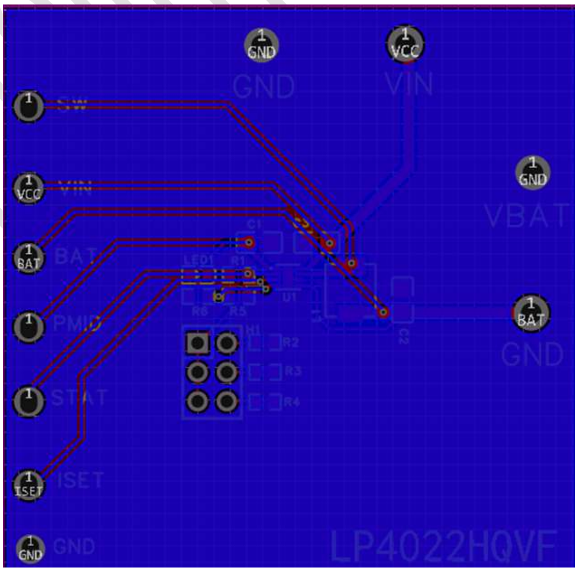
## PCB Layout Guideline

Appropriate PCB layout is important in the power supply design. Good PCB layout minimizes EMI and noises, allows good output voltage regulation and achieves higher efficiency. The following design considerations are recommended:

- Decouple PMID and VBUS pins to power GND on top layer and place decoupling capacitors as close to those pins as possible. Always avoid vias if possible because they have parasitic inductance and resistance. If vias are inevitable, always use more than one vias in parallel to decrease parasitics for power traces.
- Connect IC GND pad to the power ground plane on the bottom side with multiple vias that is for both heat dissipation and electrical connection.
- Minimize switching SW node size and trace lengths and keep it away from ISET and BAT traces.
- A PCB layout example is shown in Figure 19.
-



Top Layer

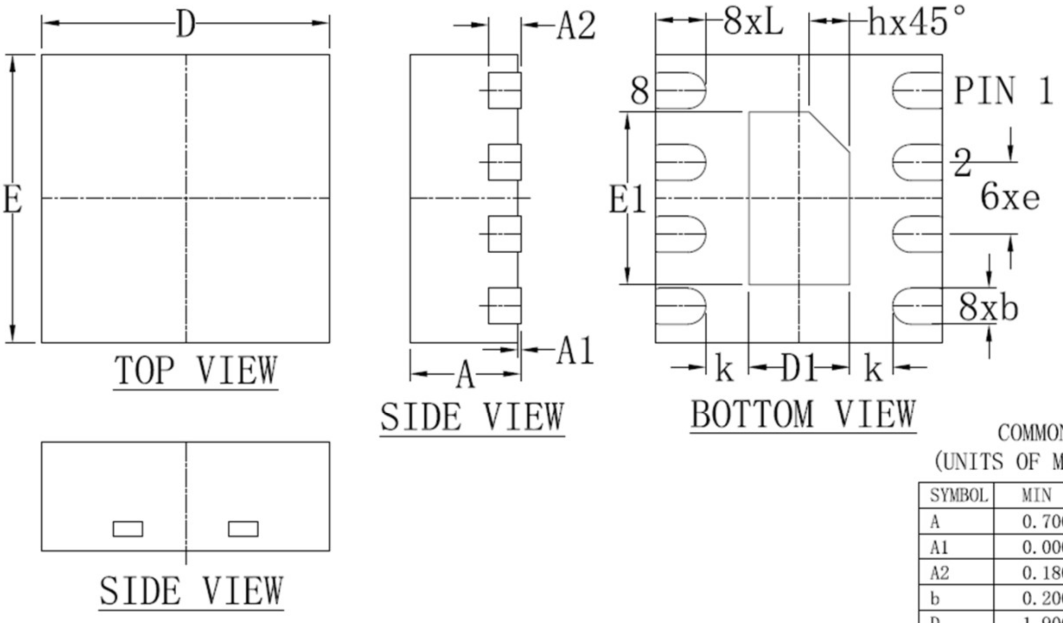


Bottom Layer

Figure 19. 2-layer PCB Layout Example

## Packaging Information

### DFN2x2-8

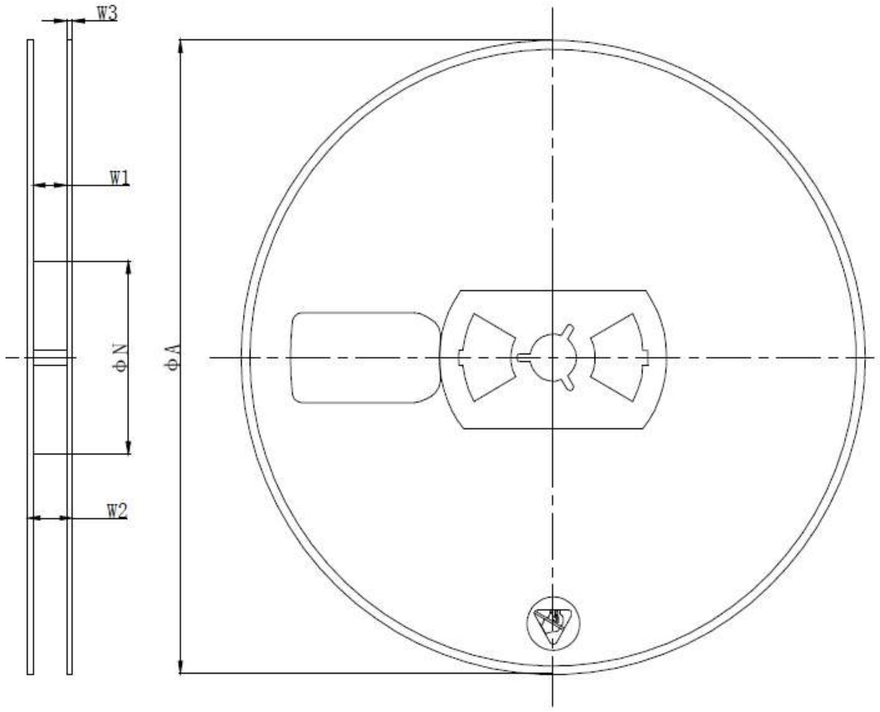


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.700 | 0.750 | 0.800 |
| A1 | 0.000 | / | 0.050 |
| A2 | 0.180 | 0.203 | 0.220 |
| b | 0.200 | 0.250 | 0.300 |
| D | 1.900 | 2.000 | 2.100 |
| D1 | 0.600 | 0.700 | 0.800 |
| E | 1.900 | 2.000 | 2.100 |
| E1 | 1.100 | 1.200 | 1.300 |
| e | 0.475 | 0.500 | 0.525 |
| h | 0.230 | 0.280 | 0.330 |
| k | 0.280 | 0.300 | 0.320 |
| L | 0.300 | 0.350 | 0.400 |

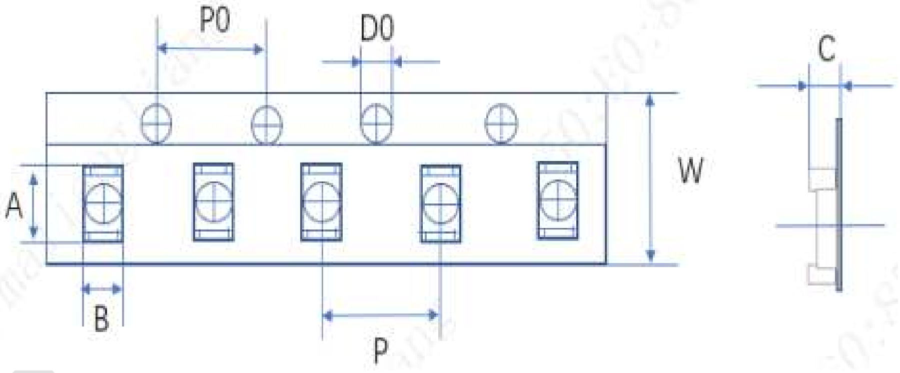
## Carrier Information

Reel Dimensions (Unit: mm)



| Device | ΦA | W2 |
|---|---|---|
| LP4022HQVF | 180±4 | 12±3 |

Tape Dimension (Unit: mm)



| Device | A | B | P0 | P | D0 | W | C |
|---|---|---|---|---|---|---|---|
| LP4022HQVF | 2.15±0.30 | 2.15±0.30 | 4.00±0.20 | 4.00±0.20 | 1.50±0.20 | 8.00±0.30 | 1.0±0.20 |

Pin 1 and Tape Feeding Direction