



Features

- Input voltage range: 2.7-V to 5.5-V
- VPOS positive boost converter output
 - ◇ Adjustable output: up to 15 V
 - ◇ Switch current limit 2 A
 - ◇ Conversion efficiency: up to 89%
- VNEG negative inverting buck-boost converter output
 - ◇ Adjustable output: down to -15 V
 - ◇ Switch current limit 2 A
 - ◇ Conversion efficiency: up to 81%
- Control output for external P-channel FET
- Supports complete disconnection from battery
- 1µA shutdown current
- Individual enable inputs for flexible output sequencing
- Protection features
 - ◇ Over voltage protection at VPOS and VNEG
 - ◇ Input under voltage lockout
 - ◇ VPOS and VNEG SCP
 - ◇ Thermal shutdown protection
- 4-mm × 4-mm QFN-24 package

Application

- LCD and AMOLED displays (approx. 4" to 17")
 - ◇ Personal electronics (notebook, monitor, gaming)
 - ◇ Healthcare, fitness, EPOS, industrial HMI, test & measurement

General Description

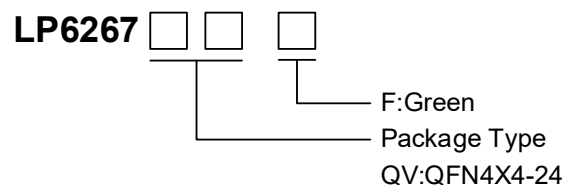
The LP6267QVF device is a dual-output DC-DC converter supply that generates a positive output up to 15 V and a negative output down to -15 V. The converter maintains low output voltage ripple. Typically, the maximum output currents are in the 200- mA to 500-mA range, depending on input voltage to output voltage ratio and the current limit option. The combined (VPOS and VNEG) efficiency reaches 85% to keep systems cool or achieve a longer battery-on time. The input voltage range of 2.7 V to 5.5 V allows the devices to be powered from batteries or from fixed 3.3-V or 5-V rails.

The converter operates with a fixed frequency PWM control topology and, when operating in power save mode, uses a pulse skipping mode at light load currents. It operates with only 500µA device quiescent current.

Independent enable pins allow flexible power-up and power-down sequencing for both outputs. The positive and negative outputs operate independently, allowing for non-symmetrical output voltages and currents.

The converter has an internal current limit, over voltage protection, and a thermal shutdown for highest reliability under fault conditions. The converter is available in a 4-mm × 4-mm QFN-24 package. The solution size is small with a minimum switching frequency of 1.25 MHz for smaller inductors and few other external components required.

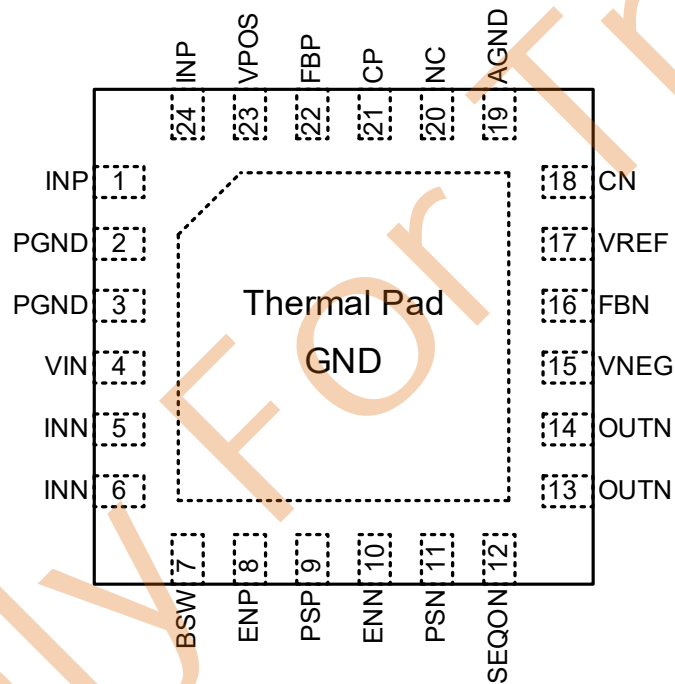
Order Information



Device Information

| Part Number | Top Marking | Moisture Sensitivity Level | Package | Shipping |
|--|----------------------|----------------------------|-----------|----------|
| LP6267QVF | LPS LP6267 YWX | MSL3 | QFN4X4-24 | 3K/REEL |
| Marking indication: Y: Year code. W: Week code. X: Batch numbers. | | | | |

Pin Configuration

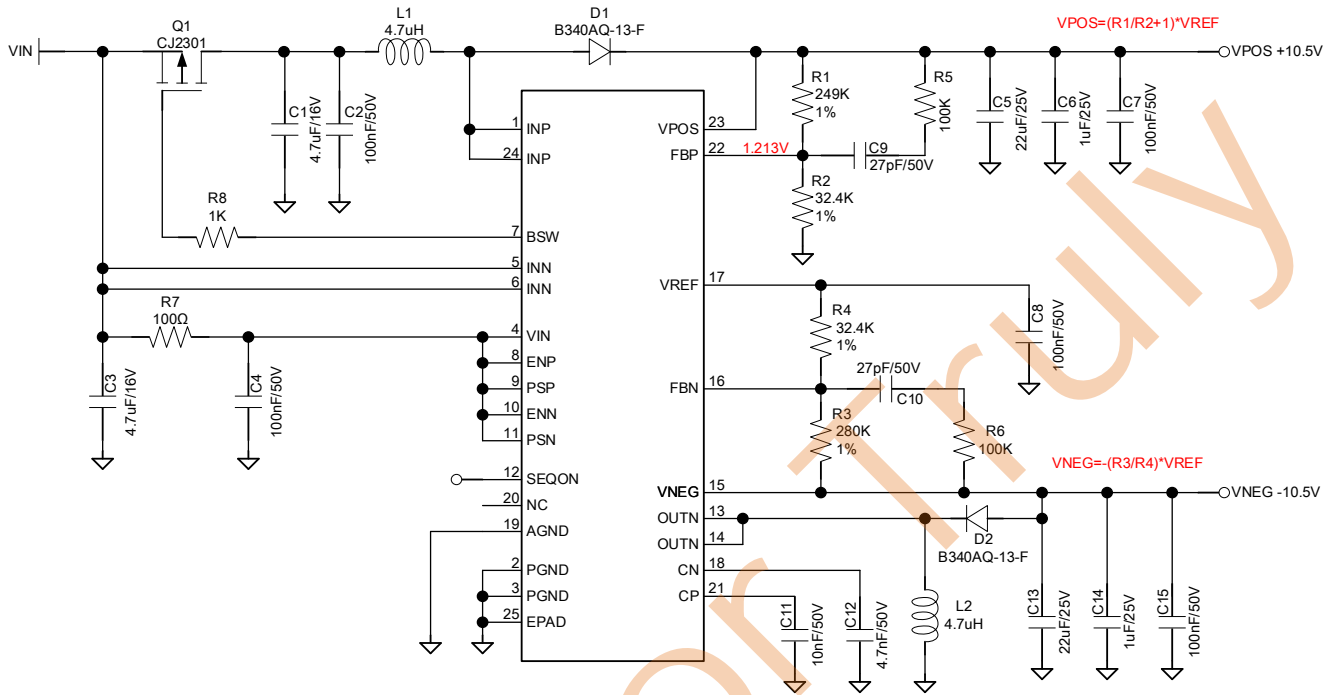


QFN4X4-24 (Top View)

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation



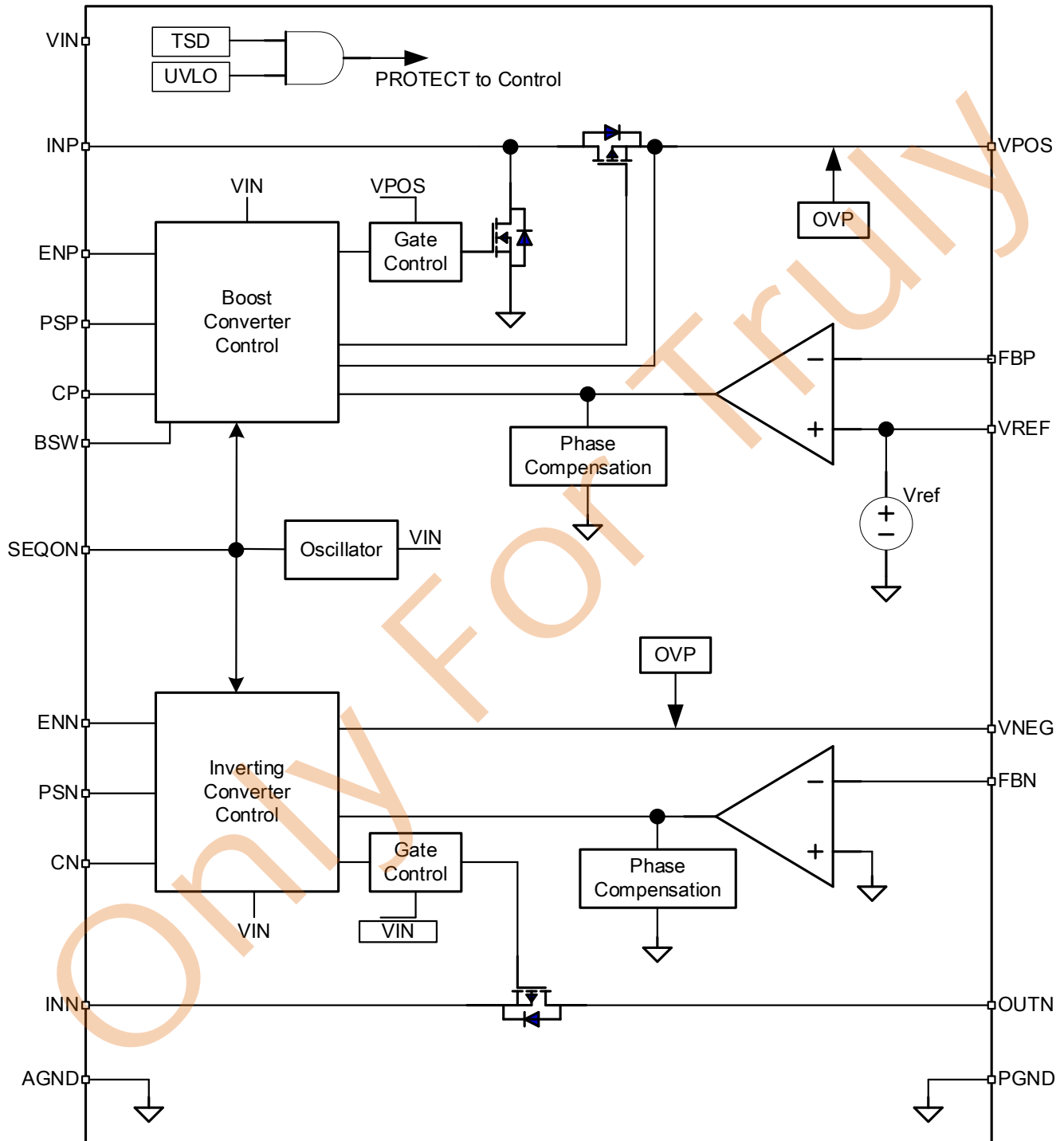
Type Application Circuit



Special attention was paid to the selection of isolated PMOS(Q1), $V_{IN} - V_{GS(TH).max} > 1.5V$



Functional Block Diagram



Pin Description

| PIN | NAME | FUNCTION |
|-----|-----------------------|--|
| 1 | INP | Boost converter switch input. |
| 2 | PGND | Power ground PIN |
| 3 | PGND | Power ground PIN |
| 4 | VIN | Control supply input |
| 5 | INN | Inverting converter switch input |
| 6 | INN | Inverting converter switch input |
| 7 | BSW | Gate control pin for external battery switch. This pin goes low when ENP is set high. |
| 8 | ENP | Enable pin for the positive output voltage (0 V: disabled, VIN: enabled) |
| 9 | PSP | Power-save mode enable for boost converter stage (0 V: disabled, VIN: enabled) |
| 10 | ENN | Enable pin for the negative output voltage (0 V: disabled, VIN: enabled) |
| 11 | PSN | Power-save mode enable for inverter stage (0 V: disabled, VIN: enabled) |
| 12 | SEQON | Power ON sequence Control |
| 13 | OUTN | Inverting converter switch output. |
| 14 | OUTN | Inverting converter switch output. |
| 15 | VNEG | Negative output voltage sense input |
| 16 | FBN | Feedback pin for the negative output voltage divider |
| 17 | VREF | Reference output voltage. Bypass this pin with a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin |
| 18 | CN | Compensation pin for inverting converter control |
| 19 | AGND | Analog ground pin |
| 20 | NC | Not connected |
| 21 | CP | Compensation pin for boost converter control |
| 22 | FBP | Feedback pin for the positive output voltage divider |
| 23 | VPOS | Positive output voltage sense input |
| 24 | INP | Boost converter switch input. |
| 25 | PGND (Exposed Pad) | GND. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |



Absolute Maximum Ratings (Note 1)

| | | |
|--------------------------|-------|-------------------|
| VIN, INN to GND | ----- | -0.3V to +6.0V |
| VPOS to GND | ----- | -0.3V to +17V |
| VNEG to GND | ----- | -17V to VIN+0.3V |
| ENN, ENP to GND | ----- | -0.3V to VIN+0.3V |
| FBP, FBN to GND | ----- | -0.3V to VIN+0.3V |
| CN, CP to GND | ----- | -0.3V to VIN+0.3V |
| PSP, PSN, BSW to GND | ----- | -0.3V to VIN+0.3V |
| INP to GND | ----- | -0.3V to +17V |
| OUTN to V _{INN} | ----- | -0.3V to +24V |
| AGND, PGND to GND | ----- | -0.3V to 0.3V |

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability

Recommend Operating Range

| | | |
|--|-------|----------------|
| Junction Temperature | ----- | 150°C |
| Operating Junction Temperature Range (TJ) | ----- | -40°C to 150°C |
| Ambient Temperature Range | ----- | -40°C to 85°C |
| Storage Temperature Range | ----- | -65°C to 150°C |
| Reflow Temperature (soldering, 10sec) | ----- | 260°C |
| Thermal Resistance Junction to Ambient, (θJA)* | | |
| QFN4X4-24 | ----- | 55.3°C/W |
| Continuous Power Dissipation (TA=25°C)* | | |
| QFN4X4-24 | ----- | 1.8 W |
| Thermal Resistance Junction to Case, (θJC) | | |
| QFN4X4-24 | ----- | 9.9°C/W |

Note 2. Please refer to 1in² of 1oz PCB Layout Section.

ESD Susceptibility (Note 2)

| | | |
|--------------------------------|-------|-------|
| ESD HBM (Human Body Model) | ----- | 2000V |
| ESD MM (Machine Model) | ----- | 300V |
| ESD CDM (Charged Device Model) | ----- | 1000V |

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

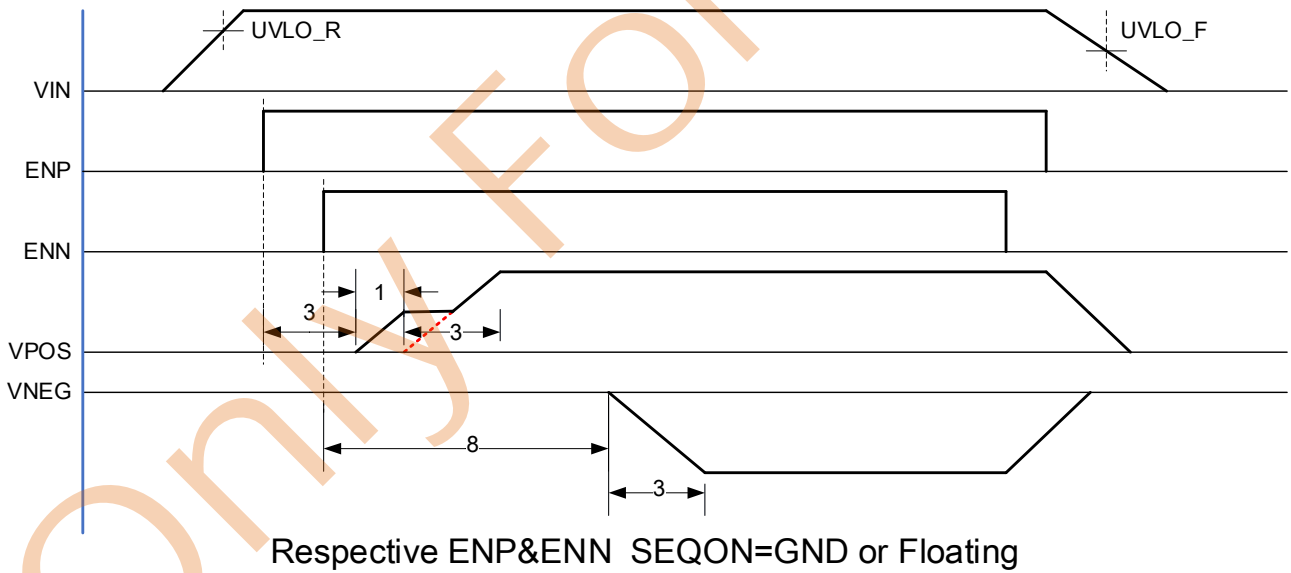
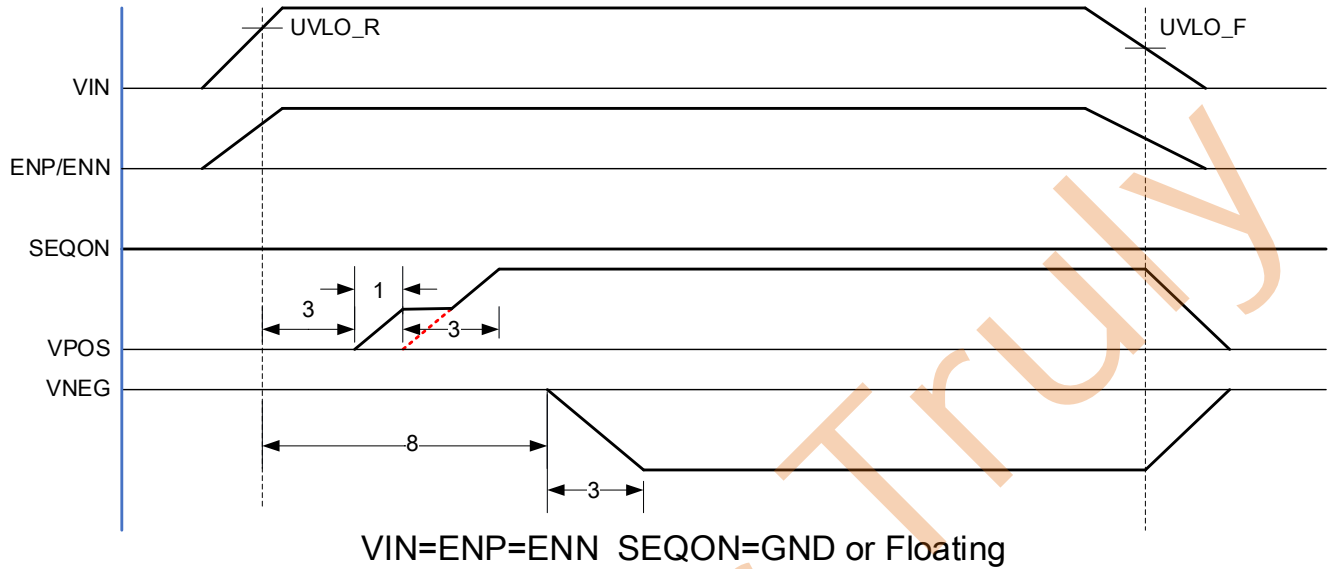
Electrical Characteristics

over the full recommended input voltage range $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ and over the temperature range $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ unless otherwise noted. Typical values apply for $V_{IN} = 3.6\text{ V}$ and $T_J = 25^\circ\text{C}$.

| PARAMETR | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|--------------|-------|-------|------------------|
| V_{IN} Input Voltage Range | | 2.7 | 3.3 | 5.5 | V |
| V_{IN} Quiescent current | $V_{IN} = 3.6\text{ V}$, $I_{POS} = I_{NEG} = 0$, $ENP = ENN = PSP = PSN = V_{IN}$, $V_{POS} = 6\text{ V}$, $V_{NEG} = -6\text{ V}$ | --- | 0.8 | 6.0 | mA |
| I_Q Shutdown supply current | $ENN = ENP = GND$ | --- | 100 | 200 | μA |
| V_{UVLO} Under voltage lockout threshold | V_{IN} rising, turn-on IC | 2.4 | 2.50 | 2.6 | V |
| V_{UVLO_H} hysteresis Voltage | $V_{UVLO_H} = V_{UVLO_R} - V_{UVLO_F}$ | 0.1 | 0.15 | 0.2 | V |
| T_{SD} Thermal shutdown | | 150 | 160 | 170 | $^\circ\text{C}$ |
| T_{HYST} Thermal shutdown hysteresis | | --- | 15 | --- | $^\circ\text{C}$ |
| V_{IH} ENP, ENN, PSP, PSN, SEQON | High voltage | 1.4 | --- | --- | V |
| V_{IL} ENP, ENN, PSP, PSN, SEQON | Low voltage | --- | --- | 0.4 | V |
| I_{IN} Input current, ENP, ENN, PSP, PSN | $ENP, ENN, PSP, PSN = GND$ or V_{IN} | --- | 0.01 | 0.1 | μA |
| SEQON Internal Pull Down Resistor | | --- | 1 | --- | M Ω |
| R_{BSW} Output resistance | | --- | 10 | --- | K Ω |
| V_{POS} Adjustable output voltage range | | $V_{IN}+0.5$ | --- | 15 | V |
| V_{NEG} Adjustable output voltage range | | -15 | --- | -2 | V |
| V_{REF} Reference voltage | $I_{REF} = 10\ \mu\text{A}$ | 1.2 | 1.213 | 1.225 | V |
| I_{FBP} Positive feedback input bias current | $V_{FBP} = V_{REF}$ | | 50 | | nA |
| I_{FBN} Negative feedback input bias current | $V_{FBN} = 0.1 V_{REF}$ | | 50 | | nA |
| V_{FBP} Positive feedback regulation voltage | $V_{IN} = 2.7\text{ V}$ to 5.5 V | 1.189 | 1.213 | 1.237 | V |
| V_{FBN} Negative feedback regulation voltage | $V_{IN} = 2.7\text{ V}$ to 5.5 V | -0.024 | 0 | 0.024 | V |
| Total Output DC accuracy | | -1.5 | | +1.5 | % |
| $R_{DS(ON)(N)}$ Inverter switch ON-resistance | $V_{IN} = 3.6\text{ V}$ | | 250 | 400 | m Ω |
| | $V_{IN} = 5.0\text{ V}$ | | 200 | 400 | m Ω |
| I_{LIMN} Inverter switch current limit | $V_{IN} = 3.6\text{ V}$ | 1800 | 2200 | | mA |
| $R_{DS(ON)(P)}$ Boost switch ON-resistance | $V_{POS} = 3.6\text{ V}$ | | 200 | 300 | m Ω |
| | $V_{POS} = 5\text{ V}$ | | 150 | 200 | m Ω |
| I_{LIMP} Boost switch current limit | $V_{IN} = 3.6\text{ V}$; $V_{POS} = 8\text{ V}$ | 1800 | 2200 | | mA |
| F_S Oscillator frequency | $-40 < T_a < 85^\circ\text{C}$ | 1250 | 1380 | 1500 | KHz |
| D_{MAXP} Maximum duty Boost converter | | | 87.5 | | % |
| D_{MAXN} Maximum duty Inverter converter | | | 87.5 | | % |
| D_{MINP} Minimum duty Boost converter | | | 12.5 | | % |
| D_{MINN} Minimum duty Inverter converter | | | 12.5 | | % |
| V_{POS} Power Off Discharge | Only SEQON = Hi | --- | 200 | --- | Ω |
| V_{NEG} Power Off Discharge | Only SEQON = Hi | --- | 200 | --- | Ω |

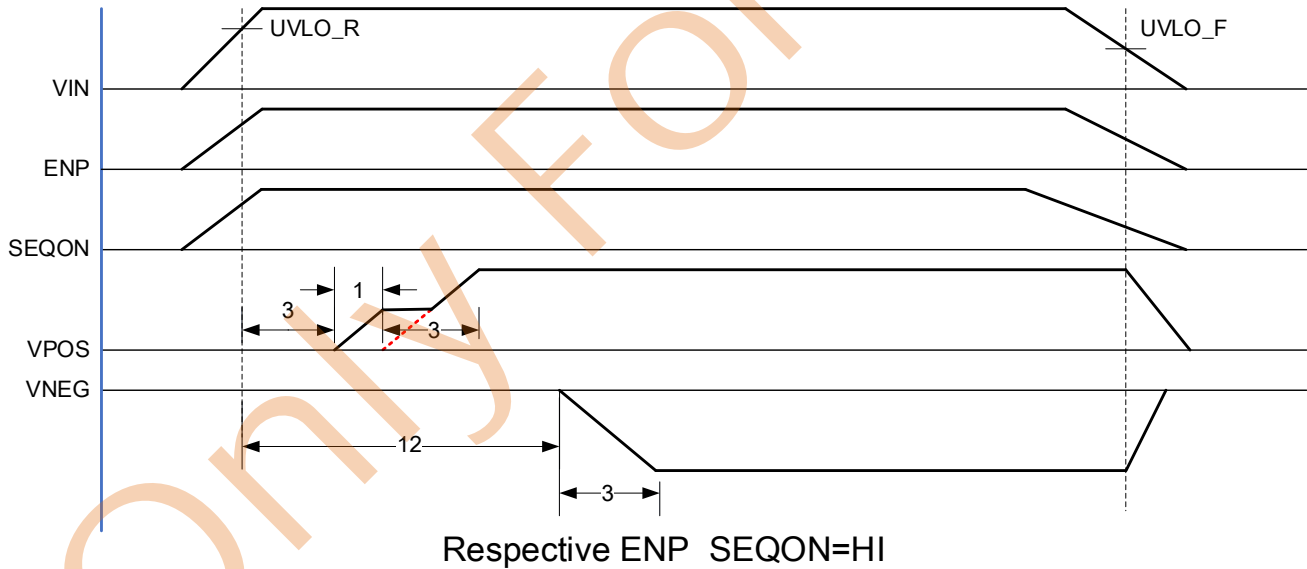
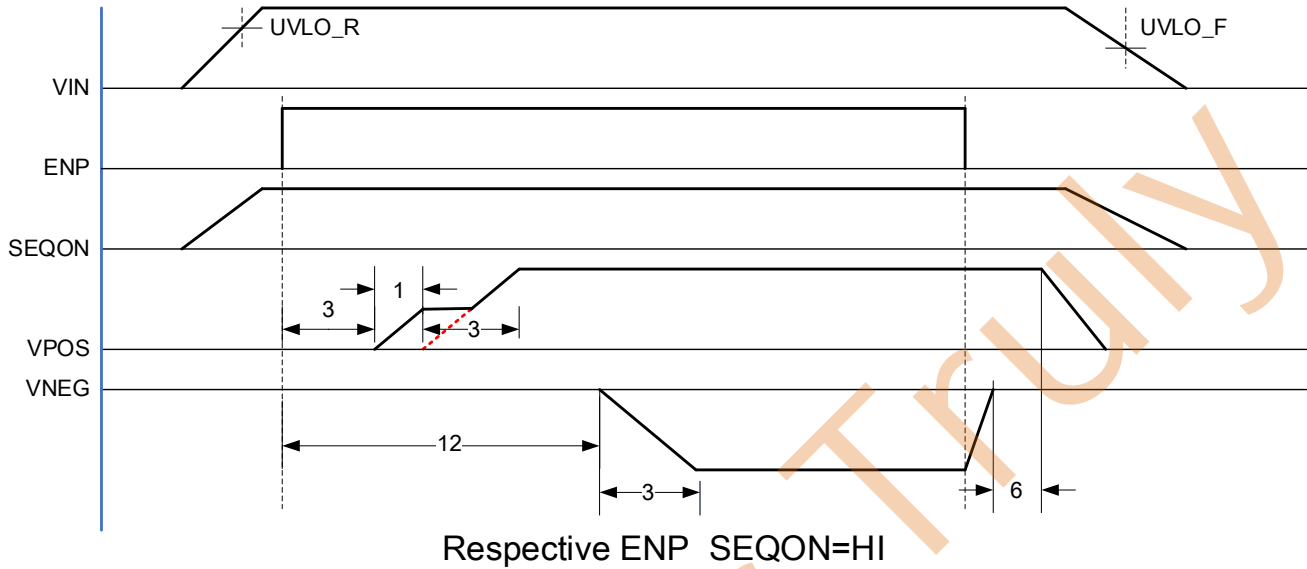


Timing Chart1





Timing Chart2



Applications Information

The LP6267QVF operates with an input voltage range of 2.7 V to 5.5 V and can generate both a positive and negative output. Both converters work independently of each other. They only share a common clock and a common voltage reference. Both outputs are separately controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. In general, each converter operates at continuous conduction mode (CCM). At light loads, the negative converter can enter discontinuous conduction mode (DCM). As the load current decreases, the converters can enter a power-save mode if enabled. This works independently at both converters. Output voltages can go up to 15 V at the boost output and down to -15 V at the inverter output.

Power Conversion

Both converters operate in a fixed-frequency, PWM control scheme. So, the ON-time of the switches varies depending on input-to-output voltage ratio and the load. During this ON-time, the inductor connected to the converters charge with current. In the remaining time, the time period set by the fixed operating frequency, the inductor discharge into the output capacitors through the rectifier diodes. Usually at greater loads, the inductor currents are continuous. At lighter loads, the boost converter uses an additional internal switch to allow current flowing back to the input. This avoids inductor current becoming discontinuous in the boost converter. So, the boost converter is always controlled in a continuous current mode. At the inverting converter, during light loads, the inductor current can become discontinuous. In this case, the control circuit of the inverting controller output automatically takes care of these changing conditions to always operate with an optimum control setup.

Control

The controller circuits of both converters employ a fixed-frequency, multiple-feed forward controller topology. The circuits monitor input voltage, output voltage, and voltage drop across the switches. Changes in the operating conditions of the converters directly affect the duty cycle and must not take the indirect and slow way through the output voltage control loops. Measurement errors in this feed-forward system are corrected by a self-learning control system. An external capacitor damps the output to avoid output-voltage steps due to output changes of this self-learning control system.

The voltage loops, determined by the error amplifiers, must only handle small signal errors. The error amplifiers feature internal compensation. Their inputs are the feedback voltages on the FBP and FBN pins. The device uses a comparison of these voltages with the internal reference voltage to generate an accurate and stable output voltage.

Enable

Both converters can be enabled or disabled individually. Applying a logic HIGH signal at the enable pins (ENP for the boost converter, ENN for the inverting converter) enables the corresponding output. After enabling, internal circuitry necessary to operate the specific converter turns on followed by the soft-start period.

Applying a low signal at the enable ENP or ENN pin shuts down the corresponding converter. When both enable pins are low, the device enters shutdown mode, where all internal circuitry turns off. At this point, the device consumes shutdown current flowing into the VIN pin. The output loads of the converters can be disconnected from the input



Load Disconnect

The device supports completely disconnecting the load when the converters are disabled. For the inverting converter, the device turns off the internal PMOS switch. If the inverting converter is turned off, no DC current path remains which could discharge the battery or supply.

This is different for the boost converter. The external rectifying diode, together with the boost inductor, form a DC current path which could discharge the battery or supply if any load connects to the output. The device has no internal switch to prevent current from flowing. For this reason, the device offers a PMOS gate control output (BSW) to enable and disable a PMOS switch in this DC current path, ideally directly between the boost inductor and battery. To be able to fully disconnect the battery, the forward direction of the parasitic back gate diode of this switch must point to the battery or supply. The external PMOS switch, which connects to BSW, turns on when the boost converter is enabled and turns off when the boost converter is disabled.

Soft-Start

Both converters have implemented soft-start functions. When each converter is enabled, the implemented switch current limit ramps up slowly to its nominal programmed value in about 3 ms. Soft-start is implemented to limit the input current during start-up to avoid high peak currents at the battery which could interfere with other systems connected to the same battery. Without soft-start, the high input peak current could trigger the implemented switch current limit, which can lead to a significant voltage drops across the series resistance of the battery and its connections.

Over Voltage Protection

Both converters (boost and inverter) have implemented individual over voltage protection. If the feedback voltage under normal operation exceeds the nominal value by typically 5%, the corresponding converter shuts down immediately to protect any connected circuitry from possible damage.

Under Voltage Lockout

An undervoltage lockout (UVLO) prevents the device from starting up and operating if the supply voltage at the VIN pin is lower than the undervoltage lockout threshold. For this case, the device automatically shuts down both converters when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown.

Over Temperature Shutdown

The device automatically shuts down both converters if the implemented internal temperature sensor detects a chip temperature above the thermal shutdown temperature. It automatically starts operating again when the chip temperature falls below this thermal shutdown temperature. The built-in hysteresis avoids undefined operation caused by ringing from shutdown and prevents operating at a temperature close to the over temperature shutdown threshold.

Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically require special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of heat-generating components affect the power dissipation limits of a given component.

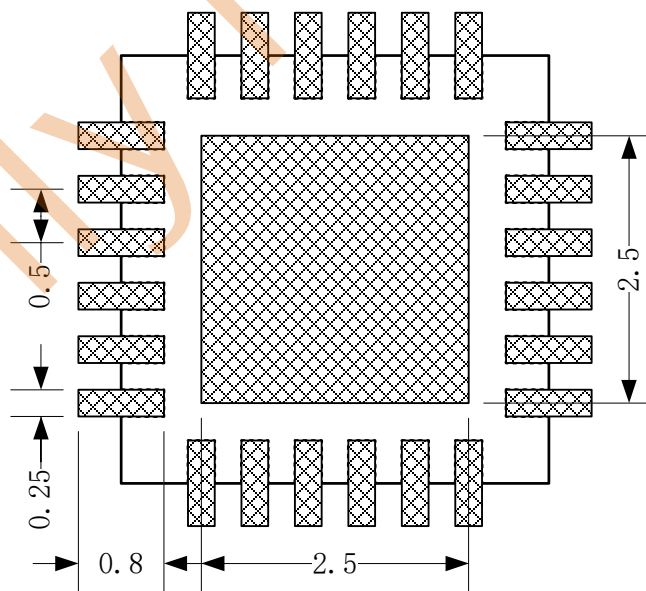
These three basic approaches enhance thermal performance:

- ✧ Improving the power dissipation capability of the PCB design.
- ✧ Improving the thermal coupling of the component to the PCB.
- ✧ Introducing airflow to the system.

The recommended device junction temperature range, T_J , is -40°C to 125°C . The thermal resistance of the QFN4X4-24 package is $R_{\theta JA} = 55.3^{\circ}\text{C}/\text{W}$. The recommended operating ambient temperature range for the device is $T_A = -40^{\circ}\text{C}$ to 85°C . Use Equation 1 to calculate the maximum power dissipation, P_{Dmax} , as a function of T_A . In this equation, use $T_J = 125^{\circ}\text{C}$ to operate the device within the recommended temperature range, use $T_J = T_{TS}$ to determine the absolute maximum threshold when the device might go into thermal shutdown. If the maximum ambient temperature of the application is lower, more heat dissipation is possible.

$$P_{D.MAX} = \frac{T_J - T_A}{R_{\theta JA}} \quad (1)$$

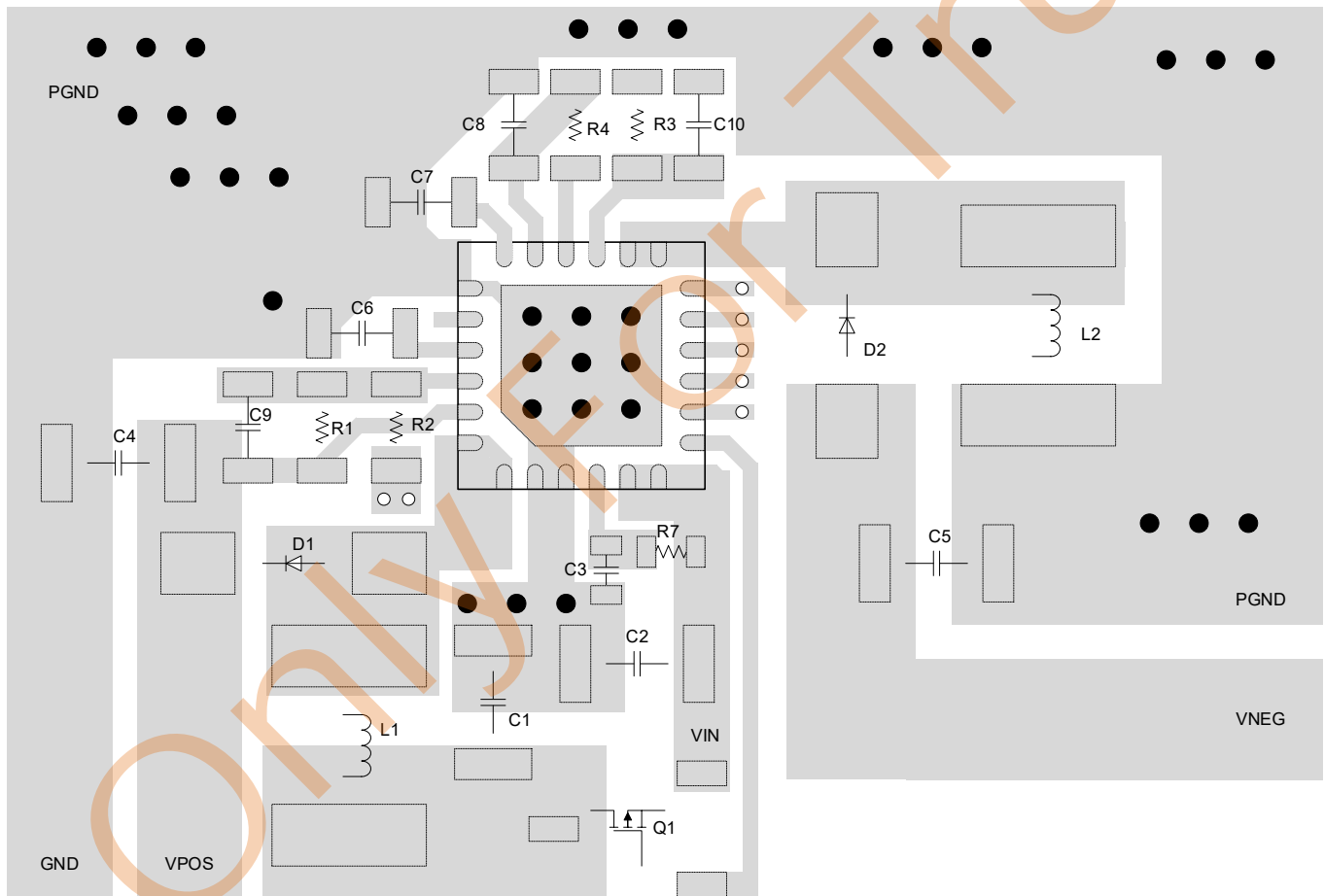
Minimum Footprint PCB Layout Section



QFN4X4-24

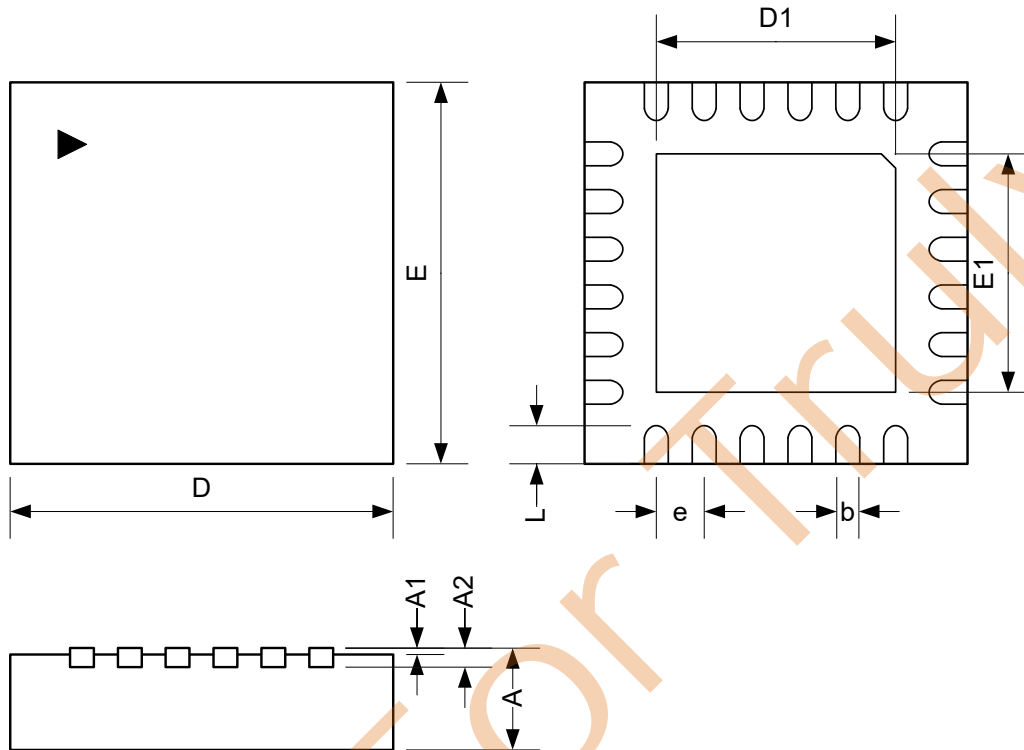
Layout Consideration

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. Therefore, use wide and short traces for the main current paths and for the power ground tracks. The input capacitors (C1, C2, C3), output capacitors (C4, C5), the inductors (L1, L2), and the rectifying diodes (D1, D2) should be placed as close as possible to the IC to keep parasitic inductances low. Use a wide power ground (PGND) plane. Connect the analog ground pin (AGND) to the PGND plane. Further, connect the PGND plane with the exposed thermal pad. Place the feedback dividers as close as possible to the control pin (boost converter) or the VREF pin (inverting converter) of the IC.





Packaging Information



QFN4X4-24

| Symbol | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|------|------|-------------------|--------|--------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.0276 | 0.0295 | 0.0315 |
| A1 | 0.00 | --- | 0.05 | 0.0000 | --- | 0.0020 |
| A2 | 0.20 REF | | | 0.0079 REF | | |
| D | 3.90 | 4.00 | 4.10 | 0.1535 | 0.1575 | 0.1614 |
| E | 3.90 | 4.00 | 4.10 | 0.1535 | 0.1575 | 0.1614 |
| D1 | 2.40 | 2.50 | 2.60 | 0.0945 | 0.0984 | 0.1024 |
| E1 | 2.40 | 2.50 | 2.60 | 0.0945 | 0.0984 | 0.1024 |
| b | 0.18 | 0.25 | 0.30 | 0.0071 | 0.0098 | 0.0118 |
| e | 0.5 BSC | | | 0.0256 BSC | | |
| L | 0.35 | 0.40 | 0.45 | 0.0138 | 0.0157 | 0.0177 |