

300mA, Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3992 is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3992 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. The LP3992 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3992 consumes less than 0.1 μ A in shutdown mode and has fast turn-on time less than 50 μ s. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. It is available in the 5-lead of SOT23-5 and TSOT23-5 packages.

Order Information

LP3992	□ □ □ □ □	
		F: Pb-Free
		Package Type
		B3: SOT23-3
		B5: SOT23-5
		J5: TSOT23-5
		Output Type
		12: 1.2V
		15: 1.5V
		18: 1.8V
		25: 2.5V
		28: 2.8V
		30: 3.0V
		33: 3.3V
		36: 3.6V
		50: 5.0V

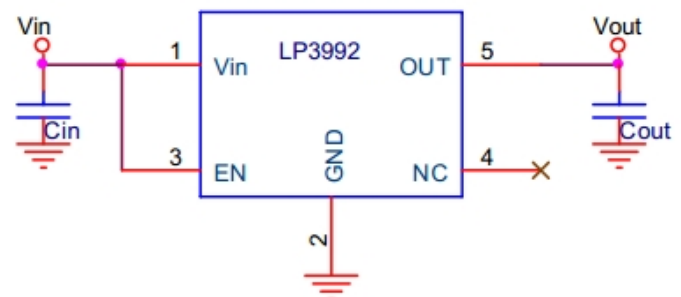
Features

- ◆ Ultra-Low-Noise for RF Application
- ◆ 2.5V- 5.5V Input Voltage Range
- ◆ Low Dropout : 220mV @ 300mA
- ◆ 1.2V, 1.5V, 1.8V, 2.5V, 2.8V,3.0V,3.3V, 3.6V and 5V Fixed
- ◆ 300mA Output Current
- ◆ High PSRR:-76dB at 1KHz
- ◆ < 1uA Standby Current When Shutdown
- ◆ Available in SOT23-5、 SOT23 and TSOT23-5 Package
- ◆ TTL-Logic-Controlled Shutdown Input
- ◆ Ultra-Fast Response in Line/Load transient
- ◆ Current Limiting and Thermal Shutdown Protection
- ◆ Quick start-up (typically 50uS)

Applications

- ◇ Portable Media Players/MP3 players
- ◇ Cellular and Smart mobile phone
- ◇ LCD
- ◇ DSC Sensor
- ◇ Wireless Card

Typical Application Circuit



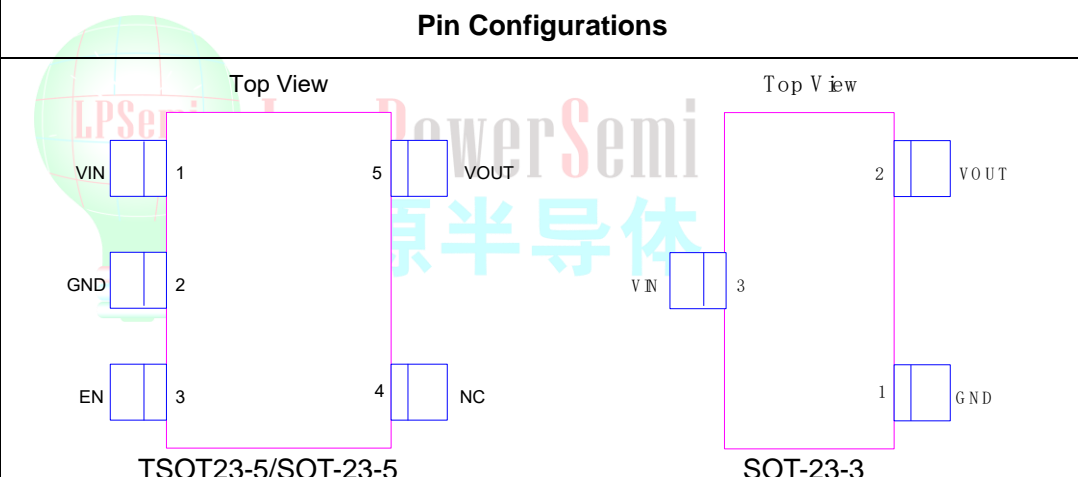
Marking Information

Device	Marking	Package	Shipping
LP3992-12B5F	LPS 1BYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL
LP3992-15B5F	LPS 1NYWX / LPS 4NYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL
LP3992-18B5F	LPS 1CYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL

Device	Marking	Package	Shipping
LP3992-28B5F	LPS 1HYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL
LP3992-25B5F	LPS 1DYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL
LP3992-30B5F	LPS 1GYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL
LP3992-33B5F	LPS 1EYWX	SOT23-3 SOT23-5 TSOT23-5	3K/REEL

Y: Y is year code. W: W is week code. X: X is series number.

Functional Pin Description

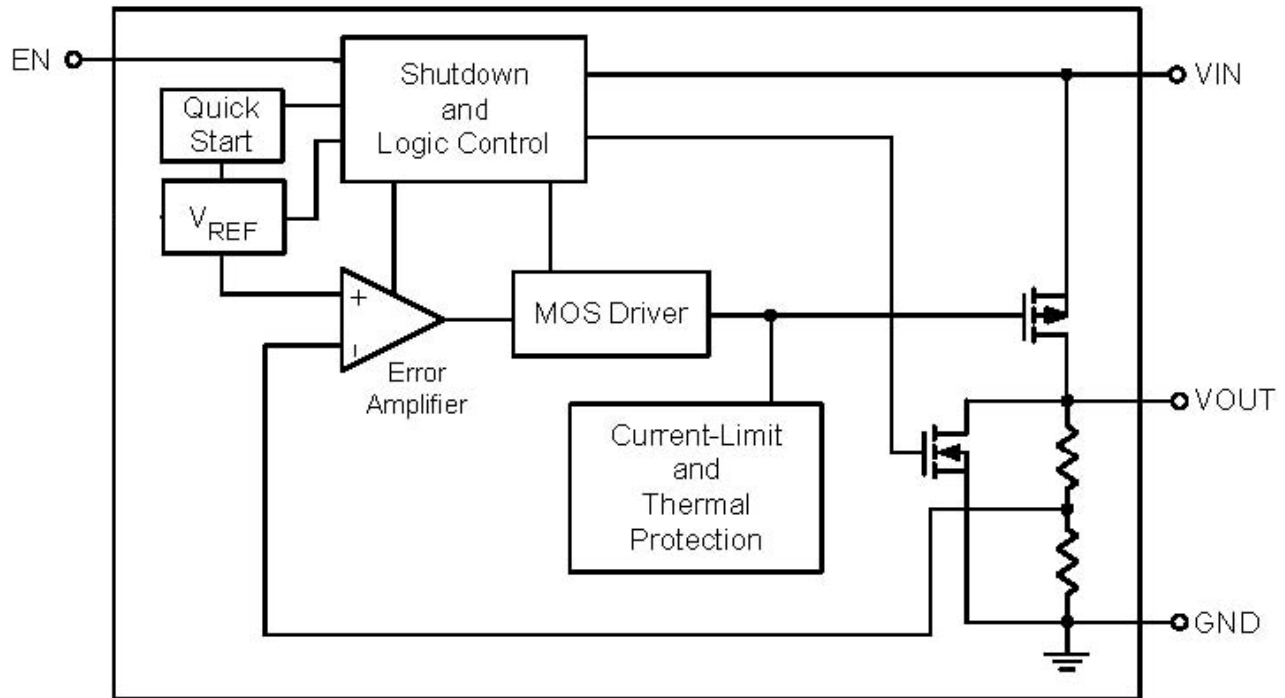
Package Type	Pin Configurations
TSOT23-5 SOT-23-5 SOT-23-3	 <p>Top View</p> <p>Top View</p> <p>TSOT23-5/SOT-23-5</p> <p>SOT-23-3</p>

Pin Description

Pin		Name	Description
SOT23-5	SOT23-3		
1	3	VIN	Power Input Voltage.
2	1	GND	Ground.
3		EN	Chip Enable (Active High).
4		NC	No Connection.
5	2	VOUT	Output Voltage.



Function Diagram



Absolute Maximum Ratings

◇ Supply Input Voltage 6.5V

◇ Other Pin Voltage -0.3V to VIN+0.3V

Power Dissipation, PD @ TA = 25°C

◇ T/SOT23-5 500mW

◇ SOT23-3 500mW

Package Thermal Resistance

◇ Thermal Resistance(SOT23-5/SOT23) (JA) 195°C/W

◇ Thermal Resistance(SOT23-5/SOT23) (JC) 60°C/W

◇ Maximum Junction Temperature 150°C

◇ Maximum Soldering Temperature (at leads, 10 sec) 260°C

◇ Storage Temperature Range -60°C to 125°C

ESD Susceptibility

◇ HBM (Human Body Mode) 2kV

◇ MM(Machine-Mode) 200V

Recommended Operating Conditions

- ◇ Supply Input Voltage ----- 2.5V to 5.5V
- ◇ EN Input Voltage ----- 0V to $V_{in}+0.3V$
- ◇ Operation Junction Temperature Range ----- $-40^{\circ}C$ to $125^{\circ}C$
- ◇ Operation Ambient Temperature Range ----- $-40^{\circ}C$ to $85^{\circ}C$

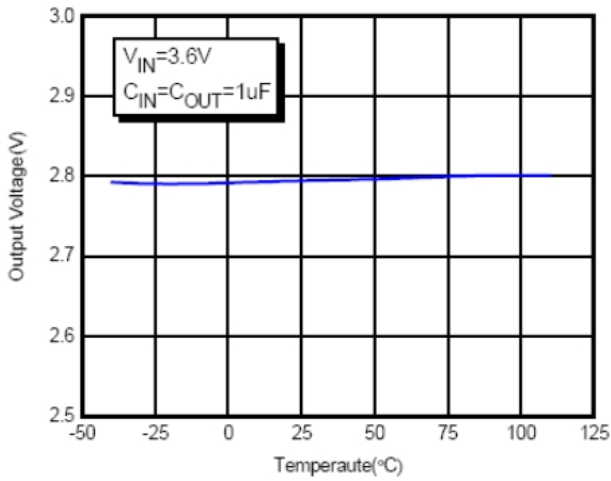
Electrical Characteristics

(LP3992-33B5F, $V_{IN} = V_{OUT} + 1V$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = 25^{\circ}C$, unless otherwise specified)

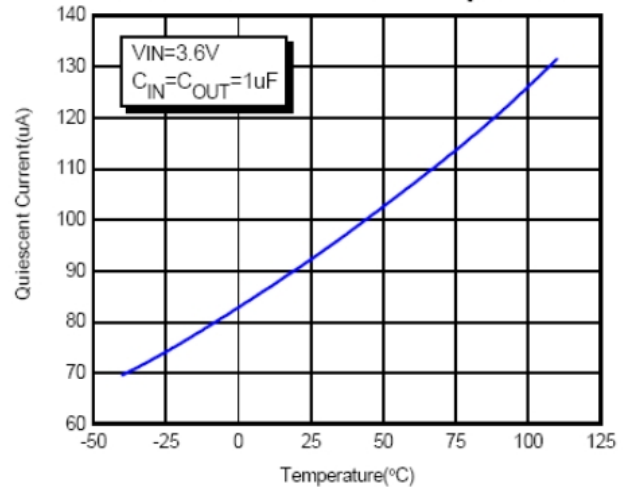
Parameter	Symbol	Test Conditions	Min	Typ.	Max	Units	
Output Voltage Accuracy	ΔV_{OUT}	$I_{OUT} = 1mA$	-3	--	+3	%	
Output Voltage	V_{OUT}	$I_{OUT} = 1mA$		3.33		V	
Output Loading Current	I_{LOAD}	$V_{EN}=V_{IN}, V_{IN}>2.5V$	300			mA	
Current Limit	I_{LIM}	$R_{LOAD} = 1\Omega$	420	450		mA	
Quiescent Current	I_Q	$V_{EN} \geq 1.4V, I_{OUT} = 0mA$		75	130	μA	
Dropout Voltage	V_{DROP}	$I_{OUT} = 200mA, V_{OUT} > 2.8V$		130	200	mV	
		$I_{OUT} = 300mA, V_{OUT} > 2.8V$		220	300		
Line Regulation	ΔV_{LINE}	$V_{IN} = (V_{OUT} + 1V)$ to $5.5V$, $I_{OUT} = 50mA$			0.2	%/V	
Load Regulation	ΔV_{LOAD}	$1mA < I_{OUT} < 300mA$			2	%/A	
Standby Current	I_{STBY}	$V_{EN} = GND$, Shutdown		0.01	1	μA	
EN Input Bias Current	I_{IBSD}	$V_{EN} = 3V$		1.5	3.5	μA	
EN Threshold	Logic-Low Voltage	V_{IL}	$V_{IN} = 3V$ to $5.5V$, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	$V_{IN} = 3V$ to $5.5V$, Start-Up	1.4		$V_{IN}+0.3$	
Output Noise Voltage		$10Hz$ to $100kHz$, $I_{OUT} = 200mA$, $C_{OUT} = 1\mu F$		300		$\mu VRMS$	
Power Supply Rejection Rate	$f = 1kHz$	$C_{OUT} = 1\mu F$, $I_{OUT} = 100mA$		-76		dB	
	$f = 10kHz$			-65			
Thermal Shutdown Temperature	TSD			150		$^{\circ}C$	

Typical Operating Characteristics

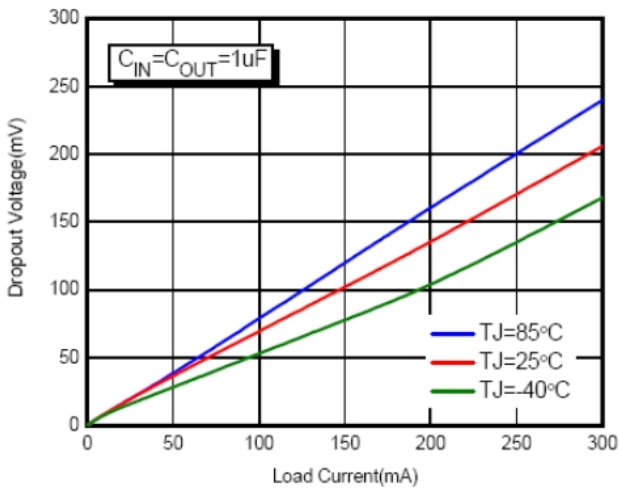
Output Voltage Vs. Temperature



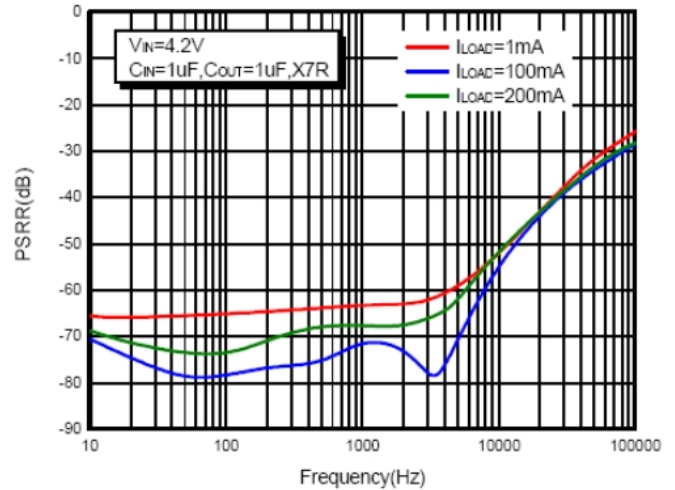
Quiescent Current Vs. Temperature



Dropout Voltage Vs. Load Current



PSRR



Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3992 must be carefully selected for regulator stability and performance. Using a capacitor whose value is $> 1\mu\text{F}$ on the LP3992 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3992 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ with ESR is $> 25\text{m}\Omega$ on the LP3992 output ensures stability. The LP3992 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP3992 and returned to a clean analog ground.

Start-up Function Enable Function

The LP3992 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For protecting the system, the LP3992 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in LP3992. When the operation junction temperature exceeds 150°C , the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C . For continue operation, do not exceed absolute maximum operation junction temperature 125°C .

The power dissipation definition in device is:

$$PD = (VIN - VOUT) \times I_{OUT} + VIN \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula:

$$PD(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$$

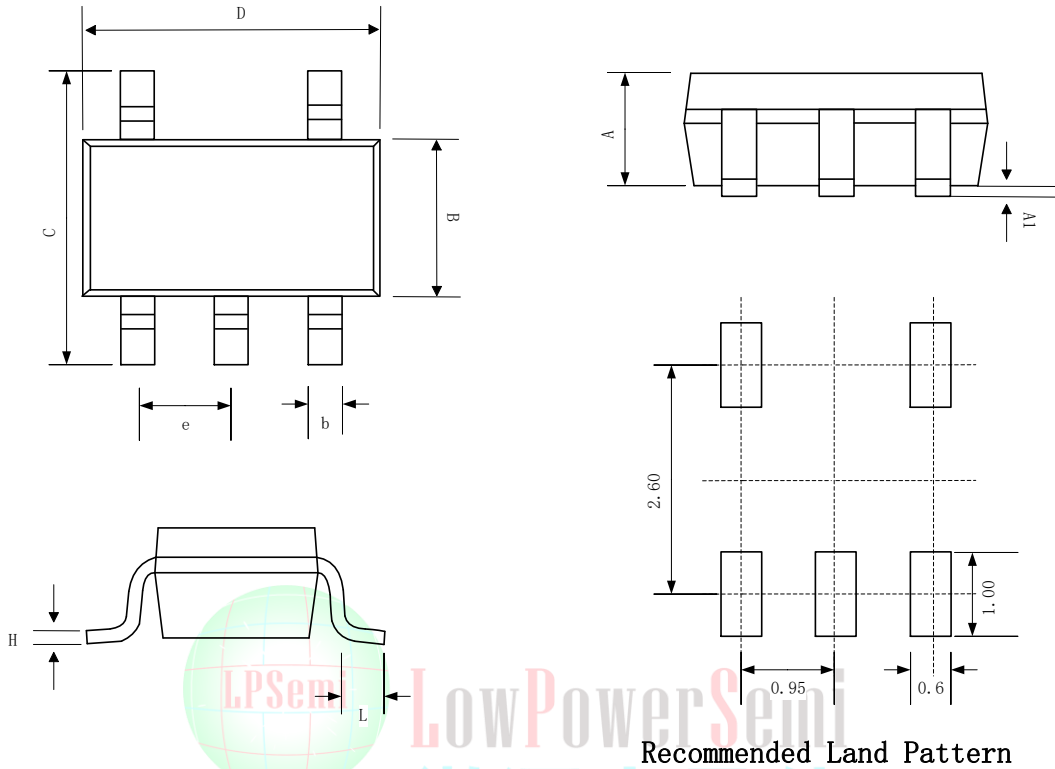
Where $T_J(\text{MAX})$ is the maximum operation junction temperature 125°C , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3992, where $T_J(\text{MAX})$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT23-5 package is $195^\circ\text{C}/\text{W}$.

$$PD(\text{MAX}) = (125^\circ\text{C} - 25^\circ\text{C}) / 195 = 500\text{mW}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_J(\text{MAX})$ and thermal resistance θ_{JA} .

Packaging Information

SOT23-5

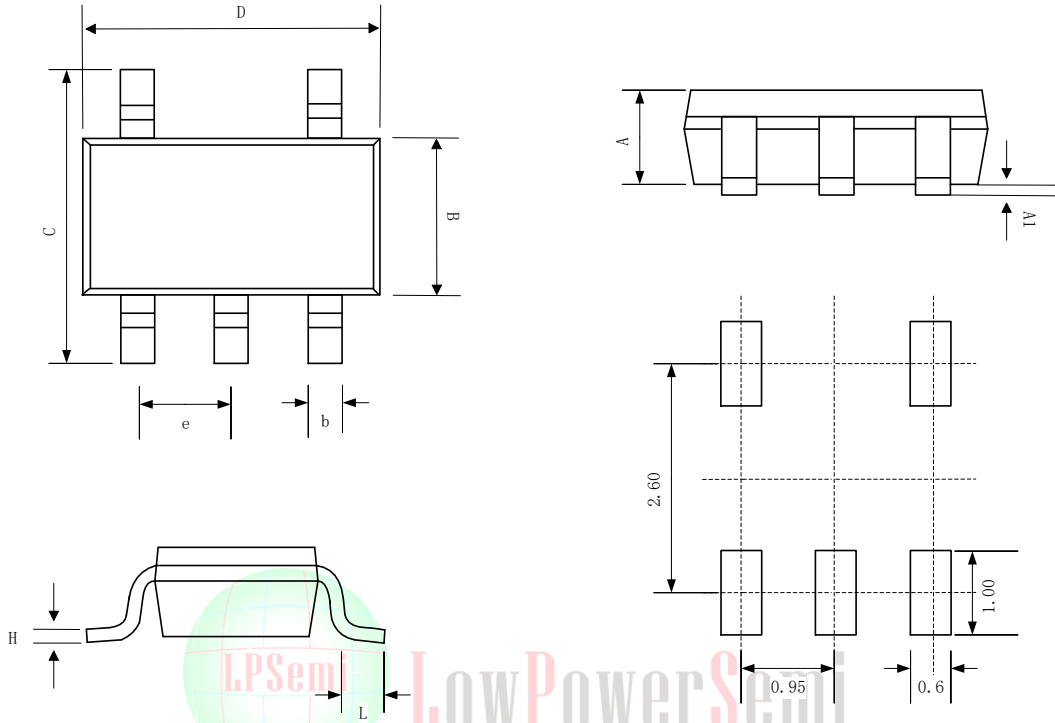


Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610



TSOT23-5

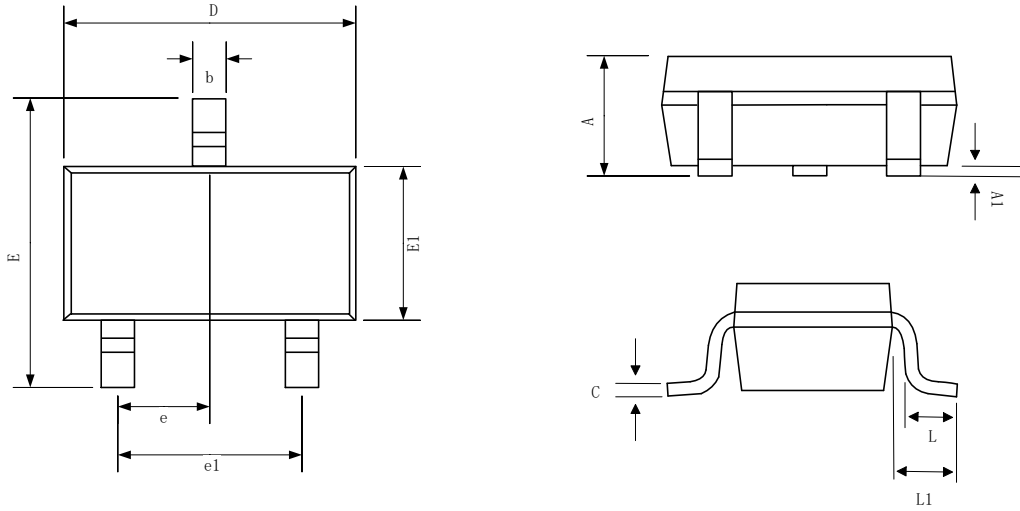


Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.00
A1	0.00	0.05	0.15
B	1.40	1.60	1.80
b	0.28	0.35	0.56
C	2.59	2.80	3.00
D	2.69	2.92	3.12
e	0.95 BSC		
H	0.08	0.15	0.25
L	0.30	0.45	0.61



SOT23-3



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.000	1.150	1.330
A1	0.000	0.050	0.130
b	0.300	0.380	0.450
c	0.110	0.150	0.190
D	2.820	2.920	3.020
E	2.600	2.800	3.000
E1	1.400	1.600	1.800
e	0.950BSC		
e1	1.900BSC		
L	0.300	0.450	0.600
L1	0.600REF		

Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100°C	150°C
Temperature Max(T_{SMAX})	150°C	200°C
Time(T_s) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max	3°C/second max
Liquidous temperature(T_L)	183°C	217°C
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5°C of the specified classification temperature(T_C), see Figure 1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6°C/second max	6°C/second max
Time 25°C to peak temperature	6 minutes max	8 minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1 Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260°C	260°C	260°C
1.6mm~2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

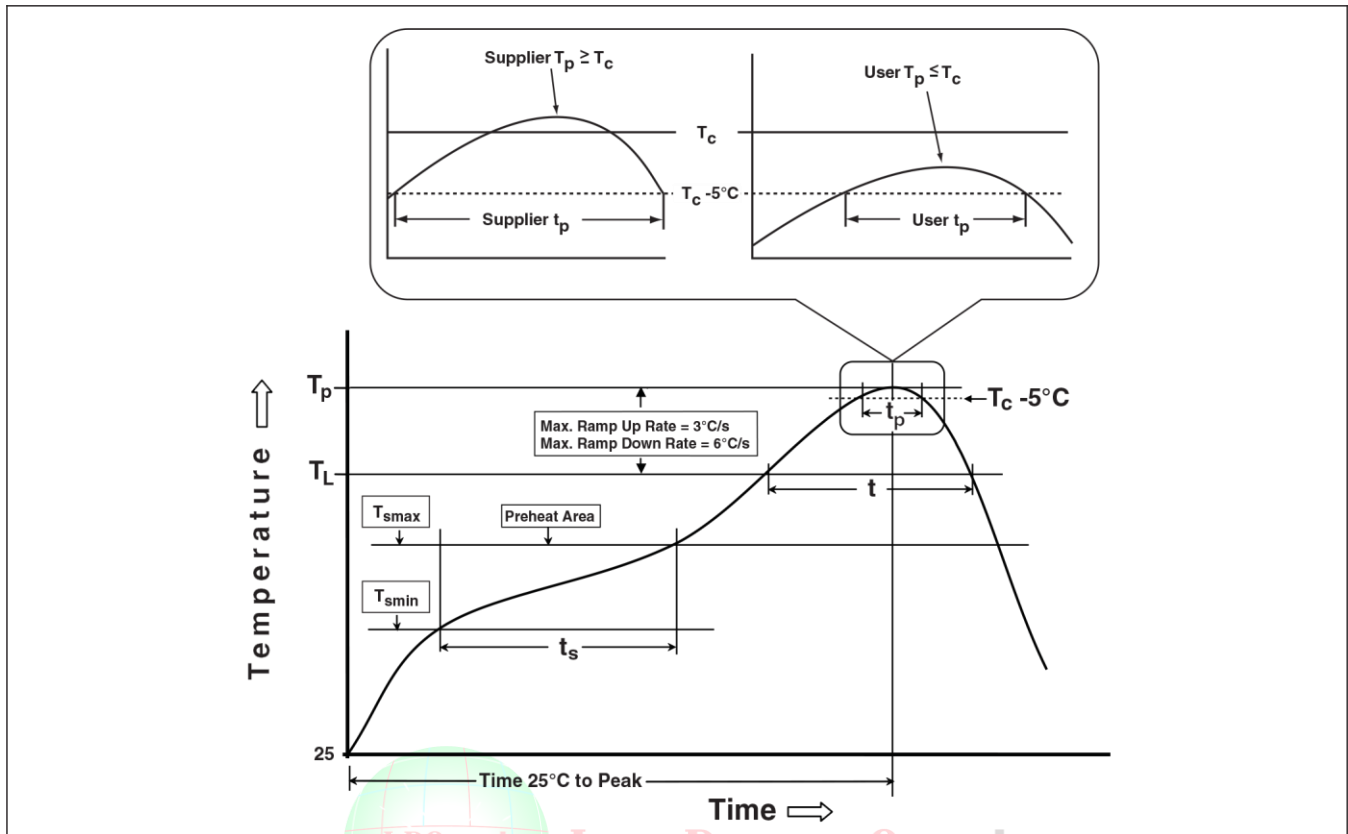


Figure 1 Classification Profile (Not to scale)

Products shipped conform to “RoHS” standards;

Moisture Sensitivity Level: MSL3 (CONDITION: $\leq 30\text{ }^{\circ}\text{C}/60\%\text{RH}$ 、Time control:168 hours) ;