LP54334

32V/3A Synchronous BUCK Switching Converter

Features

- Wide input voltage range: 4.5V – 32V
- Output voltage range: V_{ref} – 13.2V
- High efficiency operation
  - Integrated an 85-mΩ LS-MOSFET and an 130-mΩ HS-MOSFET
  - 88% efficiency at 3A load from 12V to 5V conversion
- Automatic PFM mode to achieve high efficiency at light load
- ±1% Vref accuracy
- Typical 500-kHz switching frequency
- COT control scheme with fast load transient response
- Hiccup protection
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- ESOP-8 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV and TV box
- 12V and 24V Industrial bus applications

General Description

The LP54334 is a synchronous buck converter supporting up to 3A output current. The LP54334 employs an adaptive constant-on-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP54334 supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP54334 integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP54334 also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), output over-voltage protection (OVP), and short circuit protection (SCP).

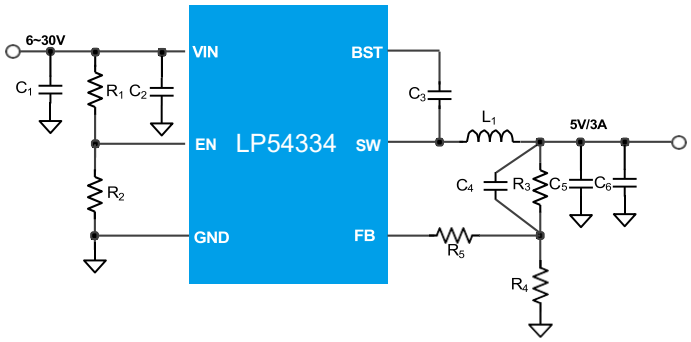
The LP54334 is available in a ESOP-8 package.

Order Information

LP54334 □□ □

- F:Green/Pb-Free
- Package Type
- SP: ESOP

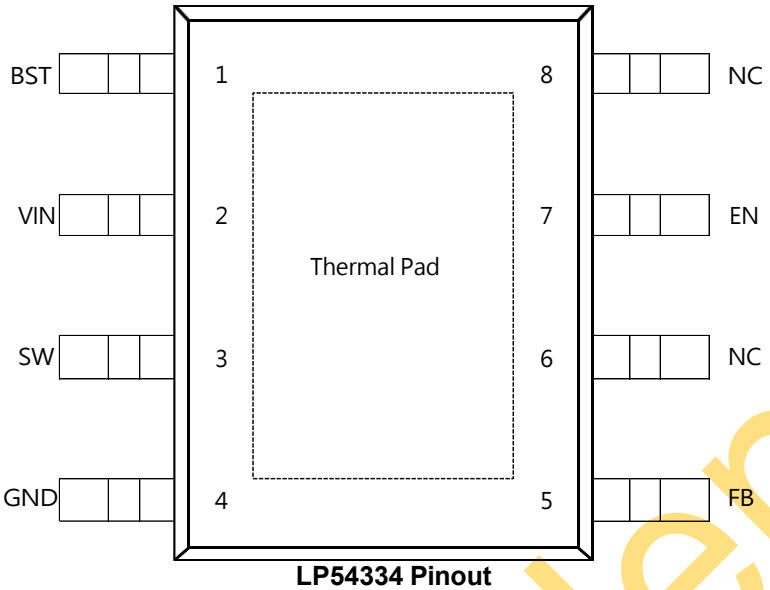
Typical Application Circuit



Device Information

Part Number	Top Marking	Fsw	Operation Mode	MSL	Shipping
LP54334SPF	LPS LP54334 YWX	500kHz	PFM	LEVEL 3	4K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers. **MSL: Moisture Sensitivity Level according to JEDEC Standard.**					

Pin Diagram



LP54334 Pinout

Pin Description

Pin #	Name	Description
1	BST	Bootstrap pin. Power supply for high-side MOSFET gate driver. A 0.1-μF capacitor must be connected between this pin and SW pin.
2	VIN	IC power supply input.
3	SW	The switching node of the converter.
4	GND	Power ground of the IC.
5	FB	Feedback pin. Use a resistor divider to set the desired output voltage.
6	NC	No connection inside.
7	EN	Enable input. This pin can be used to control the system power sequence as well.
8	NC	No connection inside.
Thermal Pad		Connect to GND pin for good power dissipation.

Absolute Maximum Ratings (Note)

VIN to GND ---------- -0.3V to 34V
SW to GND ---------- -1V to 34V
SW to GND （5ns transient） ---------- -5.5V to 34V
EN to GND ---------- -0.3V to 34V
FB to GND ---------- -0.3V to 6.5V
BST to SW ---------- -0.3V to 5.5V
BST to GND (EN=Low) ---------- -0.3V to 34V
BST to GND (EN=High) ---------- -0.3V to 38V
Junction Temperature Range (T_J) ---------- -40°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
CDM (Charged-device Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 63°C/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VIN	Input voltage	4.5		32	V
VOUT	Output voltage	V_{ref}		13.2	V
L	Inductor	0.7		13	μH
T_A	Ambient temperature range	-40		85	°C
C_{IN}	Input decoupling capacitor,25V rating or higher	4.7		100	μF
C_{OUT}	Output capacitor,10V rating or higher	10		100	μF

Electrical Characteristics

(The specifications are measured under conditions V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_R}	Input under voltage lockout threshold	V_{IN} rising threshold		4.2	4.5	V
V_{ULVO_H}	UVLO hysteresis	V_{IN} falling threshold		0.2		V
I_{q_VIN}	Input quiescent current	No switching, EN=3V, FB=1.0V		300		μA
I_{SD}	Shutdown current	EN=0V, V_{IN} = 12V		4.5		μA
BUCK CONVERTER						
I_{LIM}	Low-side valley current limit	T_A=25°C	2.6	3.6		A
V_{ref}	Reference voltage	T_A=25°C,	0.792	0.8	0.808	V
R_{dson_HS}	High-side FET on resistance	V_{IN}=12V		130		mΩ
R_{dson_LS}	Low-side FET on resistance	V_{IN}=12V		85		mΩ
F_{sw}	Switching frequency			500		kHz
$t_{on\text{-}min}$	Minimum on-time[1]			50		ns
$t_{off\text{-}min}$	Minimum off-time[1]	V_{FB}=V_{ref} - 0.2V		100		ns
$t_{on\text{-}hiccup}$	Hiccup on time[1]			1		ms
$t_{off\text{-}hiccup}$	Hiccup waiting time[1]			10		ms
t_d	EN delay time[1]	From EN high to first switching		250		μs
t_{ss}	Soft-start time[1]	From first switching to 95%Vref		600		μs
T_{jsd}	Thermal shutdown threshold	Rising threshold		160		°C
	Thermal shutdown threshold	Falling threshold		135		°C
I_{leak_FB}	FB pin leakage current			0.01		μA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN LOGIC						
V_H	EN pin logic high threshold	EN Rising threshold	1.14	1.2	1.26	V
V_{hys}	EN pin threshold hysteresis			0.1		V
	EN pin internal pull-down resistance			1000		kΩ
OUTPUT OVP						
V_{OVP_rise}	OVP threshold	VOUT rising edge, reference to Vref	108	110	112	%
V_{OVP_fall}	OVP hysteresis	VOUT falling edge, reference to Vref		105		%

[1]: Not production tested. Guaranteed by design.

Typical Characteristics

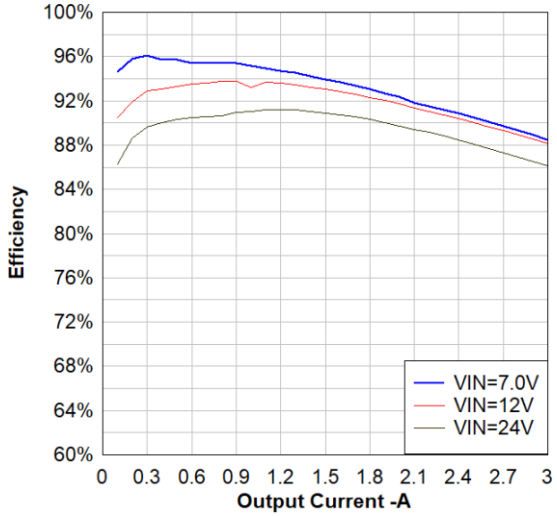


Figure 1. V_{OUT}=5.0V, Efficiency, L=4.7-μH

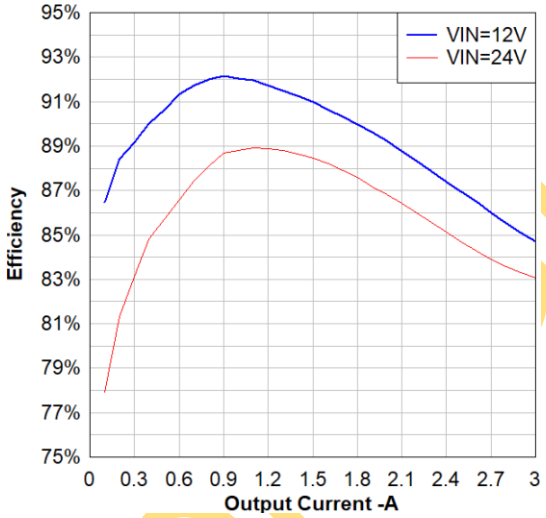


Figure 2. V_{OUT}=3.3V, Efficiency, L=4.7-μH

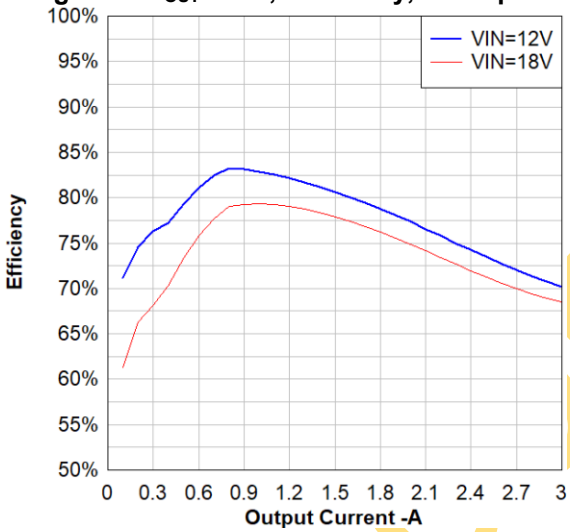


Figure 3. V_{OUT}=1.2V, Efficiency, L=2.2-μH

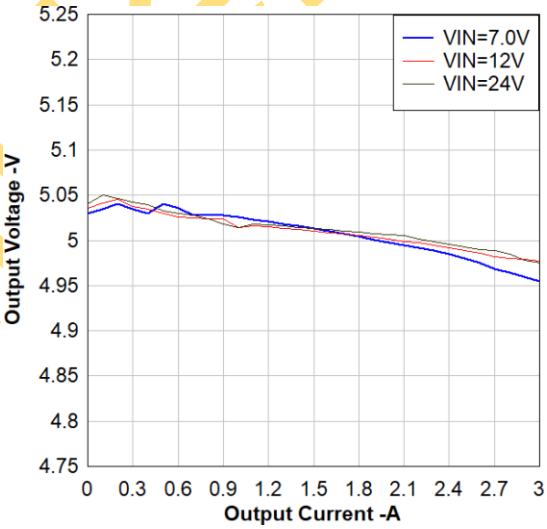


Figure 4. VOUT=5V, Regulation, L=4.7-μH

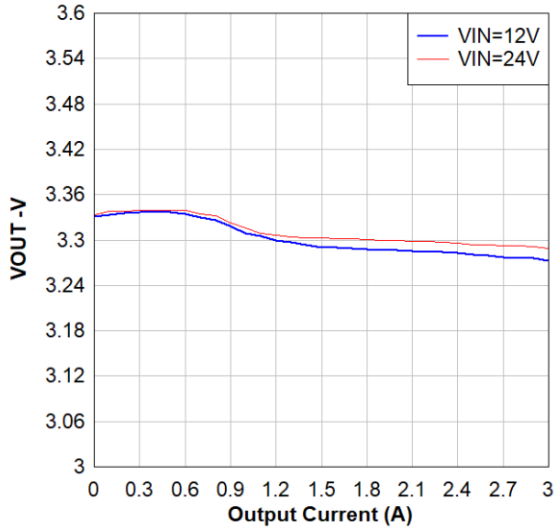


Figure 5. V_{OUT}=3.3V, Regulation, L=4.7-μH

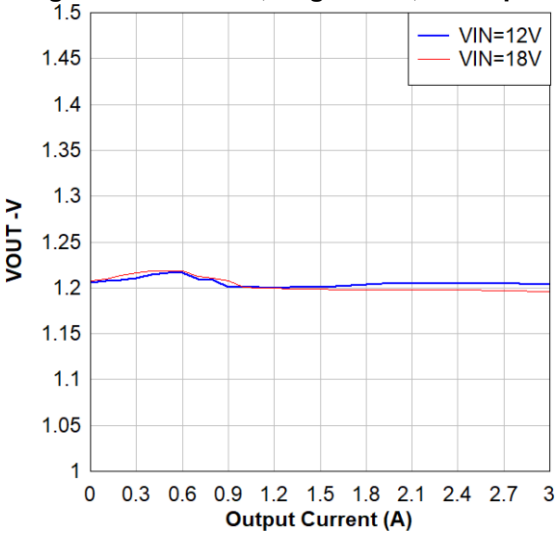


Figure 6. V_{OUT}=1.2V, Regulation, L=2.2-μH

Application Waveforms (Vin=12V, L=4.7μH, Cout=22μF*2)

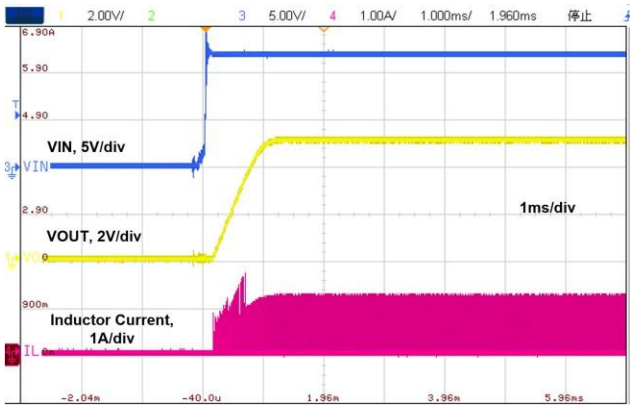


Figure 7. Startup by VIN, 50Ω load

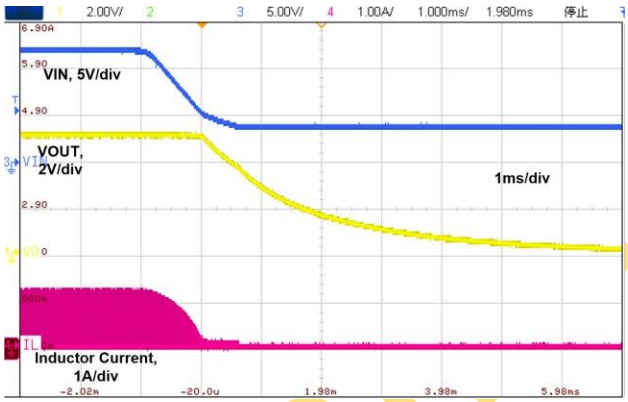


Figure 8. Shutdown by VIN, 50Ω load

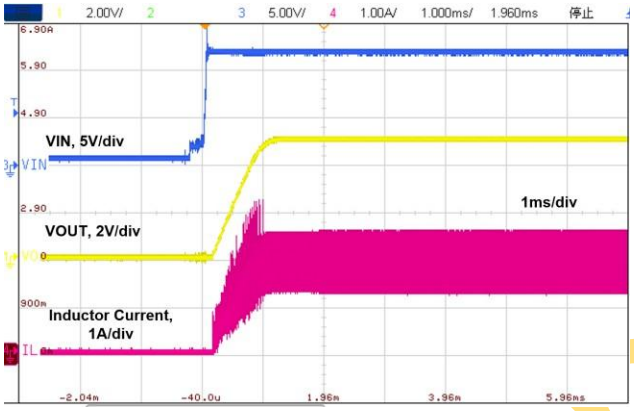


Figure 9. Startup by VIN, 2.5Ω load

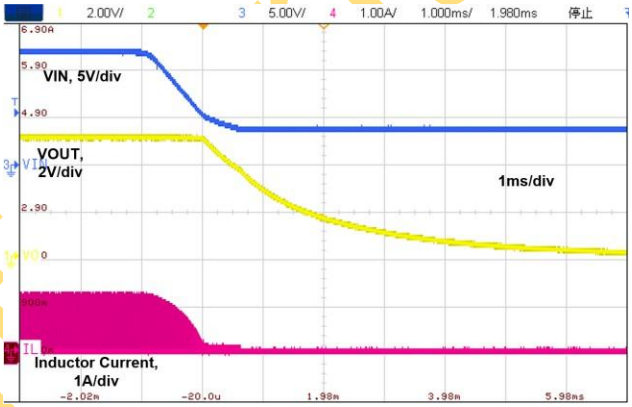


Figure 10. Shutdown by VIN, 2.5Ω load

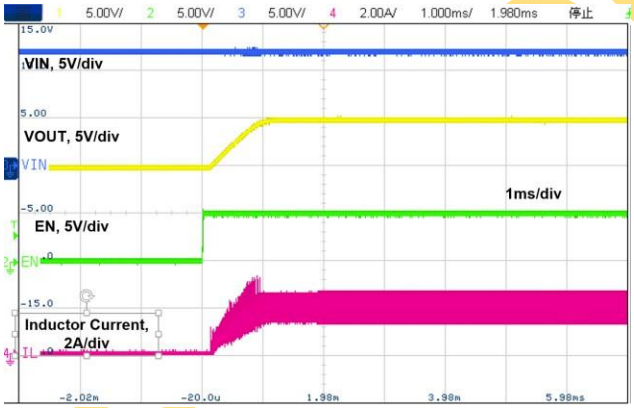


Figure 11. Startup by EN, 2.5Ω load

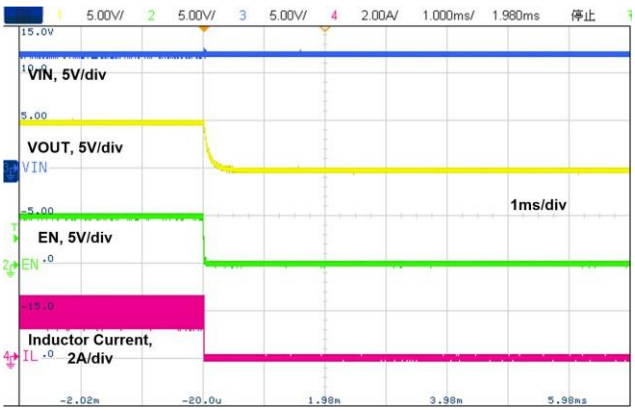


Figure 12. Shutdown by EN, 2.5Ω load

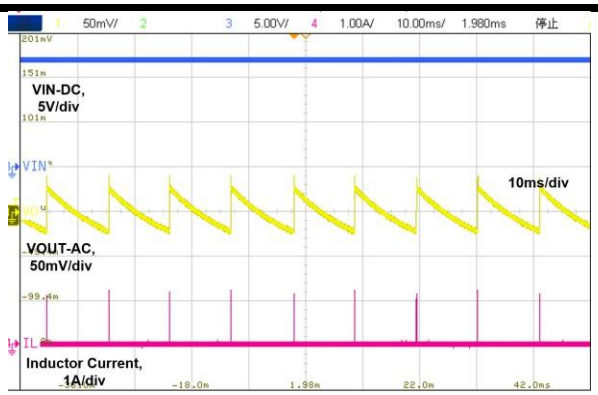


Figure 13. Switching Waveform, 0A load

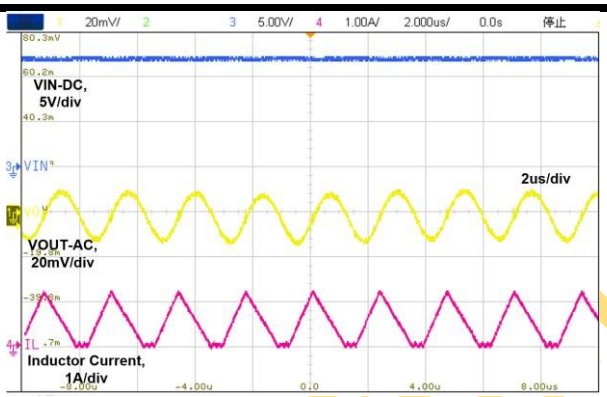


Figure 14. Switching Waveform, 500mA load

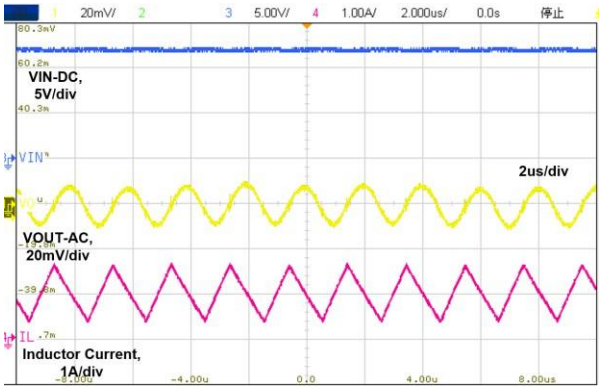


Figure 15. Switching Waveform, 1A load

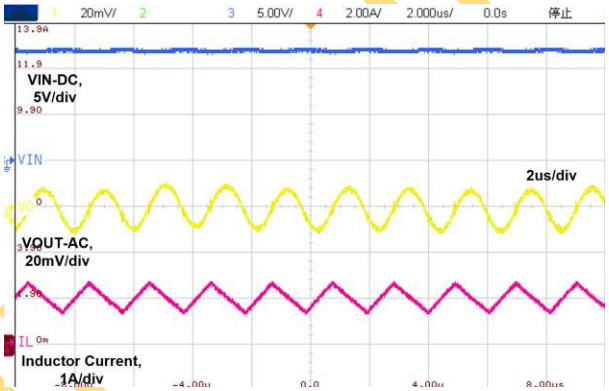


Figure 16. Switching Waveform, 2A load

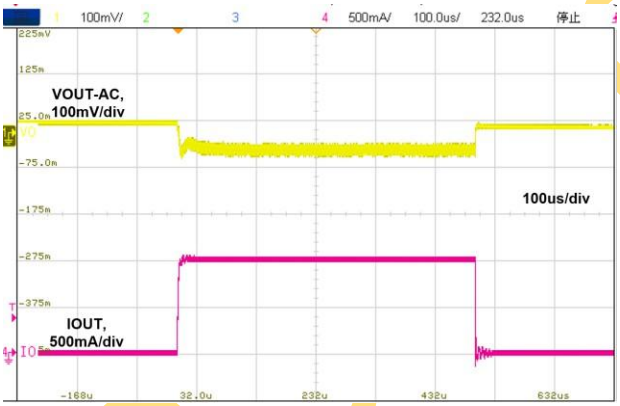


Figure 17. Load Transient, 0A-1A-0A

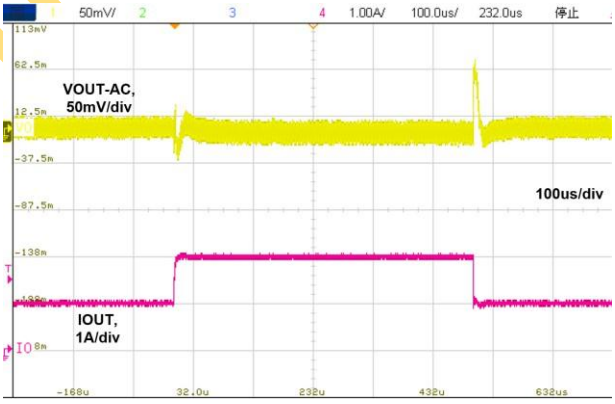


Figure 18. Load Transient, 1A-2A-1A

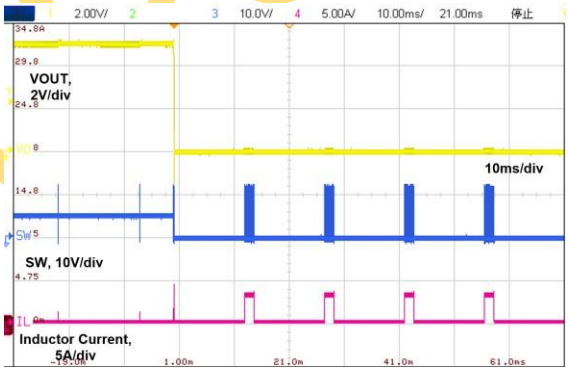


Figure 19. SCP Happen, Hiccup Operation

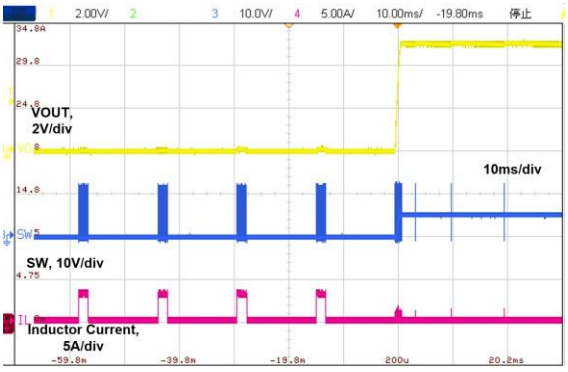
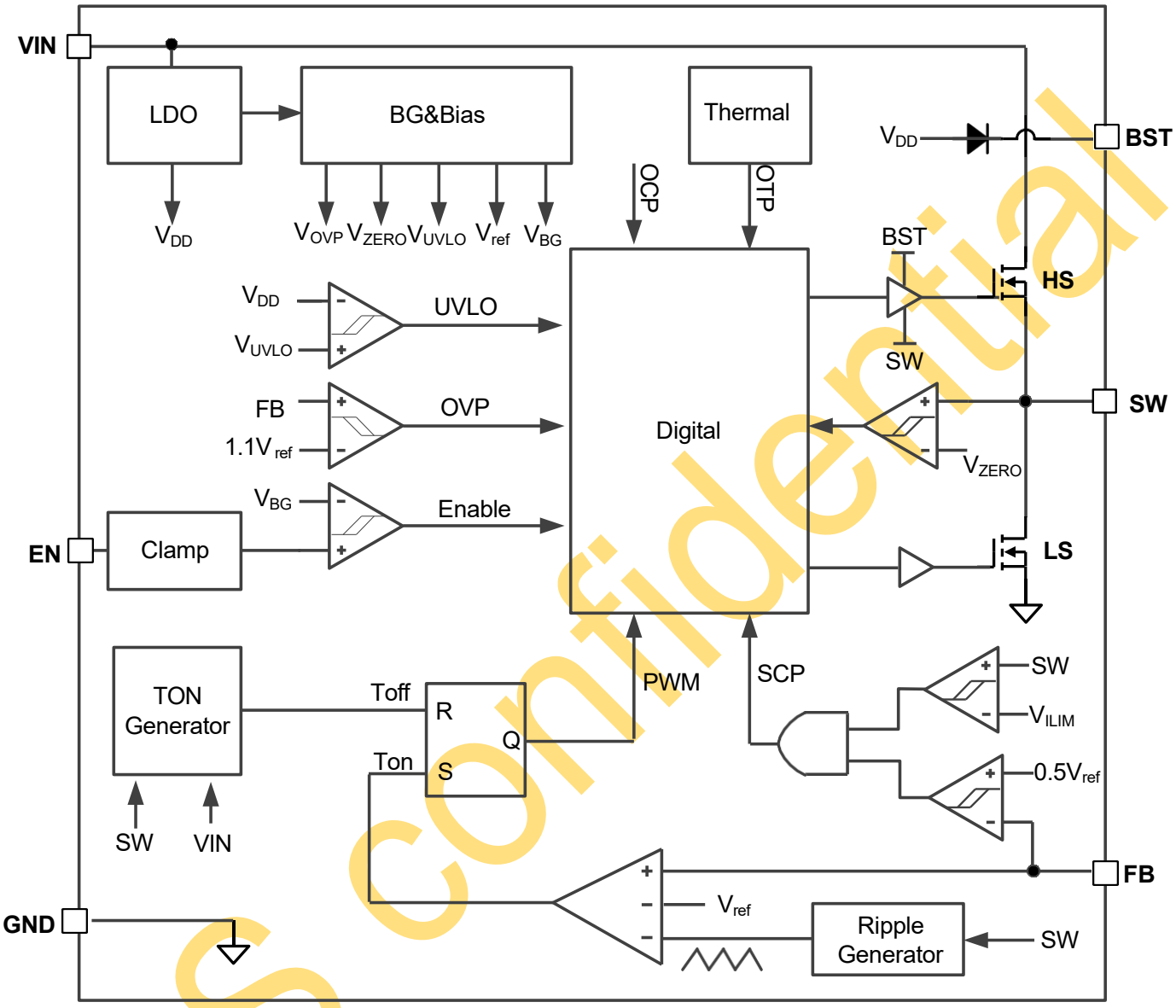


Figure 20. SCP Recovery

Functional Block Diagram



Detailed Description

Overview

The LP54334 is a 3A synchronous buck converter, supporting 4.5-32V input operating voltage range. The adaptive COT control scheme enables fast transient respond and minimizes the output capacitance. The LP54334X supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP54334 automatically transfers between PFM and PWM according to the output current.

Under Voltage Lockout (UVLO)

When the input voltage VIN is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP54334 can be enabled by the EN pin.

EN Control

The EN pin can be used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP54334 enables all the internal circuits, delays for 260us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1000kΩ pull-down resistor to ground.

Soft-start

The LP54334 integrates soft-start function with a typical time of 600us (t_{ss}) . After passing the UVLO threshold and enabled by the EN pin with the 250us delay(t_d), the internal reference voltage ramps from zero to the V_{ref} in 600us and the output voltage ramps up accordingly.

Figure 21. Soft Start Sequence

Constant-ON Time (COT) Control Scheme

The LP54334 integrates the COT control scheme for pseudo-fixed- frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal on-time (TON) generator block monitors the FB-pin voltage and turns on the high-side MOSFET to start a switching cycle, when the FB-pin voltage drops to an internal reference voltage Vref. Then the internal circuits start to calculate the on-time of the high-side MOSFET, which is proportional to the input voltage and inversely proportional to the output voltage. Once the on-time is finished, the TOFF generator turns off the high-side MOSFET and turns on the low-side MOSFET.

PFM Operation

The LP54334 is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

Bootstrap Capacitor

The LP54334 integrates two N-MOSFET to achieve high efficiency. The high-side MOSFET is powered by the bootstrap capacitor C_{BST}, which is between the BST pin and SW pin. A 1Ω~100Ω resistor is recommended in series with the bootstrap capacitor C_{BST} to reduce the switching noise and improve the system reliability.

Over Current Protection and Short Circuit Protection

The LP54334X protects an over current situation by limiting the inductor valley current. The current of low-side MOSFET is monitored all the time to sense the inductor valley current when the LP54334 is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit pluses a half of the inductor ripple current.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to 50% of the Vref for 1-ms, the LP54334 shuts down. The LP54334 will restart after a typical 10-ms hiccup waiting time. If the SCP condition still holds after soft-start, the LP54334 shutdown again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

Output Over-voltage Protection

The LP54334 stops switching immediately when the FB voltage rising above 110%Vref to protect the output capacitor voltage from further increasing. The LP54334 recovers switching when the FB voltage falls below 105%Vref.

Thermal Protection

The LP54334 has a thermal protection function. The device will shut down when the internal temperature is higher than 160°C and will restart after the temperature drops below 135°C.

Application Information

Design Requirements

The table 1 shows the design parameters for a typical 5V output voltage in the IPC application.

Table 1 Design Parameters

Parameter	Target
Input voltage range	9~30V
Output voltage	5.0V
Transient ripple	±200mV
Operating frequency	500kHz

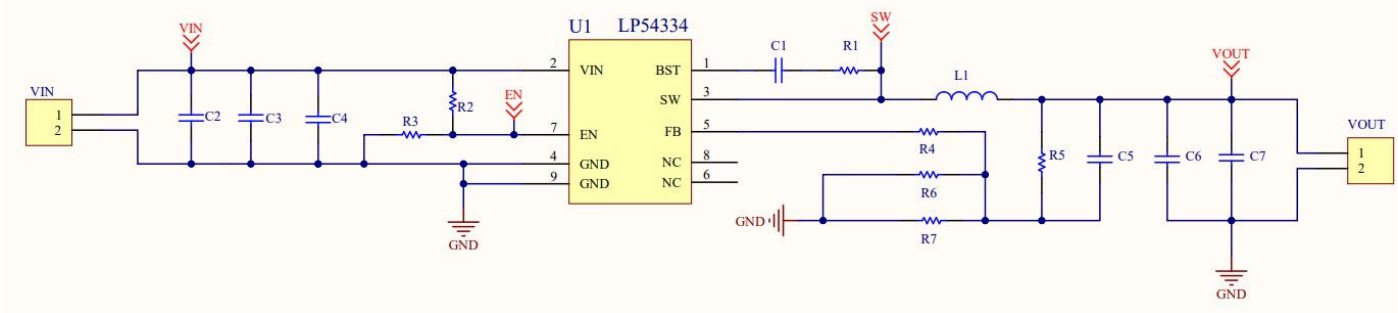


Figure 22. Typical schematic

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1\right) * V_{ref}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.8V.

For better accuracy, the R_{DOWN} is recommended to be lower than 10kΩ to ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current.

For a 5.0V-output application, a 10kΩ R_{DOWN} is selected and the R_{UP} is 53kΩ.

A resistor with higher than 100Ω but lower than 1kΩ should be placed between the resistor divider and FB pin if a C_{ff} capacitor is soldered to reduce the switching noise influence.

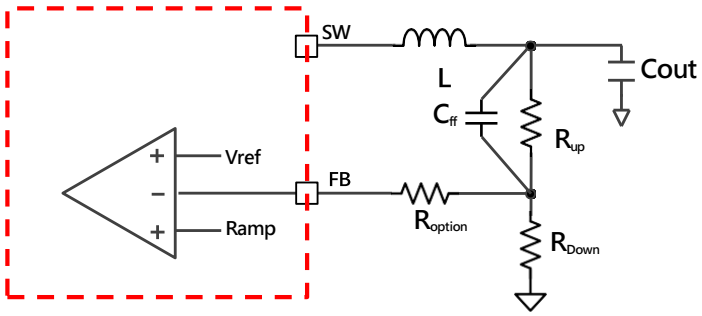


Figure 23. FB connection

EN Design

The LP54334 allows the user to design a precise VIN voltage to enable the converter during power on. The startup sequence can be designed by adjusting the resistor divider of R_{UP_EN} and R_{DOWN_EN} with the equation below,

$$V_{EN} = \frac{1000k\Omega // R_{DOWN\_EN}}{R_{UP\_EN} + 1000k\Omega // R_{DOWN\_EN}} * VIN$$

where V_{EN} is the EN rising threshold voltage at which the converter is enabled, which is 1.2V typically. A 47pF-1nF capacitor is recommend to be soldered in parallel with the R_{EN_DOWN} to avoid the high-frequency noise influence from the switching node.

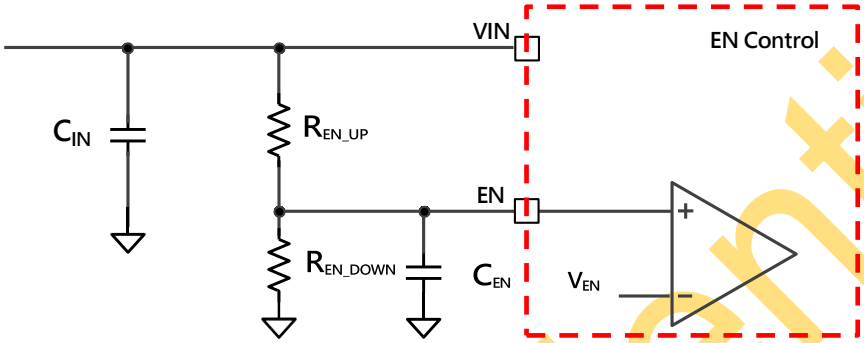


Figure 24. EN connection

Inductor and Output Capacitor Setting

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * Fsw} * \frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.
For a typical 12V input voltage and 5V output voltage, a low DCR value, 6.8-μH or 4.7-μH inductor is recommended. The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor C_{FF} can be selected to improve the transient behavior. The typical capacitance can be 10-100pF. For this design, 10V, X5R, 22μF capacitors (GRM21BR61A226ME51) from Murata are soldered at the VOUT to GND. Multiple capacitors should be soldered to keep the system stable because of the voltage rating effect.

Table 2 Recommend R/L/C values

Vout	Inductor-L	Cout	R_{UP}	R_{DOWN}	R_{option}	C_{ff}
1.2V	1.5μH/3.3μH	22μF*1	5 kΩ	10 kΩ	0-1 kΩ	NA
3.3V	2.2μH~6.8μH	22μF*2	31.5 kΩ	10 kΩ	0.1-1 kΩ	22-100pF
5.0V	4.7μH ~10μH	22μF*2	53 kΩ	10 kΩ	0.1-1 kΩ	47-100pF

Bootstrap capacitor

Bootstrap capacitor is critical to drive the high-side MOSFET. A 0.1-μF ceramic capacitor is needed to supply power for the high-side driver. The capacitor should be at least 10V. The resistor R_1 is used to adjust the driver speed to optimize the EMI performance and reliability.

Input capacitor

A typical 22-μF ceramic capacitor is needed to serve as the bulk capacitor at the VIN pin. An additional 0.1-μF is strongly recommended to provide additional high frequency filtering and should be placed to the VIN pin and GND as close as possible.

PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place the input capacitors (C_4, 0603 or 0402 size) as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane, this is the most critical path and should have the highest priority when designing PCB floorplan. To minimize the switching noise, the SW pin is recommended to layout at the bottom layer by vias.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Minimize parasitic capacitance from this area to any other trace or plane.
- R_1 is reserved to slow down the switching speed for noise sensitive applications.

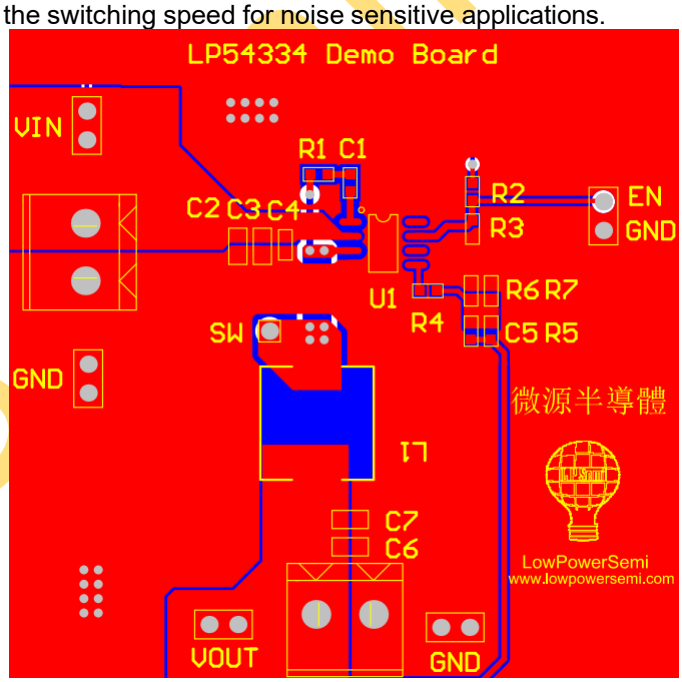


Figure 25. Layout example (TOP)

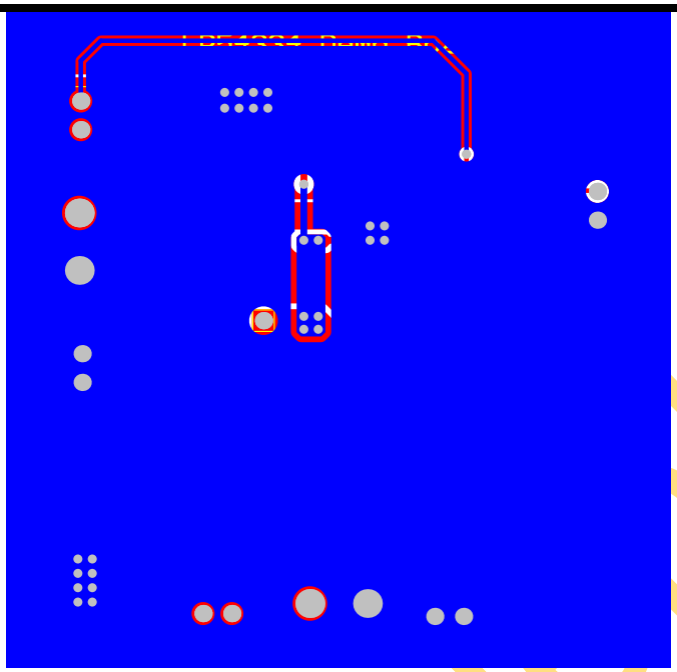
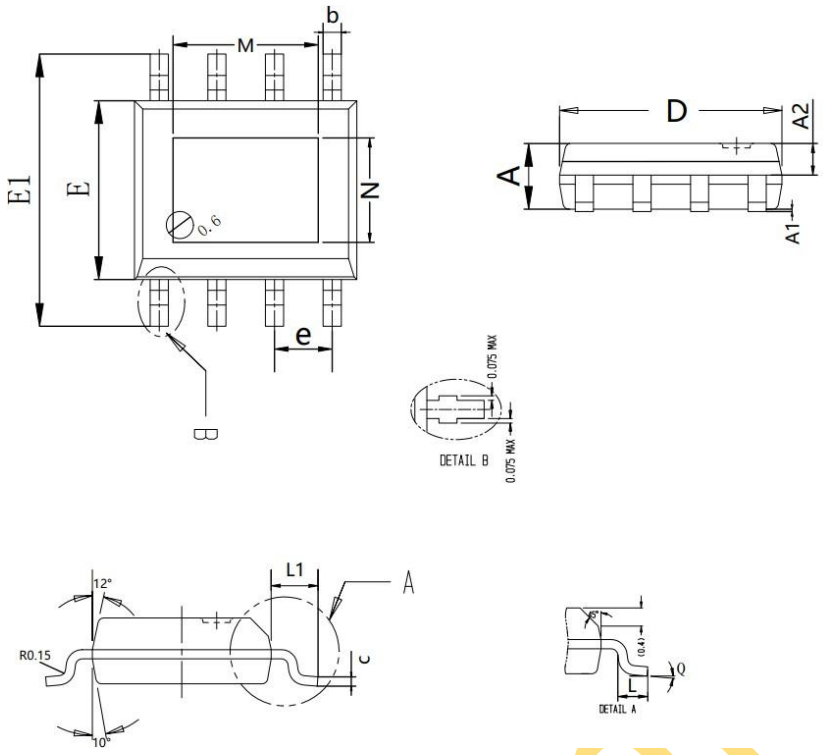


Figure 26. Layout example (BOTTOM)

Packaging Information

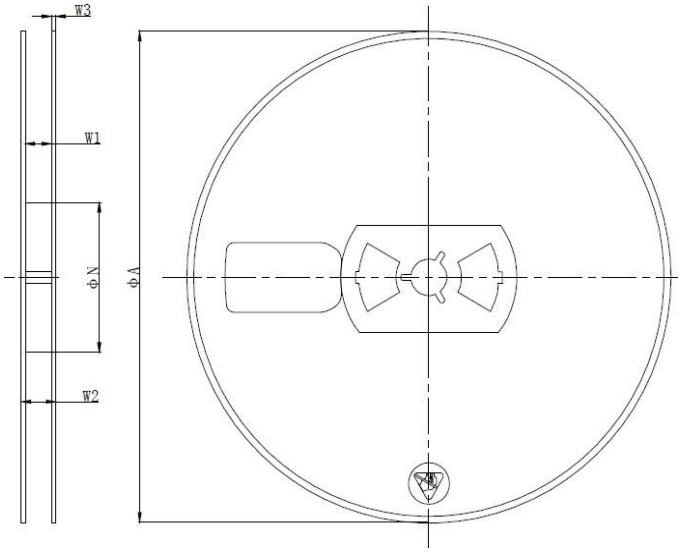
ESOP-8 package



COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	MID	MAX
A	1.35	1.45	1.55
A1	0.00	0.05	0.10
A2	0.65	0.70	0.75
b	0.35	0.40	0.45
c	0.18	0.20	0.22
D	4.70	4.90	5.10
e	-	1.27TYP	-
E1	5.80	6.00	6.20
E	3.80	3.90	4.00
L	0.40	0.60	0.80
Q	0°	/	8°
M	3.10	3.20	3.30
N	2.20	2.30	2.40
L1	1.05REF		

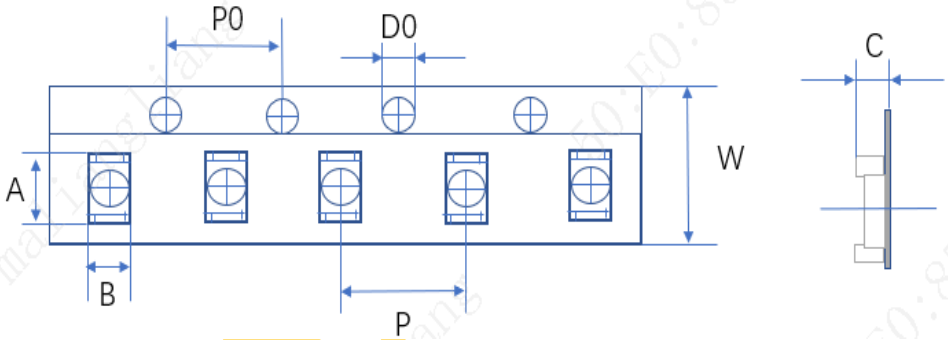
Tape and Reel information

REEL DIMENSIONS (Unit: mm)



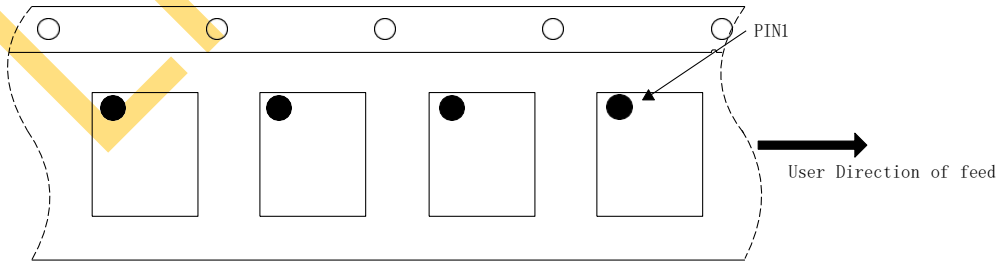
ΦA	W2
329±4	17±2

TAPE DIMENSIONS (Unit: mm)



口袋宽度A		口袋长度B		编带孔中心间距P0		IC中心间距P		孔径D0		编带宽度W		编带厚度C	
尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差
6.60	±0.40	5.50	±0.40	4.00	±0.20	8.00	±0.20	1.50	±0.20	12.00	0.3/-0.1	2.10	±0.20

PIN1 AND TAPE FEEDING DIRECTION



Revision History

Revision	Date	Change Description
Rev 1p0	12/10/2022	First release version
Rev 1p1	10/30/2023	Update PCB layout and recommended values of feedback circuit
Rev 1p2	12/18/2023	1: VIN, SW, BST voltage range update 2: R_{option} description update 3: Add tape and reel information
Rev 1p3	01/03/2024	Device information update
Rev 1p4	08/28/2025	1. Consider the case when the current flows through the body diode of the LS-FET, update the absolute maximum rating of 'SW to GND'. 2. Consider the pin contact inductance and the internal parasitic inductance of the IC, update the absolute maximum rating of 'SW to GND (5ns transient)', which will not affect the reliable operation of the IC.