Features

- Input Supply Range : 2.6V ~ 5.5V
- IIC Interface
- Current Mode Sync. Boost Converter for AVDD
  Programmable Switching Frequency
  7V to 13.5V Programmable Output
  Fast Transient Response to Pulsed Load
  High-Accuracy Output Voltage(±2%)
  High Efficiency up to 88%
- Sync. Buck Converter for V_{CORE}/V_{IO}
  Programmable Switching Frequency
  0.8V to 2.0V Programmable Output for VCORE
  1.0V to 2.8V Programmable Output for VIO
  Fast Transient Response to Pulsed Load
  High-Accuracy Output Voltage(±1.5%)
  High Efficiency up to 90%
- Sync. Boost Converter for V_{GH}
  Programmable Switching Frequency
  10V to 34V Programmable Output
  Fast Transient Response to Pulsed Load
  High-Accuracy Output Voltage(±4%)
  High Efficiency up to 80%
- Negative Charge-pump regulator for V_{GL}
  Programmable Switching Frequency
  -4.4V to -13.0V Programmable Output
  High-Accuracy Output Voltage(±3%)
- Low Dropout Regulator
  1.0V to 2.8V Programmable Output
- Programmable VCOM,GMA1/2,HAVDD Voltage
- Programmable Voltage Detector
- OCP/OTP/OVP/UVP/SCP Protection Function
- Compact Package: QFN3.5X3.5-28

Applications

- NB PCs
- Table PCs

General Description

The LP6263A includes 2-wire IIC interface, two synchronous boost converters for AVDD and VGH, two buck converters for Vcore and VIO, one charge pump for VGL, one LDO regulator, one voltage detector, one high-speed amplifier for programmable VCOM, one high-speed operation amplifier for HAVDD, two high-speed operation amplifiers for GMA, for active-matrix,thin-film transistor, liquid-crystal displays (LCDs).

One synchronous boost converter (AVDD) provides the regulated supply voltage for the panel source driver ICs. The converter is a high-frequency current-mode regulator with integrated MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while achieving efficiencies over 88%.

One synchronous boost converter (VGH) provides the regulated supply voltage for the panel gate driver ICs. The converter is a high-frequency current-mode regulator with integrated MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while achieving efficiencies over 80%.

Two buck converters (Vcore and VIO) provides the regulated supply voltage for T-con. The converter is a high-frequency current-mode regulator with an integrated MOSFET that allows the use of ultra-small inductors and ceramic capacitors.

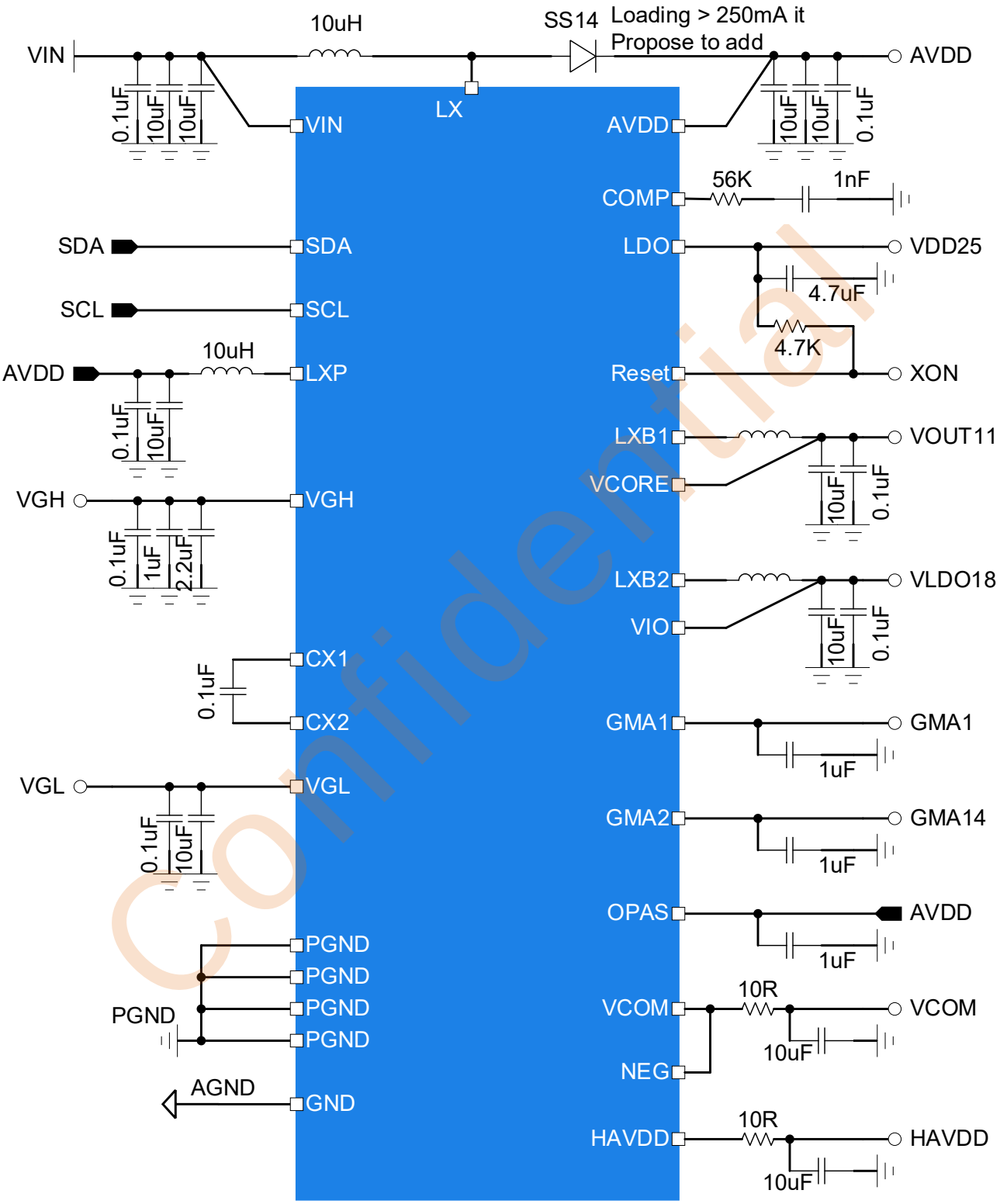
The VGL charge pump provides regulated TFT gate-off supply.

Order Information

LP6263A □ □ □

- F:Green
- Package Type
  QV:QFN3.5X3.5-28

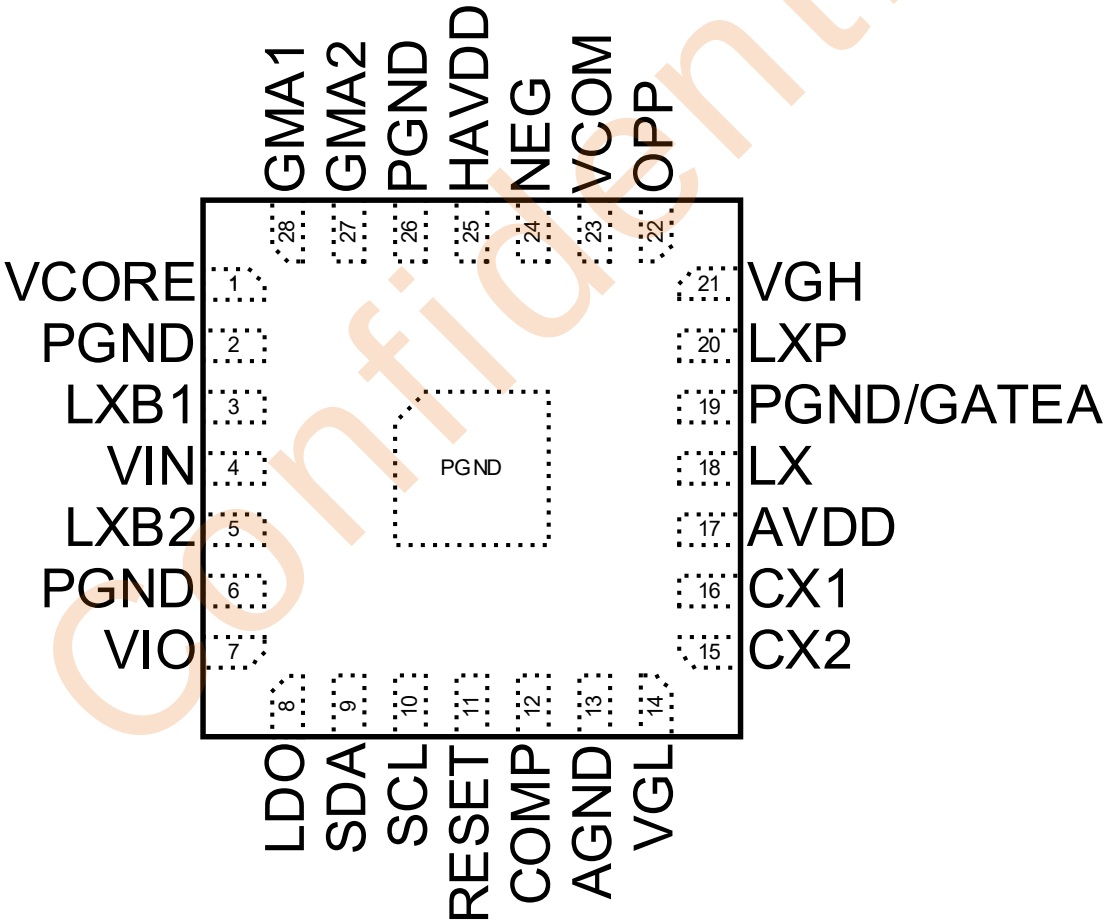
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6263AQVF	LPS LP6263A YWX	MSL3	QFN3.5X3.5-28	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Lot Serial Code.				

Pin Diagram



LP6263AQVF

Pin Description

LP6263A

Pin#	Name	Description
1	VCORE	VCORE output feedback
2	PGND	Power ground
3	LXB1	VCORE buck switching node.
4	VIN	IC supply voltage input.
5	LXB2	VIO buck switching node.
6	PGND	Power ground
7	VIO	VIO output feedback.
8	LDO	LDO Output
9	SDA	Serial data input/output for IIC interface.
10	SCL	Clock Input for IIC interface.
11	RESET	Output of voltage detector function.
12	COMP	AVDD Boost converter compensation input.
13	AGND	Analog Ground.
14	VGL	VGL charge pump output voltage.
15	CX2	VGL charge pump flying cap node2.
16	CX1	VGL charge pump flying cap node1.
17	AVDD	Output of AVDD Boost Converter
18	LX	Switching Pin of AVDD Boost Converter
19	PGND/ GATEA	Internal Power NMOSFET: Can be connected to PGND External Power NMOSFET: Gate Driver pin
20	LXP	VGH switching node.
21	VGH	Output of VGH Boost Converter
22	OPP	Power of OP amplifier
23	VCOM	VCOM OP-amp output.
24	NEG	VCOM OP Feedback Input.
25	HAVDD	HAVDD output pin.
26	PGND	Power ground
27	GMA2	Gamma2 output pin.
28	GMA1	Gamma1 output pin.
29	EAP	GND

Absolute Maximum Ratings (Note1)

VIN to PGND ---------- -0.3V to +6V
SDA,SCL to AGND ---------- -0.3V to VIN+0.3V
PGND,AGND to GND ---------- -0.3V to +0.3V
COMP,RESET to GND ---------- -0.3V to +6V
AVDD,LX to GND ---------- -0.3V to +14.5V
LXB1,LXB2 to GND ---------- -0.3V to +6V
VGH,VGHLX to PGND ---------- -0.3V to 35V
VCORE,VIO,VLDO to PGND ---------- -0.3V to +6V
VOPP to PGND ---------- -0.3V to(V_{AVDD}+0.3V)
VCOM,NEG to PGND ---------- -0.3V to(V_{AVDD}+0.3V)
HAVDD to PGND ---------- -0.3V to(V_{AVDD}+0.3V)
CX1 to PGND ---------- -0.3V to +14.5V
VGL,CX2 to PGND ---------- -14.5V to 0.3V
GMA1,GMA2 to PGND ---------- -0.3V to (V_{AVDD}+0.3V)

Note1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2KV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ---------- 150℃
Operating Junction Temperature Range (TJ) ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	VIN Supply Range		2.6	3.3	5.0	V
A_{VDD}	AVDD Output Range	Step:100mV	7	8.5	13.5	V
V_{CORE1}	VCORE Output Range1	Step:50mV (reg0x12[7]=0)	0.8	1.2	2.0	V
V_{CORE2}	VCORE Output Range2	Step:20mV (reg0x12[7]=1)	0.62		1.1	V
V_{IO}	VIO Output Range	Step:50mV	1.0	1.8	2.8	V
V_{LDO}	LDO Output Range	Step:100mV	1.8	2.5	2.8	V
V_{GH}	VGH Output Range	Step:1V	10	15	34	V
V_{GL}	VGL Output Range	Step:100mV	-13.0	-8.0	-4.4	V
V_{COM}	VCOM Output Range	Step:20mV	1.5		6.2	V
V_{PVCOM}	PVCOM Output Range	Step:10mV	VCOM-10mV*64	0	VCOM+10mV*63	
HAVDD	HALF AVDD Range	Step:50mV	3.5		6.5	V
GMA1	GMA1 Output Range	Step:50mV	AVDD-1		AVDD-0.1	V
GMA2	GMA2 Output Range	Step:50mV	0.1		1	V

Electrical Characteristics

(V_{IN} = 3.3V, V_{AVDD}=9V,V_{CORE}=1.2V,V_{IO}=1.8V,V_{LDO}=2.5V,V_{GH}=22V,V_{GL}=-8V, TA= 25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VIN	Input Voltage Range		2.6	3.3	5.0	V
VIN_{UVLO_R}	VIN UVLO Rising		2.2	2.3	2.4	V
VIN_{UVLO_F}	VIN UVLO Falling		1.9	2.0	2.1	V
VIN_{Write}	Write to MTP minimum Input voltage		2.6			V
VIN_{IQ}	VIN Pin Quiescent Current	All regulator enabled Non-switching.		2	4	mA
VIN_{IQ}	VIN Pin Quiescent Current	All regulator enabled. Switching.		8	12	mA
VIN_IQ	VIN Total Supply Current	All regulator enabled. No load		15	20	mA
VIN_{FAULT}	Duration to Trigger Fault Condition	Boost,Buck,Charge pumps		60		mS
TSD	Thermal Shutdown Protection			150		℃
THYS	Thermal Shutdown Protection Hysteresis			20		℃
AVDD Boost Converter						
VAVDD	AVDD Output Voltage Range	Programmable	7	---	13.5	V
$AVDD_{BIT}$	AVDD Output Voltage Bit		---	7	---	Bits
$AVDD_{RES}$	AVDD Output Voltage Resolution		---	0.1	---	V
$AVDD_{ACC}$	AVDD Output Voltage Accuracy	AVDD = 9V	-2	---	+2	%
F_{OSC}	AVDD Switching Frequency	Accuracy ±20%	600	715	1225	kHz
$FOSC_{BIT}$	AVDD Switching Frequency Bit		---	3	---	Bits
MAX_{DUTY}	AVDD Maximum Duty Cycle		86	90	94	%
	AVDD Line Regulation	V_{IN} = 2.6V to 5.0V	-0.3	---	+0.3	%/V
R_{DS_NMOS}	AVDD LX NMOS ON-Resistance		---	150	250	mΩ
I_{LEAK}	AVDD LX Leakage Current	V_{LX} = 14.5V	---	1	5	uA
I_C	AVDD LX Current Limit	By 0x0E[6:5]=00h Accuracy: ±20%	0.4	0.5	0.6	A
I_C	AVDD LX Current Limit	By 0x0E[6:5]=01h Accuracy: ±20%	0.8	1.0	1.2	A
I_C	AVDD LX Current Limit	By 0x0E[6:5]=10h Accuracy: ±20%	1.2	1.5	1.8	A
I_C	AVDD LX Current Limit	By 0x0E[6:5]=11h Accuracy: ±20%	1.6	2.0	2.4	A
R_{DS_PMOS}	AVDD LX PMOS ON-Resistance		---	300	450	mΩ
LX_{SR}	AVDD LX Switch ON / OFF Slew Rate	2 Bits, falling Edge	FF		SS	nS

Electrical Characteristics

(VIN = 3.3V, VAVDD=9V,VCORE=1.2V,VIO=1.8V,VLDO=2.5V,VGH=22V,VGL=-8V, TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	AVDD Output Current Ability		250	---	---	mA
	AVDD Current Limit Bit		---	2	---	Bits
	AVDD Current Limit Resolution		---	0.5	---	A
$AVDD_{SS}$	AVDD Soft-start time	Programmable	5	---	20	ms
	AVDD Soft-start time Bit		---	2	---	Bits
	AVDD Soft-start time Resolution		---	5	---	ms
	AVDD Startup Delay Time Range	3 Bits, Step = 5ms	0	---	35	ms
	AVDD UVP Level	VAVDD falling edge	75	80	85	%
	AVDD SCP Level	VAVDD falling edge	25	30	35	%
VGH Boost Converter						
VGH	VGH Output Voltage Range		10		34	V
VGH_{BIT}	VGH Output Voltage Bit			5		Bits
	VGH Output Voltage Resolution			1		V
	VGH Output Voltage Accuracy	VGH=20V	-4		+4	%
F_{OSC}	VGH Switching Frequency	Programmable (Accuracy ±20%)	600	715	1225	KHz
	VGH Switching Frequency Bit			3		Bits
	VGH Maximum Duty Cycle		86	90	94	%
	VGH Line Regulation	VIN=2.6V to 5.0V	-0.3		+0.3	%/V
$VGHLX_{leak}$	VGH LXP Leakage Current	VLXP=35V		1	20	uA
	VGH LXP Current Limit			0.7		A
	VGH LXP NMOS on-Resistance			1		Ω
	VGH LXP PMOS on-Resistance			2		Ω
	VGH Output Current Ability	VIN=3.3V VGH=22V	30			mA
	VGH Soft-start time	Programmable	2		8	ms
	VGH Soft-start time Bit			2		Bits
	VGH Startup Delay Time Range	3 Bits, Step=5ms	0		35	ms
	VGH UVP Level	VGH falling edge	75	80	85	%
	VGH SCP Level	VGH falling edge	25	30	35	%

Electrical Characteristics

(VIN = 3.3V, VAVDD=9V,VCORE=1.2V,VIO=1.8V,VLDO=2.5V,VGH=22V,VGL=-8V, TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCORE Buck Converter						
VCORE1	VCORE1 Output Voltage Range 1	Programmable	0.8	1.2	2.0	V
	VCORE1 Output Voltage Bit			5		Bits
	VCORE1 Output Voltage Resolution			0.05		V
	VCORE2 Output Voltage Range 2	VCORE_V-reg0x12[7]=1	0.62		1.1	V
	VCORE2 Output Voltage Bit			5		Bits
	VCORE2 Output Voltage Resolution			0.02		V
	VCORE Output Voltage Accuracy	VCORE=1.2V	-1.5		+1.5	%
$VCORE_{FOSC}$	VCORE Switching Frequency	Programmable (Accuracy ±20%)	600	715	1225	KHz
	VCORE Switching Frequency Bit			3		Bits
$VCORE_{LIMIT}$	VCORE LXB1 Current Limit		0.8	1.2		A
R_{DSON}	VCORE LXB1 PMOS on-Resistance			250		mΩ
R_{DSON}	VCORE LXB1 NMOS on-Resistance			100		mΩ
	VCORE LXB1 Maximum Duty Cycle		100			%
	VCORE LXB1 Leakage Current	VLXB1=5.5V VIN=5.5V		1	5	uA
	VCORE Output Current Ability		300			mA
	VCORE Startup Delay Time Range	2 Bits, Step=3ms	0		9	ms
	VCORE LXB1 Switching on/off Slew Rate	2 Bits, Step=TBDns, Adj. Rising edge only	FF		SS	ns
	VCORE UVP Level	VCORE falling edge	75	80	85	%
	VCORE SCP Level	VCORE falling edge	25	30	35	%
VIO Buck Converter						
	VIO Output Voltage Range	Programmable	1.0	1.8	2.8	V
	VIO Output Voltage Bit			6		Bits
	VIO Output Voltage Resolution			0.05		V
	VIO Output Voltage Line Regulation	V_{IN}=2.6V to 5.5V I_O=200mA	-0.25		0.25	%/V
	VIO Output Voltage Load Regulation	V_{IN}=3.3V V_O=1.8V I_O=1 to 400mA	-1		+1	%
	VIO Output Voltage Accuracy	Vo=1.8V	-1.5		+1.5	%
	VIO Switching Frequency	Programmable (Accuracy ±20%)	600	715	1225	KHz
	VIO Switching Frequency Bit			3		Bits
	VIO LXB2 Current Limit		0.8	1.2		A
	VIO LXB2 PMOS on-Resistance			250		mΩ
	VIO LXB2 NMOS on-Resistance			100		mΩ
	VIO LXB2 Leakage Current	VLXB2=5.5V VIN=5.5V		1	5	uA

Electrical Characteristics

(VIN = 3.3V, VAVDD=9V,VCORE=1.2V,VIO=1.8V,VLDO=2.5V,VGH=22V,VGL=-8V, TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO Buck Converter						
	VIO Output Current Ability		250			mA
	VIO Soft-start Time			3		ms
	VIO Startup Delay Time Range	2 Bits, Step=3ms	0		9	ms
	VIO LXB2 Switch on/off Slew Rate	2 Bits, Step=TBDns Adj. Rising edge only	FF		SS	ns
	VIO UVP Level	VIO falling edge	75	80	85	%
	VIO SCP Level	VIO falling edge	25	30	35	%
VGL Charge Pump Regulator						
	VGL Output Voltage Range	Programmable	-13		-4.4	V
	VGL Output Voltage Bit			7		Bits
	VGL Output Voltage Resolution			-0.1		V
	VGL Output Voltage Accuracy	VGL=-8V	-2		+2	%
	VGL Operation Frequency	Programmable (Accuracy ±20%)	0.5* FAVDD		FAVDD	KHz
	VGL Operation Frequency Bit			1		bit
	VGL Line Regulation	V_{AVDD}=8V to 11V V_{GL}=-6V I_O=10mA	-0.3		+0.3	%/V
	VGL Load Regulation	V_{AVDD}=9.2V V_{GL}=-6V,I_O=1 to 30mA	-1		+1	%
	VGL Output Current Ability	V_{AVDD}-V_{GL}=-0.5V Fly.Cap=0.1uF	20			mA
	VGL PMOS on-Resistance			2	4	Ω
	VGL NMOS on-Resistance			1.5	3	Ω
	VGL Soft-start Time	Programmable	2		8	ms
	VGL Soft-start Time Bit			2		Bits
	VGL Soft-start time Resolution			2		ms
	VGL Startup Delay Time	3 Bits, Step=5ms	0		35	ms
	VGL UVP Level	VGL rising edge	75	80	85	%
	VGL SCP Level	VGL rising edge	25	30	35	%
Voltage Detector --- RESET						
	RESET Detect Voltage Range		2.0	2.2	2.7	V
	RESET Detect Voltage Bit			3		Bits
	RESET Detect Voltage Resolution			0.1		V
	RESET Detect Voltage Accuracy		-2		+2	%
	RESET Startup Delay time	4 Bits, Step=5ms	0		75	ms

Electrical Characteristics

(VIN = 3.3V, VAVDD=9V,VCORE=1.2V,VIO=1.8V,VLDO=2.5V,VGH=22V,VGL=-8V, TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HAVDD Amplifier Output						
V_{OPP}	OPP Input Voltage Range	V_{OPP}	7		13.5	V
I_Q	OPP Quiescent Current	I_{QOPP}		2.5		mA
	HAVDD Output Voltage Range	Programmable	3.5		6.5	V
	HAVDD Output Voltage Bit			6		Bits
	HAVDD Output Voltage Resolution			0.05		V
	HAVDD Output Current Ability		±40	±75		mA
	HAVDD Short-circuit Current	Source	200	250		mA
	HAVDD Short-circuit Current	Sink	-200	-250		mA
	HAVDD Output Slew Rate		8	12		V/us
	HAVDD -3dB Bandwidth	R_L=10KΩ, C_L=10pF		10		MHz
	HAVDD Gain-Bandwidth Product	R_L=10KΩ, C_L=10pF		5		MHz
	HAVDD Integral Nonlinearity Error	HAVDD=3.5V to 6.5V		2		LSB
	HAVDD Differential Nonlinearity Error	HAVDD=3.5V to 6.5V		1		LSB
VCOM Amplifier Output						
V_{OPP}	OPP Input Voltage Range	V_{OPP}	7		13.5	V
	VCOM Output Voltage Range		1.5		6.2	V
	VCOM NEG Input offset Voltage		-15		+15	mV
	VCOM NEG Input Bias Current		-100		+100	nA
	VCOM Soft-start time			3		ms
	VCOM Output Voltage Swing High	I_{OUT}=100uA	AVDD-0.03	AVDD-0.05		V
		I_{OUT}=75mA	AVDD-1.9	AVDD-1.5		V
	VCOM Output Voltage Swing Low	I_{OUT}=-100uA		GND+0.05	GND+0.03	V
		I_{OUT}=-75mA		GND+1.5	GND+1.9	V
	VCOM Output Short-circuit Current	Source	+100	+150		mA
		Sink	-100	-150		mA
	VCOM Output Current Ability	V_{AVDD}/2, V_{OS}<10mV,Source	45	75		mA
		V_{AVDD}/2, V_{OS}<10mV,Sink	-45	-75		mA
	VCOM Output Slew Rate			12		V/us
	VCOM -3dB Bandwidth	R_L=10KΩ, C_L=10pF		10		MHz
	VCOM Gain-Bandwidth Product	R_L=10KΩ, C_L=10pF		5		MHz
	VCOM Integral Non-Linearity	Unit Gain V_{COM}=1.5V to 6.2V		2		LSB
	VCOM Differential Non-Linearity	Unit Gain V_{COM}=1.5V to 6.2V		1		LSB
	VCOM Startup Delay time	5 Bits, Step=5ms	0		155	ms

Electrical Characteristics

(VIN = 3.3V, VAVDD=9V,VCORE=1.2V,VIO=1.8V,VLDO=2.5V,VGH=22V,VGL=-8V, TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable VCOM Calibrator						
PVCOM	PVCOM Resolution			7		Bits
	PVCOM Integral Non-Linearity Error			1		LSB
	PVCOM Differential Non-Linearity Error			1		LSB
Low Dropout Linear Regulator						
	LDO Output Voltage Range		1.8		2.8	V
	LDO Output Voltage Bit			4		Bits
	LDO Output Voltage Resolution			0.1		V
	LDO Output Voltage Accuracy	V_{LDO}=2.5V	-1		+1	%
	LDO Line Regulation	V_{IN}=2.7V to 5.5V I_O=100mA	-0.5		+0.5	%
	LDO Load Regulation	V_{IN}=3.3V,V_{LDO}=2.5V I_O=1 to 100mA	-0.5		+0.5	%
	LDO Output Dropout Voltage	V_{IN}=3.3V, I_{OUT}=200mA		0.2		V
	LDO Output Current Limit		150	200		mA
	LDO Output Current Ability		150			mA
	LDO Soft-start time			1		ms
	LDO Startup Delay Time Range	2 Bits, Step=3ms	0		9	ms
	LDO UVP Level	VLDO falling edge	55	60	65	%
	LDO SCP Level	VLDO falling edge	25	30	35	%
GMA1/GMA2 Output						
	GMA1 Output Voltage Range		AVDD-1		AVDD-0.1	V
	GMA2 Output Voltage Range		0.1		1	V
	GMA1/GMA2 Output Current Ability		1			mA
	GMA1/GMA2 Short-circuit Current		5			mA
	GMA1 Output Voltage Swing High	I_{OUT}=1mA	AVDD-0.2			V
	GMA2 Output Voltage Swing Low	I_{OUT}=1mA			GND+0.2	V
	GMA1/GMA2 Output Resolution			5		Bits
	GMA Integral Non-linearity Error			2		LSB
	GMA Differential Non-linearity Error			1		LSB

Electrical Characteristics

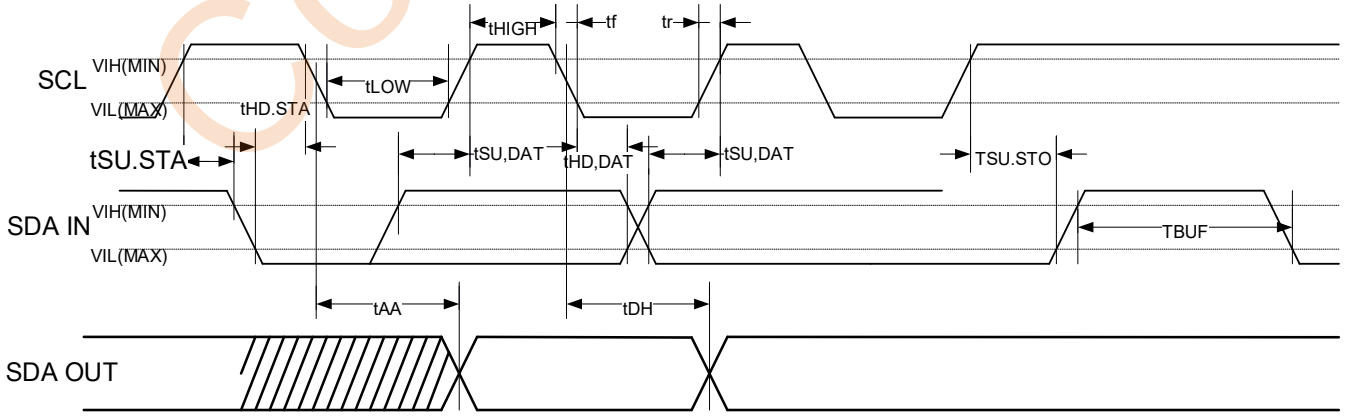
(VIN = 3.3V, VAVDD=9V,VCORE=1.2V,VIO=1.8V,VLDO=2.5V,VGH=22V,VGL=-8V, TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

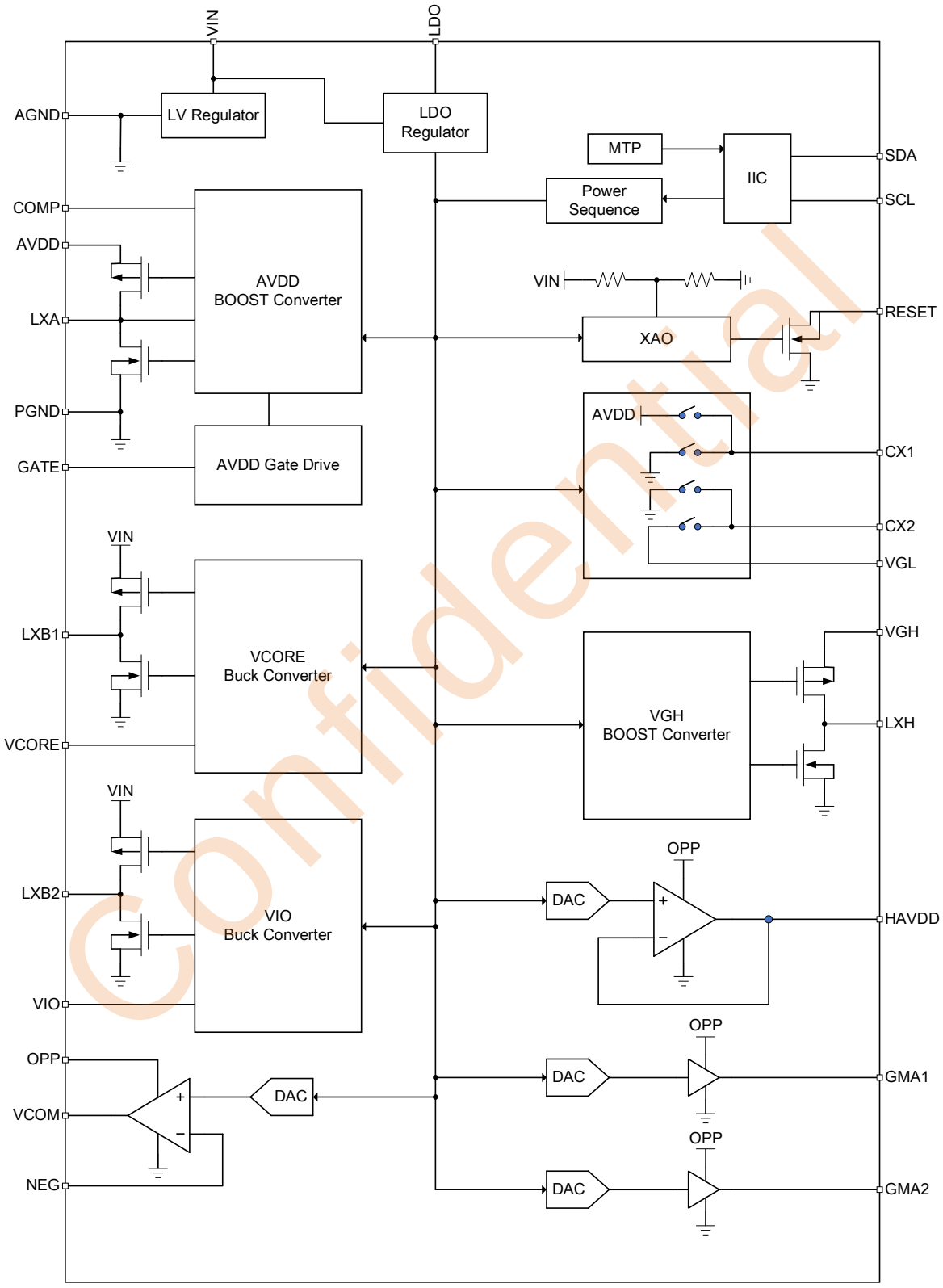
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IIC INTERFACE(SDA,SCL)						
V_{IH}	High Level Input Voltage		1.2	---	---	V
V_{IL}	Low Level Input Voltage		---	---	0.4	V
IIC TIMING CHARCTERISTICS						
f_{SCL}	Serial-Clock Frequency		10	---	1000	KHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		500	---	---	nS
$t_{HD.STA}$	Hold Time(Repeated) START Condition		250	---	---	nS
t_{LOW}	SCL Pulse-Width Low		1300	---	---	nS
t_{HIGH}	SCL Pulse-Width High		600	---	---	nS
$t_{SU.STA}$	Setup Time for a Repeated START Condition		250	---	---	nS
$t_{HD.DAT}$	Data Hold Time		50	---	300	nS
$t_{SU.DAT}$	Data Setup Time		100	---	---	nS
t_R	SDA and SCL Receiving Rise Time	CB is IN pF	20+ 0.1CB	---	200	nS
t_F	SDA and SCL Receiving Fall Time	CB is IN pF	20+ 0.1CB	---	200	nS
CIN	SDA and SCL Input Capacitance			5		pF
$t_{SU.STO}$	Setup Time for STOP Condition		600	---	---	nS
t_{AA}	Clock Low to Data Out Valid		100	---	900	nS

I2C Serial-Interface

The LP6263A communicates through an industry standard 2-wire I2C serial-interface to receive data in slave mode. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. A master device, usually a microcontroller or a digital signal processor, controls the bus.



Functional Block Diagram



Typical Application Circuit_1

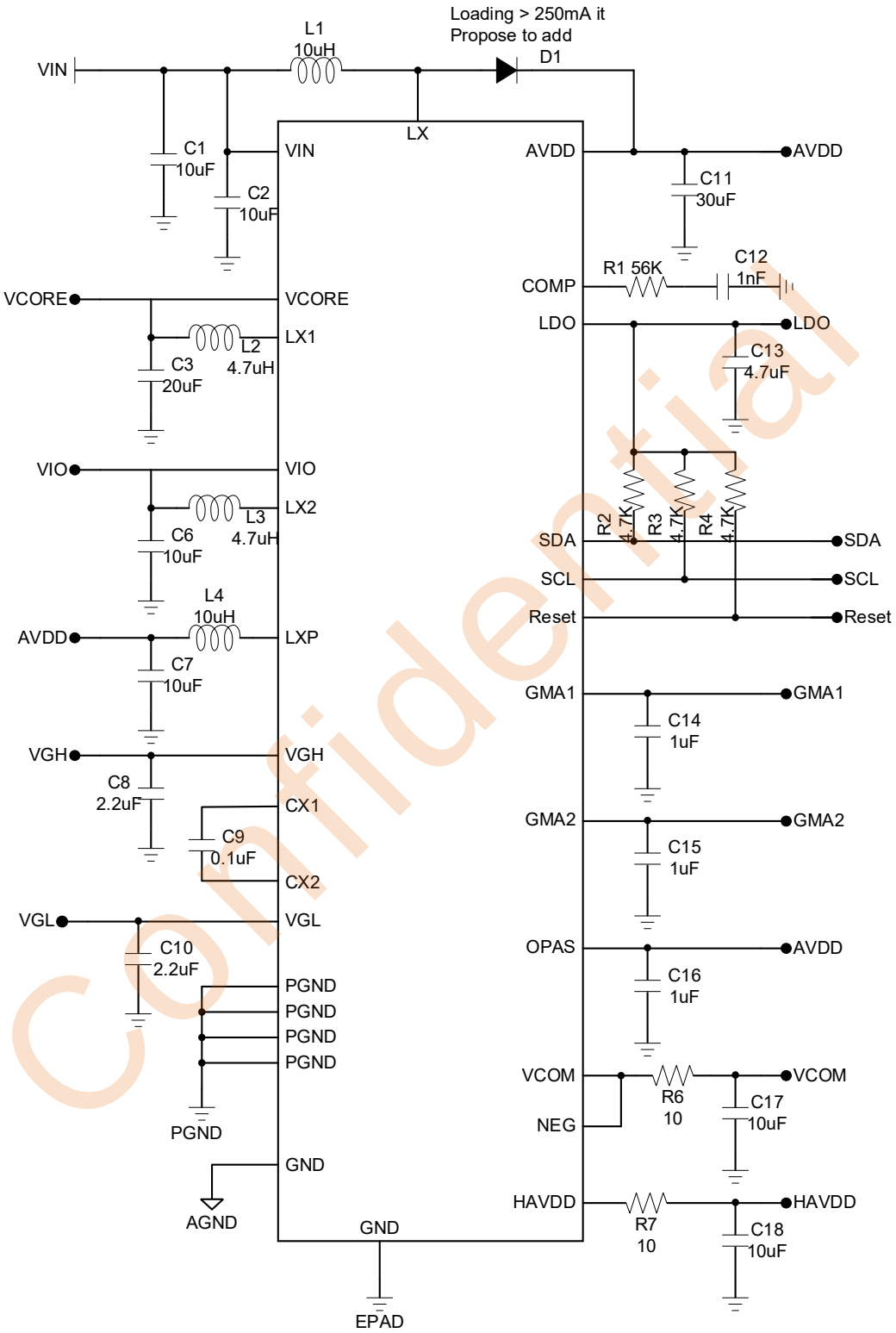


Figure 1 The Application Circuit for VGL Internal
|VGL=-8V|<|AVDD=9V|
Register 0x10 Bit[7:6]=00h (VGL>-(AVDD-0.5V)

Typical Application Circuit_2

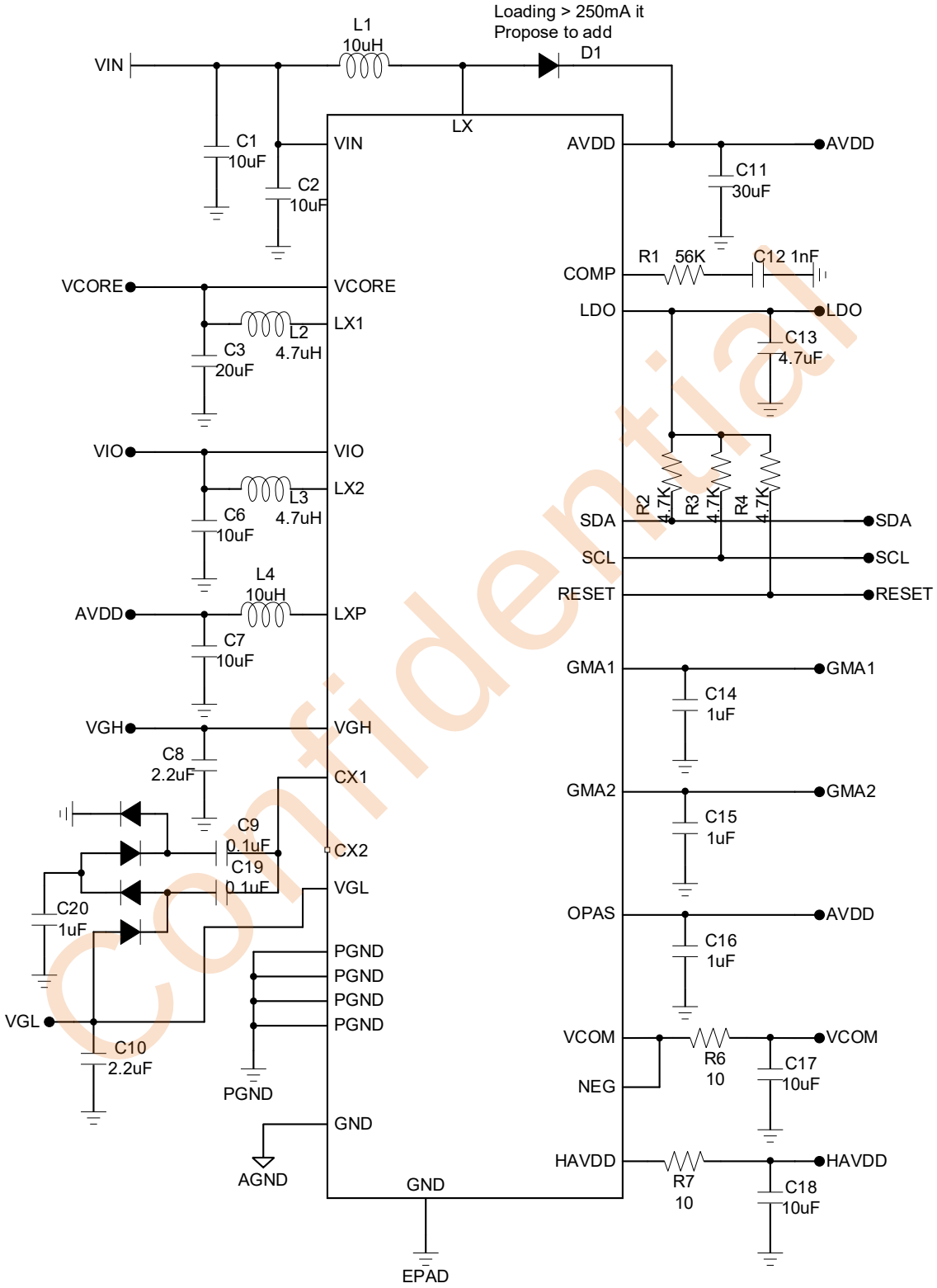


Figure 2 The Application Circuit for VGL Internal
|VGL=-12V|>|AVDD=9V| & |VGL|<|VGL max = -13V|
Register 0x10 Bit[7:6]=01h (-13V<= VGL<=-(AVDD-0.5V))

Typical Application Circuit_3

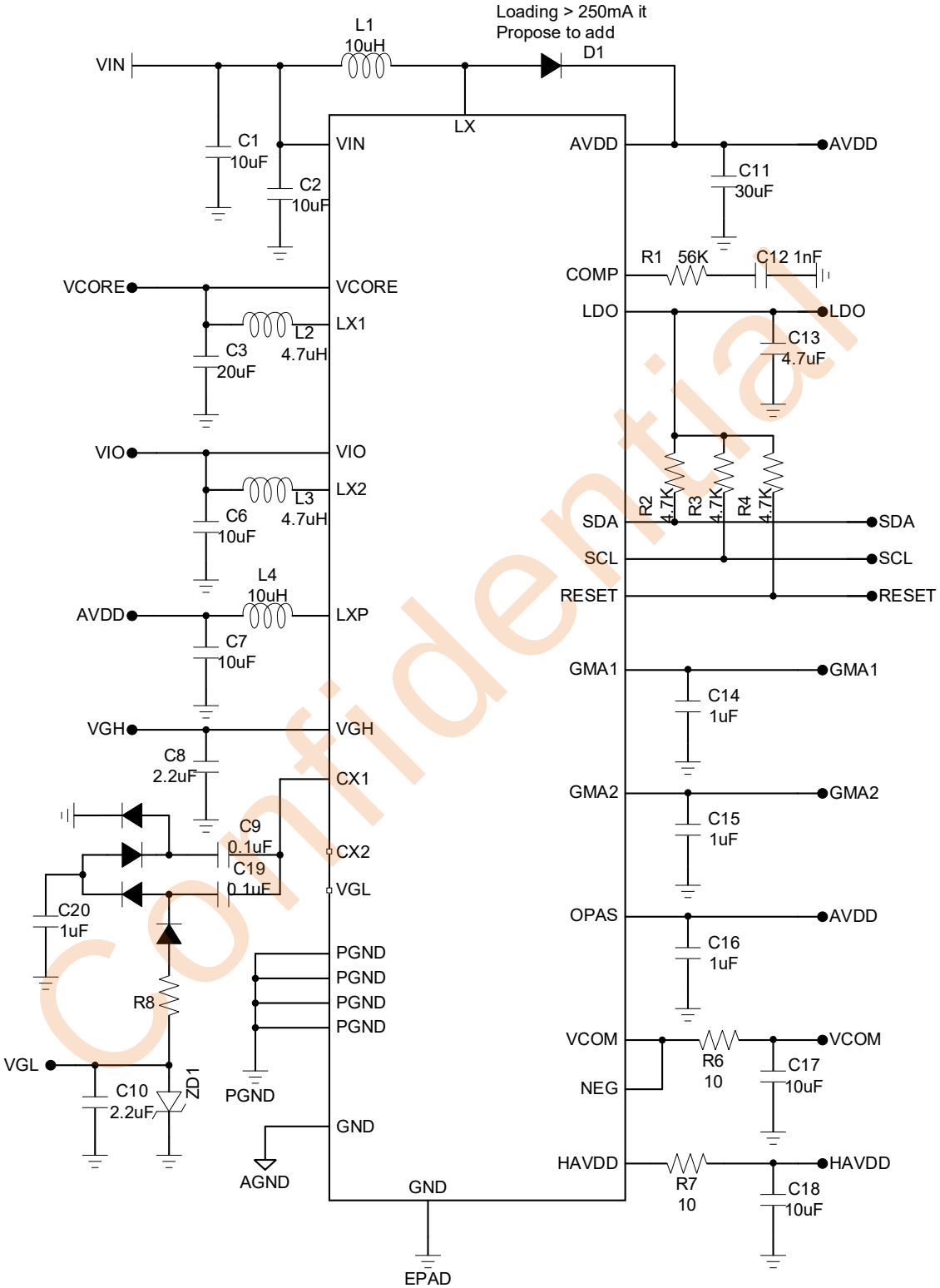
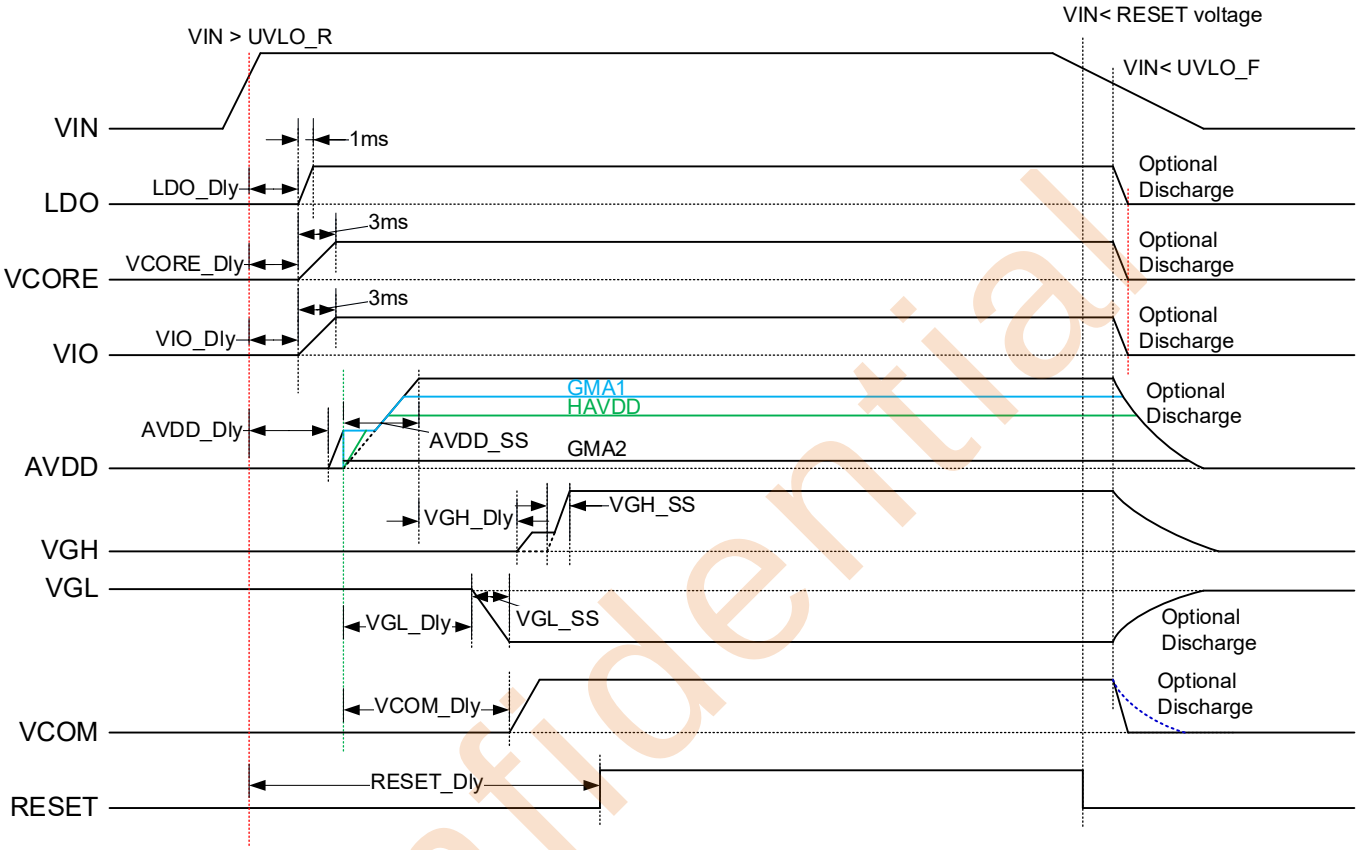


Figure 3 The Application Circuit for VGL Internal
|VGL=-18V|>|AVDD=9V| & |VGL|>|VGL max = -13V|
Register 0x10 Bit[7:6]=10h (VGL<-13V)

Timing Diagram-LP6263A

The LP6263A Power On/Off Sequence is as Figure below. The regulators including VLDO, VIO, VCORE and VAVDD have adjustable time delay which is referred to input voltage. The VGL and VCOM startup delay will be enabled when AVDD enables its soft-start routine. The VGH startup delay will be enabled when AVDD is in regulation.



Note：

1. HAVDD/GMA1/GMA2 can power on with AVDD, But the voltage level can't be higher than AVDD
2. AVDD power on sequence: imbedded MOS for AVDD isolation
3. VCOM power on delay time range: 0~155ms, Power off VCOM to GND Less than 1ms.

THEORY OF OPERATION

The LP6263A offers a complete solution for powering TFT LCD panels. The device integrates one synchronous boost regulator for the source driver supply (AVDD), the second synchronous boost regulator for gate-on voltage (VGH), one negative charge pump regulator for the gate-off voltage (VGL), two synchronous buck regulators (VCORE and VIO), a low dropout linear regulator (LDO) for system logic power, one or two RESET (XAO) function for input supply monitor, a programmable VCOM amplifier and one operational amplifier for HAVDD application. The device includes various system protection schemes such as soft start, power up sequencing, fault protection, and thermal shutdown. The LP6263A also includes IIC interface for various device settings such as output voltages, switching frequency, soft start time, delay time, etc.

Under Voltage Lockout(UVLO)

For systematic startup, LP6263A employs a UVLO rising threshold of 2.6V typical. Thus, the input supply must exceed the UVLO threshold for the regulators to begin switching. Likewise, the device shuts down all functions when the input voltage is lower than UVLO falling threshold of 2.0V. A 600mV hysteresis is added to prevent device chattering when the input supply is noisy or unstable during power up or power down.

Boost Regulator for AVDD

The synchronous AVDD boost regulator integrates a low R_{DSON} NMOS for the low side switch, and a PMOS as the output rectifier. It features true-shutdown switch to isolate input voltage before enabled. The boost output voltage, switching current limit, switching frequency, switching ON transient slew rate, soft start time, and delay time are programmed via IIC interface. See more details in the register map.

Boost Regulator for VGH

The synchronous boost regulator that supplies the VGH voltage to the TFT-LCD gate-on voltage also uses a current mode control scheme. Similarly, the output voltage, switching frequency, soft start time, and delay time are programmed via IIC interface. See more details in the register map.

Buck Regulator for (VCORE and VIO)

The two synchronous buck regulators have the same architect which has implemented a high-side PMOS and a low-side NMOS and it eliminates the need for an external Schottky diode. Low on-resistance for both the switches maximizes efficiency. Moreover, the buck is compensated internally so that no external compensation network is required. The output voltage of VCORE buck regulator can be set from 0.8V to 2.0V with 0.05V step resolution or from 0.62V to 1.1V with 0.02V step resolution and the VIO output voltage can be set from 1.0V to 2.8V with 0.05V steps. The switching frequency, switching ON transient slew rate and delay time are programmed via IIC interface. See more details in the register map.

Charge Pump Regulator for VGL

The LP6263A includes a negative charge pump regulator for the gate-off driver. The regulator can provide a negative voltage down to –4.4V maximum and –13V minimum, programmable with 0.1V resolution. Its switching frequency, the soft start and the delay time can be set via IIC interface. See more details in the register map.

Low Dropout Linear Regulator for VLDO

The integrated LDO output voltage can program from 1.8V to 2.8V with 0.1V step resolution via IIC interface. Power up delay time for the LDO can be set via IIC interface. See more details in the register map. The LDO is capable of a minimum 150mA output load.

HAVDD Operational Amplifier

There is an operational amplifier which is used for HAVDD voltage. Its output is programmable from 3.5V to 6.5V with 0.1V resolution via IIC. and can deliver ±250mA output short-circuit current.

RESET (XAO)

This device has two internal RESET circuits to monitor the voltage at VIN. When VIN is lower than the detect threshold, RESET output will be pulled low. RESET is an open-drain output that needs a pull-up resistor (10kΩ TYP.) to a system supply. The threshold is set via IIC from 2.0V to 2.7V with 0.1V step resolution. When VIN rises above its UVLO threshold (TYP. 2.3V), the output of RESET will be pulled High after RESET delay time has completed. The RESET delay time ranges from 0ms to 75ms with 5ms step resolution and also can be set via IIC.

Programmable VCOM Buffer

The IIC programmable VCOM operation amplifier can be used to digitally adjust a panel's VCOM voltage to remove flicker. The register 0x0A is used to adjust a central value (VCOM) of VCOM with 8-bit resolution and then the VCOM register value can program the voltage increment or decrement of VCOM by independent PVCOM protocol with 7-bit resolution.

Gamma References

The LP6263A includes 2-channel adjustable gamma references. The adjustable range for GAM1 is from (AVDD-0.1)V to (AVDD-1)V with 0.05V resolution. The adjustable range for GAM2 is from 0.1V to 1V with 0.05V resolution.

Under Voltage Protection(UVP)

Under-Voltage Protection (UVP) is included for the outputs of AVDD boost, VGH boost, charge-pump (VGL) ,the buck converters (VCORE, VIO) and linear-regulator (VLDO). When any one of the output voltage drops 80% from its nominal value for more than 60ms due to overload conditions, the device will prevent the internal MOS from switching. This latched condition can only reset by toggling VIN power.

Short Circuit Protection(SCP)

Short-Circuit Protection (SCP) is also included for AVDD boost, VGH/VGL regulator, the buck converters (VCORE, VIO) and linear-regulator (VLDO). When any one of the output voltage drops below 30% of its nominal value, the device will immediately shutdown. This latched condition can only reset by toggling VIN power.

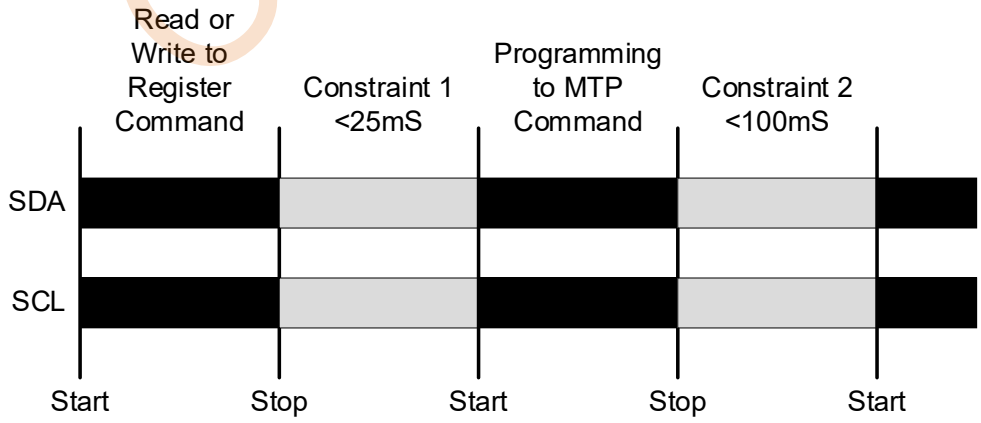
Over Voltage Protection(OVP)

The LP6263A includes over-voltage protection for AVDD, VGH and VGL regulators, When any one of the output voltage rises above its OVP threshold, the regulator will stop switching until it falls below the hysteresis threshold.

Thermal Shutdown

The LP6263A device enters into fault protection shutdown when the junction temperature reaches approximately 150°C. The device will resume the operation once the junction temperature falls below the hysteresis threshold of 20°C

IIC Programming Timing Chart



Device Address Setting

PMIC Device Slave Address (0x46h)

MSB							LSB
0	1	0	0	0	1	1	R/W

Read Address	Write Address
01000111(47h)	01000110(46h)

Configuration PVCOM Device Slave Address (0x9Eh)

MSB							LSB
1	0	0	1	1	1	1	R/W

Read Address	Write Address
10011111(9Fh)	10011110(9Eh)

PMIC IIC Command

1. Write single byte of data to DAC register Example: Write 29h to DAC Address 07h

Start	0	1	0	0	0	1	1	0	Slave ACK	0	0	0	0	0	1	1	1	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK	Stop

2. Write multiple byte of data to DAC register Example: Write 29h,2Ah,2Bh to DAC Address 06h,07h,08h

Start	0	1	0	0	0	1	1	0	Slave ACK	0	0	0	0	0	1	1	0	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK

0	0	1	0	1	0	1	0	Slave ACK	0	0	1	0	1	0	1	1	Slave ACK	Stop

3. Write All DAC Register into MTP Example: Write All DAC Register into MTP

Start	0	1	0	0	0	1	1	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	1	0	0	0	0	0	0	0	Slave ACK	Stop

4. Read data from DAC register Example: Reading Data from DAC Register Address 08h,09h,0Ah,0Bh

Start	0	1	0	0	0	1	1	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	0	0	0	0	0	0	0	0	Slave ACK	Stop

Start	0	1	0	0	0	1	1	0	Slave ACK	0	0	0	0	1	0	0	0	Slave ACK

Start	0	1	0	0	0	1	1	1	Slave ACK	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master ACK

D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master N-ACK	Stop

5. Read data from MTP Example: Reading Data from MTP Address 03h, 04h, 05h,06h

Start	0	1	0	0	0	1	1	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	0	0	0	0	0	0	0	1	Slave ACK	Stop

Start	0	1	0	0	0	1	1	0	Slave ACK	0	0	0	0	0	0	1	1	Slave ACK

Start	0	1	0	0	0	1	1	1	Slave ACK	D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master ACK

D	D	D	D	D	D	D	D	Master ACK	D	D	D	D	D	D	D	D	Master N-ACK	Stop

Configuration Parameter VCOM IIC Command

Write Command

1. Write Single DATA to DAC Example: Writing 77h(7bit data) to DAC

Start	1	0	0	1	1	1	1	0	Slave ACK	1	1	1	0	1	1	1	1	Slave ACK	Stop

2. Write Single DATA to DAC&MTP Example: Writing 77h(7bit data) to DAC&MTP

Start	1	0	0	1	1	1	1	0	Slave ACK	1	1	1	0	1	1	1	0	Slave ACK	Stop

Read Command

3. Read Single DATA from DAC When DAC DATA Same as MTP Example: Read Data from DAC

Start	1	0	0	1	1	1	1	1	Slave ACK	D	D	D	D	D	D	D	0	Slave ACK	Stop

4. Read Single DATA from DAC When DAC DATA Different as MTP Example: Read Data from DAC

Start	1	0	0	1	1	1	1	1	Slave ACK	D	D	D	D	D	D	D	1	Slave ACK	Stop

PMIC Register Map:

PMIC Device Address: 0x23h PVCOM Device Address: 0x4Fh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x00 (FFh)	[7] VCOM Enable	VCOM_EN	0:Disable; 1:Enable		1:Enable
	[6] LDO Enable	VLDO_EN	0:Disable; 1:Enable		1:Enable
	[5] VIO Enable	VIO_EN	0:Disable; 1:Enable		1:Enable
	[4] VCORE Enable	VCORE_EN	0:Disable; 1:Enable		1:Enable
	[3] HAVDD Enable	HAVDD_EN	0:Disable; 1:Enable		1:Enable
	[2] VGH Enable	VGH_EN	0:Disable; 1:Enable		1:Enable
	[1] VGL Enable	VGL_EN	0:Disable; 1:Enable		1:Enable
	[0] AVDD Enable	AVDD_EN	0:Disable; 1:Enable		1:Enable
0x01 (03h)	[7:4] Reserved				
	[3] VIO FCC Enable	VIO_FCCM_EN	0:Enable; 1:Disable		0:Enable
	[2] VCORE FCC Enable	VCORE_FCCM_EN	0:Enable; 1:Disable		0:Enable
	[1] RESET Enable	RESET_EN	0:Disable; 1:Enable		1:Enable
	[0] GMA1/GMA2 Enable	GMA1/GMA2_EN	0:Disable; 1:Enable		1:Enable
0x02 (01h)	[7:4] Reserved				
	[3] AVDD.GMA Discharge Enable	AVDD.GMA _DCG_EN	0:Disable; 1:Enable		0:Disable
	[2] VGL Discharge Enable	VGL_DCG_EN	0:Disable; 1:Enable		0:Disable
	[1] HAVDD Discharge Enable	HAVDD_DCG_EN	0:Disable; 1:Enable		0:Disable
	[0] VCOM Discharge Enable	VCOM_DCG_EN	0:Disable; 1:Enable		1:Enable
0x03 (14h)	[7] Reserved				
	[6:0] AVDD Voltage	AVDD	7.0V to 13.5V	0.1V	14h: 9.0V
0x04 (24h)	[7] Reserved				
	[6:0] VGL Voltage	VGL	-4.4V to -13.0V	0.1V	24h: -8.0V
0x05 (0Ch)	[7:5] Reserved				
	[4:0] VGH Voltage	VGH	10.0V to 34.0V	1V	0Ch: 22V
0x06 (0Ah)	[7:4] Reserved				
	[5:0] HAVDD Voltage	HAVDD	3.5V to 6.5V	0.05V	0Ah: 4.0V

PMIC Register Map:

PMIC Device Address: 0x23h PVCOM Device Address: 0x4Fh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x07 (08h)	[7:5] Reserved				
	[4:0] VCORE Voltage	VCORE	@0x12[7]=0 0.8V to 2.0V @0x12[7]=1 0.62V to 1.1V	0.05V@0x12[7]=0 0.02V@0x12[7]=1	1.2V@0x12[7]=0 0.78V@0x12[7]=1
0x08 (10h)	[7:6] Reserved				
	[5:0] VIO Voltage	VIO	1.0V to 2.8V	0.05V	10h: 1.80V
0x09 (07h)	[7:4] Reserved				
	[3:0] VLDO Voltage	VLDO	1.8V to 2.8V	0.1V	07h: 2.5V
0x0A (6Eh)	[7:0] VCOM Voltage	VCOM	1.5V to 6.2V	0.02V	6Eh: 3.70V
0x0B (02h)	[7:3] Reserved				
	[2:0] RESET Voltage	RESET	2.0V to 2.7V	0.1V	02h: 2.2V
0x0C (02h)	[7:5] Reserved				
	[4:0] GMA1 Voltage	GMA1	(AVDD-0.1)V to (AVDD-1)V	0.05V	02h: (AVDD-0.2)V
0x0D (06h)	[7] Reserved				
	[4:0] GMA2 Voltage	GMA2	0.1V to 1.0V	0.05V	06h: 0.4V
0x0E (31h)	[7] AVDD Compensation	AVDD_COMP	0: External 1: Internal		0: External
	[6:5] AVDD Current Limit	AVDD_ILIMIT	00: 0.5A 01: 1.0A 10: 1.5A 11: 2.0A		01: 1.0A
	[4:3] AVDD Slew Rate	AVDD_SR	00: Fastest 01: Fast 10: Normal 11: Slow		10:Normal
	[2:0] AVDD Switch Frequency	AVDD_FREQ	000: 600KHz ~ 101:1225KHz		001: 715KHz
0x0F (02h)	[7:6] Reserved				
	[5] AVDD Power MOSFET	AVDD_MOS	0: Internal 1: External		0: Internal
	[4:3] AVDD Soft-start time	AVDD_SS	00: 5ms 01: 10ms 10: 15ms 11: 20ms		00: 5ms
	[2:0] AVDD Delay Time	AVDD_DLY	0ms to 35ms	5ms	010: 10ms
0x10 (2Ah)	[7:6] VGL Architecture Mode	VGL_MODE	00: <AVDD-0.5 01: <13.0V 10: Open Loop		00: <AVDD-0.5
	[5] VGL Frequency	VGL_FREQ	0: 0.5*AVDD_F 1: 1*AVDD_F		1: 1*AVDD_F
	[4:3] VGL Soft-start Time	VGL_SS	00: 2ms; 01: 4ms 10: 6ms; 11: 8ms		01: 4ms
	[2:0] VGL Delay Time	VGL_DLY	0ms to 35ms	5ms	010: 10ms

PMIC Register Map:

PMIC Device Address: 0x23h PVCOM Device Address: 0x4Fh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x11 (34h)	[7:5] VGH Switch Frequency	VGH_FREQ	000: 600KHz ~ 101:1225KHz		001: 715KHz
	[4:3] VGH Soft-start Time	VGH_SS	00: 2ms; 01: 4ms 10: 6ms; 11: 8ms		10: 6ms
	[2:0] VGH Delay Time	VGH_DLY	0ms to 35ms	5ms	100: 20ms
0x12 (45h)	[7] VCORE Voltage Adjust	VCORE_V	0: 0.8V to 2.0V 1: 0.62V to 1.1V		0: 0.8V to 2.0V
	[6:5] VCORE Slew Rate	VCORE_SR	00:Fastest 01:Fast 10:Normal 11:Slow		10:Normal
	[4:2] VCORE Switch Frequency	VCORE_FREQ	000: 600KHz ~ 101:1225KHz		001: 715KHz
	[1:0] VCORE Delay Time	VCORE_DLY	00: 0ms; 01: 3ms 10: 6ms; 11: 9ms		01: 3ms
0x13 (45h)	[7:6] Reserved				
	[6:5] VIO Slew Rate	VIO_SR	00:Fastest 01:Fast 10:Normal 11:Slow		10:Normal
	[4:2] VIO Switch Frequency	VIO_FREQ	000: 600KHz ~ 101:1225KHz		001: 715KHz
	[1:0] VIO Delay Time	VIO_DLY	00: 0ms; 01: 3ms 10: 6ms; 11: 9ms		01: 3ms
0x14 (01h)	[7:2] Reserved				
	[1:0] VLDO Delay Time	VLDO_DLY	00: 0ms; 01: 3ms 10: 6ms; 11: 9ms		01: 3ms
0x15 (07h)	[7:4] Reserved				
	[3:0] RESET Delay Time	RESET_DLY	0ms to 75ms	5ms	0111: 35ms
0x16 (05h)	[7:6] Reserved				
	[5] VCOM Power Off Follow	VCOM_POFF	0: VIN_UVLO 1: RESET		0: follow VIN_UVLO
	[4:0] VCOM Delay Time	VCOM_DLY	0ms to 155ms	5ms	00101: 25ms
0x17 (00h)	[7] RESET Disable Follow	RESET_OFF_F	0: Open Drain 1: Pull Low		0: Open Drain
	[6:0] Reserved				

PMIC Register Map:

PMIC Device Address: 0x23h PVCOM Device Address: 0x4Fh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x18 (00h)	[7] VIN Discharge Enable	VIN_DCG_EN	0: Disable 1: Enable		0: Disable
	[6:5] AVDD Compensation R	AVDD_CR	00: 40K 01: 20K 10: 80K 11: 60K		00: 40KΩ
	[4:3] AVDD Compensation C	AVDD_CC	00: 30pF 01: 60pF 10: 90pF 11: 120pF		00: 30pF
	[2] VLDO Discharge Enable	VLDO_DCG_EN	0: Disable 1: Enable		0: Disable
	[1] VIO Discharge Enable	VIO_DCG_EN	0: Disable 1: Enable		0: Disable
	[0] VCORE Discharge Enable	VCORE_DCG_EN	0: Disable 1: Enable		0: Disable
0x19 (00h)	[4] VLDO Power Off Follow	VLDO_POFF	0: VIN_UVLO 1: RESET		0: follow VIN_UVLO
	[3:2] VIO Power Off Follow	VIO_POFF	00: VIN_UVLO 01: RESET 10/11: Reserved		00: follow VIN_UVLO
	[1:0] VCORE Power Off Follow	VCORE_POFF	00: VIN_UVLO 01: RESET 10/11: Reserved		00: follow VIN_UVLO
0x1B (00h)	[6] VLDO NG				00h: (Read Only)
	[5] VCORE NG				
	[4] VIO NG				
	[3] AVDD NG				
	[2] VGH NG				
	[1] VGL NG				
	[0] OTP NG				

Register Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
	Configuration Parameter VCOM (VCOM_I – 10mV*64) ~ (VCOM_I + 10mV*63)							R/W Return	Write operation 0: write to DAC register and MTP. 1: write to DAC register only Read operation Return 0: when DAC and MTP content are the same. Return 1: when DAC and MTP content are different.
0xFF	Control Register								00 : Read data from DAC register 01 : Read data from MTP 80 : Write all DAC into MTP

Registers and DAC settings

Channel on/off 1 (0x00h) --- Default Code FFh

Name	# of Bits	Access	Default	Description
VCOM_EN	7	W/R	**1**	VCOM enabled bit 0: Disabled 1: Enabled.
VLDO_EN	6	W/R	**1**	VLDO regulator enabled bit 0: Disabled 1: Enabled.
VIO_EN	5	W/R	**1**	VIO regulator enabled bit 0: Disabled 1: Enabled.
VCORE_EN	4	W/R	**1**	VCORE regulator enabled bit 0: Disabled 1: Enabled.
HAVDD_EN	3	W/R	**1**	HAVDD regulator enabled bit 0: Disabled 1: Enabled.
VGH_EN	2	W/R	**1**	VGH regulator enabled bit 0: Disabled 1: Enabled.
VGL_EN	1	W/R	**1**	VGL regulator enabled bit 0: Disabled 1: Enabled.
AVDD_EN	0	W/R	**1**	AVDD regulator enabled bit 0: Disabled 1: Enabled.

Channel on/off 2 (0x01h) --- Default Code 03h

Name	# of Bits	Access	Default	Description
---	4-7	W/R	**0**	Reserved.
VIO_FCCM_EN	3	W/R	**0**	VIO regulator forced PWM enabled bit. Set 1 to Disable forced PWM mode.
VCORE_FCCM_EN	2	W/R	**0**	VCORE regulator forced PWM enabled bit. Set 1 to Disable forced PWM mode.
RESET_EN	1	W/R	**1**	RESET function enabled bit 0: Disabled 1: Enabled.
GMA1/GMA2_EN	0	W/R	**1**	GMA1/GMA2 reference enabled bit 0: Disabled 1: Enabled.

Discharge Function Set 1 (0x02h) --- Default Code 01h

Name	# of Bits	Access	Default	Description
---	4-7	W/R	**0**	Reserved.
AVDD.GMA_DCG_EN	3	W/R	**0**	AVDD, GMA1 GMA2 discharge function disabled bit. 0: Disabled. 1: Enabled.
VGL_DCG_EN	2	W/R	**0**	VGL discharge function disabled bit. 0: Disabled. 1: Enabled.
HAVDD_DCG_EN	1	W/R	**0**	HAVDD discharge function disabled bit. 0: Disabled. 1: Enabled.
VCOM_DCG_EN	0	W/R	**1**	VCOM discharge function enabled bit 0: Disabled 1: Enabled.

AVDD Voltage Set (0x03h) --- Default Code 14h

Name	# of Bits	Access	Default	Description
---	7	W/R	**0**	Reserved.
AVDD	6	W/R	**0**	AVDD voltage adjustment from 7.0V to 13.5V/step=0.1V. Refer to table below for details.
	5	W/R	**0**	
	4	W/R	**1**	
	3	W/R	**0**	
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)
00h	7.0	10h	8.6	20h	10.2	30h	11.8
01h	7.1	11h	8.7	21h	10.3	31h	11.9
02h	7.2	12h	8.8	22h	10.4	32h	12.0
03h	7.3	13h	8.9	23h	10.5	33h	12.1
04h	7.4	14h	9.0	24h	10.6	34h	12.2
05h	7.5	15h	9.1	25h	10.7	35h	12.3
06h	7.6	16h	9.2	26h	10.8	36h	12.4
07h	7.7	17h	9.3	27h	10.9	37h	12.5
08h	7.8	18h	9.4	28h	11	38h	12.6
09h	7.9	19h	9.5	29h	11.1	39h	12.7
0Ah	8.0	1Ah	9.6	2Ah	11.2	3Ah	12.8
0Bh	8.1	1Bh	9.7	2Bh	11.3	3Bh	12.9
0Ch	8.2	1Ch	9.8	2Ch	11.4	3Ch	13.0
0Dh	8.3	1Dh	9.9	2Dh	11.5	3Dh	13.1
0Eh	8.4	1Eh	10.0	2Eh	11.6	3Eh	13.2
0Fh	8.5	1Fh	10.1	2Fh	11.7	3Fh	13.3
						40h	13.4
						41h	13.5

VGL Voltage Set (0x04h) --- Default Code 24h

Name	# of Bits	Access	Default	Description
---	7	W/R	**0**	Reserved.
VGL	6	W/R	**0**	VGL voltage adjustment from -4.4V to -13.0V/step=-0.1V. Refer to table below for details.
	5	W/R	**1**	
	4	W/R	**0**	
	3	W/R	**0**	
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VGL1 Voltage(V)	DAC Value	VGL1 Voltage(V)	DAC Value	VGL1 Voltage(V)	DAC Value	VGL1 Voltage(V)
00h	-4.4	16h	-6.6	2Ch	-8.8	42h	-11.0
01h	-4.5	17h	-6.7	2Dh	-8.9	43h	-11.1
02h	-4.6	18h	-6.8	2Eh	-9.0	44h	-11.2
03h	-4.7	19h	-6.9	2Fh	-9.1	45h	-11.3
04h	-4.8	1Ah	-7.0	30h	-9.2	46h	-11.4
05h	-4.9	1Bh	-7.1	31h	-9.3	47h	-11.5
06h	-5.0	1Ch	-7.2	32h	-9.4	48h	-11.6
07h	-5.1	1Dh	-7.3	33h	-9.5	49h	-11.7
08h	-5.2	1Eh	-7.4	34h	-9.6	4Ah	-11.8
09h	-5.3	1Fh	-7.5	35h	-9.7	4Bh	-11.9
0Ah	-5.4	20h	-7.6	36h	-9.8	4Ch	-12.0
0Bh	-5.5	21h	-7.7	37h	-9.9	4Dh	-12.1
0Ch	-5.6	22h	-7.8	38h	-10.0	4Eh	-12.2
0Dh	-5.7	23h	-7.9	39h	10.1	4Fh	-12.3
0Eh	-5.8	24h	-8.0	3Ah	-10.2	50h	-12.4
0Fh	-5.9	25h	-8.1	3Bh	-10.3	51h	-12.5
10h	-6.0	26h	-8.2	3Ch	-10.4	52h	-12.6
11h	-6.1	27h	-8.3	3Dh	-10.5	53h	-12.7
12h	-6.2	28h	-8.4	3Eh	-10.6	54h	-12.8
13h	-6.3	29h	-8.5	3Fh	-10.7	55h	-12.9
14h	-6.4	2Ah	-8.6	40h	-10.8	56h	-13
15h	-6.5	2Bh	-8.7	41h	-10.9		

VGH Voltage Set (0x05h) --- Default Code 0Ch

Name	# of Bits	Access	Default	Description
---	5-7	W/R	**0**	Reserved.
VGH	4	W/R	**0**	VGH voltage adjustment from 10V to 34V/step=1V. Refer to table below for details.
	3	W/R	**1**	
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VGH Voltage(V)	DAC Value	VGH Voltage(V)	DAC Value	VGH Voltage(V)	DAC Value	VGH Voltage(V)
00h	10	06h	16	0Ch	22	12h	28
01h	11	07h	17	0Dh	23	13h	29
02h	12	08h	18	0Eh	24	14h	30
03h	13	09h	19	0Fh	25	15h	31
04h	14	0Ah	20	10h	26	16h	32
05h	15	0Bh	21	11h	27	17h	33
						18h	34

HAVDD Voltage Set (0x06h) --- Default Code 0Ah

Name	# of Bits	Access	Default	Description
---	6-7	W/R	**0**	Reserved.
HAVDD	5	W/R	**0**	HAVDD voltage adjustment from 3.5V to 6.5V/step=0.05V. Refer to table below for details.
	4	W/R	**0**	
	3	W/R	**1**	
	2	W/R	**0**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)
00h	3.50	10h	4.30	20h	5.10	30h	5.90
01h	3.55	11h	4.35	21h	5.15	31h	5.95
02h	3.60	12h	4.40	22h	5.20	32h	6.00
03h	3.65	13h	4.45	23h	5.25	33h	6.05
04h	3.70	14h	4.50	24h	5.30	34h	6.10
05h	3.75	15h	4.55	25h	5.35	35h	6.15
06h	3.80	16h	4.60	26h	5.40	36h	6.20
07h	3.85	17h	4.65	27h	5.45	37h	6.25
08h	3.90	18h	4.70	28h	5.50	38h	6.30
09h	3.95	19h	4.75	29h	5.55	39h	6.35
0Ah	4.00	1Ah	4.80	2Ah	5.60	3Ah	6.40
0Bh	4.05	1Bh	4.85	2Bh	5.65	3Bh	6.45
0Ch	4.10	1Ch	4.90	2Ch	5.70	3Ch	6.50
0Dh	4.15	1Dh	4.95	2Dh	5.75		
0Eh	4.20	1Eh	5.00	2Eh	5.80		
0Fh	4.25	1Fh	5.05	2Fh	5.85		

VCORE Voltage Set (0x07h) --- Default Code 08h

Name	# of Bits	Access	Default	Description
---	5-7	W/R	**0**	Reserved.
VCORE	4	W/R	**0**	VCORE voltage adjustment from 0.80V to 2.00V/step=0.05V. Refer to table below for details. Optional VCORE range from 0.62V to 1.1V with 20mV/step by reg0x12[7]=1.
	3	W/R	**1**	
	2	W/R	**0**	
	1	W/R	**1**	
	0	W/R	**0**	

By reg 0x12[7]=0

DAC Value	VCORE Voltage(V)	DAC Value	VCORE Voltage(V)	DAC Value	VCORE Voltage(V)	DAC Value	VCORE Voltage(V)
00h	0.80	07h	1.15	0Eh	1.50	15h	1.85
01h	0.85	08h	1.20	0Fh	1.55	16h	1.90
02h	0.90	09h	1.25	10h	1.60	17h	1.95
03h	0.95	0Ah	1.30	11h	1.65	18h	2.00
04h	1.00	0Bh	1.35	12h	1.70		
05h	1.05	0Ch	1.40	13h	1.75		
06h	1.10	0Dh	1.45	14h	1.80		

By reg 0x12[7]=1

DAC Value	VCORE Voltage(V)	DAC Value	VCORE Voltage(V)	DAC Value	VCORE Voltage(V)	DAC Value	VCORE Voltage(V)
00h	0.62	07h	0.76	0Eh	0.90	15h	1.04
01h	0.64	08h	0.78	0Fh	0.92	16h	1.06
02h	0.66	09h	0.80	10h	0.94	17h	1.08
03h	0.68	0Ah	0.82	11h	0.96	18h	1.10
04h	0.70	0Bh	0.84	12h	0.98		
05h	0.72	0Ch	0.86	13h	1.00		
06h	0.74	0Dh	0.88	14h	1.02		

VIO Voltage Set (0x08h) --- Default Code 10h

Name	# of Bits	Access	Default	Description
---	6-7	W/R	**0**	Reserved.
VIO	5	W/R	**0**	VIO voltage adjustment from 1.00V to 2.80V/step=0.05V. Refer to table below for details.
	4	W/R	**1**	
	3	W/R	**0**	
	2	W/R	**0**	
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VIO Voltage(V)	DAC Value	VIO Voltage(V)	DAC Value	VIO Voltage(V)	DAC Value	VIO Voltage(V)
00h	1.00	0Ah	1.50	14h	2.00	1Eh	2.50
01h	1.05	0Bh	1.55	15h	2.05	1Fh	2.55
02h	1.10	0Ch	1.60	16h	2.10	20h	2.60
03h	1.15	0Dh	1.65	17h	2.15	21h	2.65
04h	1.20	0Eh	1.70	18h	2.20	22h	2.70
05h	1.25	0Fh	1.75	19h	2.25	23h	2.75
06h	1.30	10h	1.80	1Ah	2.30	24h	2.80
07h	1.35	11h	1.85	1Bh	2.35		
08h	1.40	12h	1.90	1Ch	2.40		
09h	1.45	13h	1.95	1Dh	2.45		

VLDO Voltage Set (0x09h) --- Default Code 07h

Name	# of Bits	Access	Default	Description
---	4-7	W/R	**0**	Reserved.
VLDO	3	W/R	**0**	VLDO voltage adjustment from 1.8V to 2.8V/step=0.1V. Refer to table below for details.
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**1**	

DAC Value	LDO Voltage(V)	DAC Value	LDO Voltage(V)	DAC Value	LDO Voltage(V)	DAC Value	LDO Voltage(V)
00h	1.8	03h	2.1	06h	2.4	09h	2.7
01h	1.9	04h	2.2	07h	2.5	0Ah	2.8
02h	2.0	05h	2.3	08h	2.6		

VCOM Voltage Set (0x0Ah) --- Default Code 6Eh

Name	# of Bits	Access	Default	Description
VCOM	7	W/R	**0**	VCOM_I voltage adjustment from 1.5V to 6.2V/step=0.02V. Refer to table below for details.
	6	W/R	**1**	
	5	W/R	**1**	
	4	W/R	**0**	
	3	W/R	**1**	
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)
00h	1.50	1Ch	2.06	38h	2.62	54h	3.18
01h	1.52	1Dh	2.08	39h	2.64	55h	3.20
02h	1.54	1Eh	2.10	3Ah	2.66	56h	3.22
03h	1.56	1Fh	2.12	3Bh	2.68	57h	3.24
04h	1.58	20h	2.14	3Ch	2.70	58h	3.26
05h	1.60	21h	2.16	3Dh	2.72	59h	3.28
06h	1.62	22h	2.18	3Eh	2.74	5Ah	3.30
07h	1.64	23h	2.20	3Fh	2.76	5Bh	3.32
08h	1.66	24h	2.22	40h	2.78	5Ch	3.34
09h	1.68	25h	2.24	41h	2.80	5Dh	3.36
0Ah	1.70	26h	2.26	42h	2.82	5Eh	3.38
0Bh	1.72	27h	2.28	43h	2.84	5Fh	3.40
0Ch	1.74	28h	2.30	44h	2.86	60h	3.42
0Dh	1.76	29h	2.32	45h	2.88	61h	3.44
0Eh	1.78	2Ah	2.34	46h	2.90	62h	3.46
0Fh	1.80	2Bh	2.36	47h	2.92	63h	3.48
10h	1.82	2Ch	2.38	48h	2.94	64h	3.50
11h	1.84	2Dh	2.40	49h	2.96	65h	3.52
12h	1.86	2Eh	2.42	4Ah	2.98	66h	3.54
13h	1.88	2Fh	2.44	4Bh	3.00	67h	3.56
14h	1.90	30h	2.46	4Ch	3.02	68h	3.58
15h	1.92	31h	2.48	4Dh	3.04	69h	3.60
16h	1.94	32h	2.50	4Eh	3.06	6Ah	3.62
17h	1.96	33h	2.52	4Fh	3.08	6Bh	3.64
18h	1.98	34h	2.54	50h	3.10	6Ch	3.66
19h	2.00	35h	2.56	51h	3.12	6Dh	3.68
1Ah	2.02	36h	2.58	52h	3.14	6Eh	3.70
1Bh	2.04	37h	2.60	53h	3.16	6Fh	3.72

DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)
70h	3.74	90h	4.38	B0h	5.02	D0h	5.66
71h	3.76	91h	4.40	B1h	5.04	D1h	5.68
72h	3.78	92h	4.42	B2h	5.06	D2h	5.70
73h	3.80	93h	4.44	B3h	5.08	D3h	5.72
74h	3.82	94h	4.46	B4h	5.10	D4h	5.74
75h	3.84	95h	4.48	B5h	5.12	D5h	5.76
76h	3.86	96h	4.50	B6h	5.14	D6h	5.78
77h	3.88	97h	4.52	B7h	5.16	D7h	5.80
78h	3.90	98h	4.54	B8h	5.18	D8h	5.82
79h	3.92	99h	4.56	B9h	5.20	D9h	5.84
7Ah	3.94	9Ah	4.58	BAh	5.22	DAh	5.86
7Bh	3.96	9Bh	4.60	BBh	5.24	DBh	5.88
7Ch	3.98	9Ch	4.62	BCh	5.26	DCh	5.90
7Dh	4.00	9Dh	4.64	BDh	5.28	DDh	5.92
7Eh	4.02	9Eh	4.66	BEh	5.30	DEh	5.94
7Fh	4.04	9Fh	4.68	BFh	5.32	DFh	5.96
80h	4.06	A0h	4.70	C0h	5.34	E0h	5.98
81h	4.08	A1h	4.72	C1h	5.36	E1h	6.00
82h	4.10	A2h	4.74	C2h	5.38	E2h	6.02
83h	4.12	A3h	4.76	C3h	5.40	E3h	6.04
84h	4.14	A4h	4.78	C4h	5.42	E4h	6.06
85h	4.16	A5h	4.80	C5h	5.44	E5h	6.08
86h	4.18	A6h	4.82	C6h	5.46	E6h	6.10
87h	4.20	A7h	4.84	C7h	5.48	E7h	6.12
88h	4.22	A8h	4.86	C8h	5.50	E8h	6.14
89h	4.24	A9h	4.88	C9h	5.52	E9h	6.16
8Ah	4.26	AAh	4.90	CAh	5.54	EAh	6.18
8Bh	4.28	ABh	4.92	CBh	5.56	EBh	6.20
8Ch	4.30	ACh	4.94	CCh	5.58		
8Dh	4.32	ADh	4.96	CDh	5.60		
8Eh	4.34	AEh	4.98	CEh	5.62		
8Fh	4.36	AFh	5.00	CFh	5.64		

RESET Threshold Voltage Set (0x0Bh) --- Default Code 02h

Name	# of Bits	Access	Default	Description
	3-7	W/R	**0**	Reserved
RESET	2	W/R	**0**	RESET threshold voltage adjustment from 2.0V to 2.7V/step=0.1V. Refer to table below for details.
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	RESET Voltage(V)	DAC Value	RESET Voltage(V)	DAC Value	RESET Voltage(V)	DAC Value	RESET Voltage(V)
00h	2	02h	2.2	04h	2.4	06h	2.6
01h	2.1	03h	2.3	05h	2.5	07h	2.7

GMA1 Voltage Set (0x0Ch) --- Default Code 02h

Name	# of Bits	Access	Default	Description
	5-7	W/R	**0**	Reserved
GMA1	4	W/R	**0**	GMA1 voltage adjustment from (AVDD-0.1)V to (AVDD-1)V/step=0.05V. Refer to table below for details.
	3	W/R	**0**	
	2	W/R	**0**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	GMA1 Voltage(V)	DAC Value	GMA1 Voltage(V)	DAC Value	GMA1 Voltage(V)	DAC Value	GMA1 Voltage(V)
00h	AVDD -(50mVx2)	05h	AVDD -(50mVx7)	0Ah	AVDD -(50mVx12)	0Fh	AVDD -(50mVx17)
01h	AVDD -(50mVx3)	06h	AVDD -(50mVx8)	0Bh	AVDD -(50mVx13)	10h	AVDD -(50mVx18)
02h	AVDD -(50mVx4)	07h	AVDD -(50mVx9)	0Ch	AVDD -(50mVx14)	11h	AVDD -(50mVx19)
03h	AVDD -(50mVx5)	08h	AVDD -(50mVx10)	0Dh	AVDD -(50mVx15)	12h	AVDD -(50mVx20)
04h	AVDD -(50mVx6)	09h	AVDD -(50mVx11)	0Eh	AVDD -(50mVx16)		

GMA2 Voltage Set (0x0Dh) --- Default Code 06h

Name	# of Bits	Access	Default	Description
	5-7	W/R	**0**	Reserved
GMA2	4	W/R	**0**	GMA2 voltage adjustment from 0.1V to 1V/step=0.05V. Refer to table below for details.
	3	W/R	**0**	
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	GMA2 Voltage(V)	DAC Value	GMA2 Voltage(V)	DAC Value	GMA2 Voltage(V)	DAC Value	GMA2 Voltage(V)
00h	0.10	05h	0.35	0Ah	0.60	0Fh	0.85
01h	0.15	06h	0.40	0Bh	0.65	10h	0.90
02h	0.20	07h	0.45	0Ch	0.70	11h	0.95
03h	0.25	08h	0.50	0Dh	0.75	12h	1.00
04h	0.30	09h	0.55	0Eh	0.80		

AVDD Configuration 1 (0x0Eh) --- Default Code 31h

Name	# of Bits	Access	Default	Description
AVDD_COMP	7	W/R	**0**	AVDD compensation internal/external select 0: External 1: Internal
AVDD_ILIMIT	6	W/R	**0**	AVDD current limit threshold adjustment. 00: 0.5A, 01: 1.0A, 10: 1.5A. 11: 2.0A
	5	W/R	**1**	
AVDD_SR	4	W/R	**1**	AVDD switching speed adjustment (falling edge). 00: TBDns, 01: TBDns, 10: TBDns, 11: TBDns.
	3	W/R	**0**	
AVDD_FREQ	2	W/R	**0**	AVDD switching frequency adjustment. 000: 600kHz, 001: 715kHz, 010: 800kHz, 011: 900kHz, 100: 1000kHz, 101:1225kHz
	1	W/R	**0**	
	0	W/R	**1**	

AVDD Configuration 2 (0x0Fh) --- Default Code 02h

Name	# of Bits	Access	Default	Description
	6-7	W/R	**0**	Reserved
AVDD_MOS	5	W/R	**0**	Select AVDD_MOS Type 0: Internal 1: External.
AVDD_SS	4	W/R	**0**	AVDD soft-start time adjustment. 00: 5ms, 01: 10ms, 10: 15ms, 11:20ms.
	3	W/R	**0**	
AVDD_DLY	2	W/R	**0**	AVDD startup delay adjustment. 000: 0ms, 001: 5ms, 010: 10ms, 011: 15ms 100: 20ms, 101:25ms, 110:30ms, 111:35ms
	1	W/R	**1**	
	0	W/R	**0**	

VGL Configuration (0x10h) --- Default Code 2Ah

Name	# of Bits	Access	Default	Description
VGL_MODE	7	W/R	**0**	VGL_MODE select bits. 00: VGL=-4.4V to AVDD-0.5V 01: VGL= AVDD-0.5V to -13V 10: open loop operation
	6	W/R	**0**	
VGL_FREQ	5	W/R	**1**	VGL switching frequency adjustment. 0: 0.5 x F_AVDD_OSC, 1: F_AVDD_OSC
VGL_SS	4	W/R	**0**	VGL soft-start time adjustment. 00: 2ms, 01: 4ms, 10: 6ms, 11:8ms.
	3	W/R	**1**	
VGL_DLY	2	W/R	**0**	VGL startup delay adjustment. 000: 0ms, 001: 5ms, 010: 10ms, 011: 15ms 100: 20ms, 101:25ms, 110:30ms, 111:35ms
	1	W/R	**1**	
	0	W/R	**0**	

VGH Configuration (0x11h) --- Default Code 34h

Name	# of Bits	Access	Default	Description
VGH_FREQ	7	W/R	**0**	VGH switching frequency adjustment. 000: 600kHz, 001: 715kHz, 010: 800kHz 011: 933kHz, 100: 1000kHz, 101:1225kHz
	6	W/R	**0**	
	5	W/R	**1**	
VGH_SS	4	W/R	**1**	VGH soft-start time adjustment. 00: 2ms, 01: 4ms, 10: 6ms, 11:8ms.
	3	W/R	**0**	
VGH_DLY	2	W/R	**1**	VGH startup delay adjustment. 000: 0ms, 001: 5ms, 010: 10ms, 011: 15ms 100: 20ms, 101:25ms, 110:30ms, 111:35ms
	1	W/R	**0**	
	0	W/R	**0**	

VCORE Configuration (0x12h) --- Default Code 45h

Name	# of Bits	Access	Default	Description
VCORE_V	7	W/R	**0**	VCORE range extended control bit. Set 1 to extend VCORE range to 0.62V to 1.1V with 20mV/step.
VCORE_SR	6	W/R	**1**	VCORE switching speed adjustment (rising edge). 00: TBDns, 01: TBDns, 10: TBDns, 11: TBDns.
	5	W/R	**0**	
VCORE_FREQ	4	W/R	**0**	VCORE switching frequency adjustment. 000: 600kHz, 001: 715kHz, 010: 800kHz 011: 933kHz, 100: 1000kHz, 101:1225kHz
	3	W/R	**0**	
	2	W/R	**1**	
VCORE_DLY	1	W/R	**0**	VCORE startup delay adjustment. 00: 0ms, 01: 3ms, 10: 6ms, 11:9ms.
	0	W/R	**1**	

VIO Configuration (0x13h) --- Default Code 45h

Name	# of Bits	Access	Default	Description
	7	W/R	**0**	Reserved
VIO_SR	6	W/R	**1**	VIO switching speed adjustment (rising edge). 00: TBDns, 01: TBDns, 10: TBDns, 11: TBDns.
	5	W/R	**0**	
VIO_FREQ	4	W/R	**0**	VIO switching frequency adjustment. 000: 600kHz, 001: 715kHz, 010: 800kHz 011: 933kHz, 100: 1000kHz, 101:1225kHz
	3	W/R	**0**	
	2	W/R	**1**	
VIO_DLY	1	W/R	**0**	VIO startup delay adjustment. 00: 0ms, 01: 3ms, 10: 6ms, 11:9ms.
	0	W/R	**1**	

VLDO Configuration (0x14h) --- Default Code 01h

Name	# of Bits	Access	Default	Description
	2-7	W/R	**0**	Reserved
VLDO_DLY	1	W/R	**0**	VLDO startup delay adjustment. 00: 0ms, 01: 3ms, 10: 6ms, 11:9ms.
	0	W/R	**1**	

RESET Configuration (0x15h) --- Default Code 07h

Name	# of Bits	Access	Default	Description
	4-7	W/R	**0**	Reserved
RESET_DLY	3	W/R	**0**	RESET startup delay adjustment. 5ms/step. Refer to table below for details.
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**1**	

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

VCORE Configuration (0x16h) --- Default Code 05h

Name	# of Bits	Access	Default	Description
	6-7	W/R	**0**	Reserved
VCOM_POFF	5	W/R	**0**	VCOM power off select bit. 0: Listen to VIN UVLO. 1: Listen to RESET.
VCOM_DLY	4	W/R	**0**	VCOM startup delay adjustment. 5ms/step. Refer to table below for details.
	3	W/R	**0**	
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)	DAC Value	Delay Time (ms)
00h	0	08h	40	10h	80	18h	120
01h	5	09h	45	11h	85	19h	125
02h	10	0Ah	50	12h	90	1Ah	130
03h	15	0Bh	55	13h	95	1Bh	135
04h	20	0Ch	60	14h	100	1Ch	140
05h	25	0Dh	65	15h	105	1Dh	145
06h	30	0Eh	70	16h	110	1Eh	150
07h	35	0Fh	75	17h	115	1Fh	155

RESET Disable Output Follow (0x17h) --- Defalut Code 00h

Name	# of Bits	Access	Default	Description
RESET_OFF_F	7	W/R	**0**	RESET Disable Output Follow 0: RESET Open Drain output Floating 1: RESET Output Pull Low
	5-6	W/R	**0**	Reserved
	4	W/R	**0**	Reserved
	3	W/R	**0**	Reserved
	2	W/R	**0**	
	1	W/R	**0**	
	0	W/R	**0**	Reserved

Discharge Function Set 2 (0x18h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
VIN_DCG_EN	7	W/R	**0**	VIN discharge function enabled bit 0: Disabled 1: Enabled.
AVDD_CR	5-6	W/R	**0**	AVDD compensation resistance 00: 40KΩ 01: 20KΩ 10: 80KΩ 11: 60KΩ
AVDD_CC	3-4	W/R	**0**	AVDD compensation capacitor 00: 30pF 01: 60pF 10: 90pF 11: 120pF
VLDO_DCG_EN	2	W/R	0	VLDO discharge function enabled bit 0: Disabled 1: Enabled.
VIO_DCG_EN	1	W/R	0	VIO discharge function enabled bit 0: Disabled 1: Enabled.
VCORE_DCG_EN	0	W/R	0	VCORE discharge function enabled bit 0: Disabled 1: Enabled.

Power Off Configuration (0x19h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	5-7	W/R	**000**	Reserved
VLDO_POFF	4	W/R	**0**	VLDO power off select bit. 0: Listen to VIN UVLO. 1: Listen to RESET
VIO_POFF	3		**0**	VIO power off select bit. 00: Listen to VIN UVLO. 01: Listen to RESET 10/11: Reserved
	2	W/R	**0**	
VCORE_POFF	1		**0**	VCORE power off select bit. 00: Listen to VIN UVLO. 01: Listen to RESET 10/11: Reserved
	0	W/R	**0**	

Fault Indication (0x1Bh) --- Default Code 00h (Read only)

Name	# of Bits	Access	Default	Description
	7	R	**0**	Reserved
VLDO_NG	6	R	**0**	VLDO_NG = 1; shut down by fault trip level or SCP
VCORE_NG	5	R	**0**	VCORE_NG = 1; shut down by fault trip level or SCP
VIO_NG	4	R	**0**	VIO_NG = 1; shut down by fault trip level or SCP
AVDD_NG	3	R	**0**	AVDD_NG = 1; shut down by fault trip level or SCP
VGH_NG	2	R	**0**	VGH_NG = 1; shut down by fault trip level or SCP
VGL_NG	1	R	**0**	VGL_NG = 1; shut down by fault trip level or SCP
OTP	0	R	**0**	OTP = 1; Trigger temperature protection

Control Register (0xFFh)
The Non-Volatile Memory (NVM) will be written to or read from through the Control Register.

Name	# of Bits	Access	Default	Description
WR_NVM	7	W/R	**0**	Write all DAC into MTP 0: Disable, 1: Enable.
---	1-6	W/R	**0**	Reserved
READ_NVM	0	W/R	**0**	00 : Read data form DAC register 01 : Read data from MTP

00: Read data from DAC register
01: Read data from MTP
80: Write all DAC into MTP

Configuration parameter VCOM with PVCOM Protocol

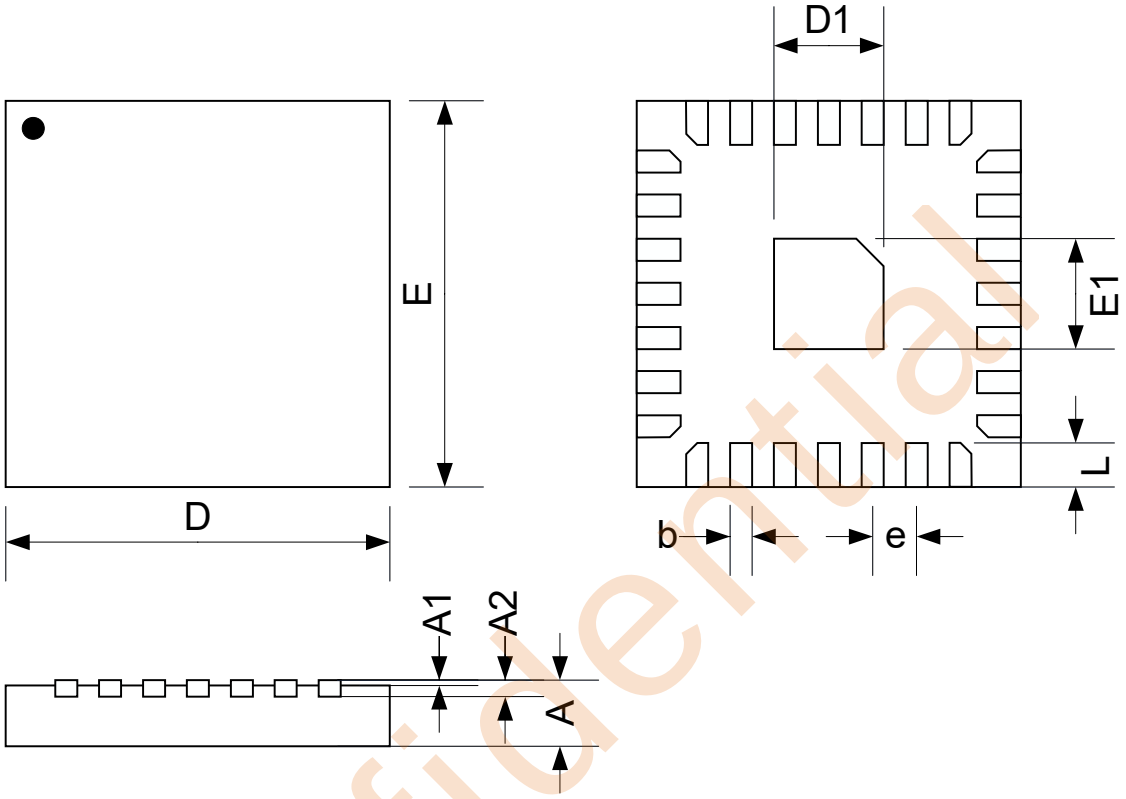
Name	# of Bits	Access	Default	Description
PVCOM	7	W/R	**1**	VCOM voltage adjustment, 10mV/step. Refer to table below for details.
	6	W/R	**0**	
	5	W/R	**0**	
	4	W/R	**0**	
	3	W/R	**0**	
	2	W/R	**0**	
	1	W/R	**0**	
	0		-	Write operation 0: write to DAC register and MTP. 1: write to DAC register only Read operation Return 0: when DAC and MTP content are the same. Return 1: when DAC and MTP content are different.

VCOM level is set by reg0x0A

DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)	DAC Value	VCOM Voltage(V)
00h	VCOM-(10mVx64)	20h	VCOM-(10mVx32)	40h	VCOM	60h	VCOM+(10mVx32)
01h	VCOM-(10mVx63)	21h	VCOM-(10mVx31)	41h	VCOM+(10mVx1)	61h	VCOM+(10mVx33)
02h	VCOM-(10mVx62)	22h	VCOM-(10mVx30)	42h	VCOM+(10mVx2)	62h	VCOM+(10mVx34)
03h	VCOM-(10mVx61)	23h	VCOM-(10mVx29)	43h	VCOM+(10mVx3)	63h	VCOM+(10mVx35)
04h	VCOM-(10mVx60)	24h	VCOM-(10mVx28)	44h	VCOM+(10mVx4)	64h	VCOM+(10mVx36)
05h	VCOM-(10mVx59)	25h	VCOM-(10mVx27)	45h	VCOM+(10mVx5)	65h	VCOM+(10mVx37)
06h	VCOM-(10mVx58)	26h	VCOM-(10mVx26)	46h	VCOM+(10mVx6)	66h	VCOM+(10mVx38)
07h	VCOM-(10mVx57)	27h	VCOM-(10mVx25)	47h	VCOM+(10mVx7)	67h	VCOM+(10mVx39)
08h	VCOM-(10mVx56)	28h	VCOM-(10mVx24)	48h	VCOM+(10mVx8)	68h	VCOM+(10mVx40)
09h	VCOM-(10mVx55)	29h	VCOM-(10mVx23)	49h	VCOM+(10mVx9)	69h	VCOM+(10mVx41)
0Ah	VCOM-(10mVx54)	2Ah	VCOM-(10mVx22)	4Ah	VCOM+(10mVx10)	6Ah	VCOM+(10mVx42)
0Bh	VCOM-(10mVx53)	2Bh	VCOM-(10mVx21)	4Bh	VCOM+(10mVx11)	6Bh	VCOM+(10mVx43)
0Ch	VCOM-(10mVx52)	2Ch	VCOM-(10mVx20)	4Ch	VCOM+(10mVx12)	6Ch	VCOM+(10mVx44)
0Dh	VCOM-(10mVx51)	2Dh	VCOM-(10mVx19)	4Dh	VCOM+(10mVx13)	6Dh	VCOM+(10mVx45)
0Eh	VCOM-(10mVx50)	2Eh	VCOM-(10mVx18)	4Eh	VCOM+(10mVx14)	6Eh	VCOM+(10mVx46)
0Fh	VCOM-(10mVx49)	2Fh	VCOM-(10mVx17)	4Fh	VCOM+(10mVx15)	6Fh	VCOM+(10mVx47)
10h	VCOM-(10mVx48)	30h	VCOM-(10mVx16)	50h	VCOM+(10mVx16)	70h	VCOM+(10mVx48)
11h	VCOM-(10mVx47)	31h	VCOM-(10mVx15)	51h	VCOM+(10mVx17)	71h	VCOM+(10mVx49)
12h	VCOM-(10mVx46)	32h	VCOM-(10mVx14)	52h	VCOM+(10mVx18)	72h	VCOM+(10mVx50)
13h	VCOM-(10mVx45)	33h	VCOM-(10mVx13)	53h	VCOM+(10mVx19)	73h	VCOM+(10mVx51)
14h	VCOM-(10mVx44)	34h	VCOM-(10mVx12)	54h	VCOM+(10mVx20)	74h	VCOM+(10mVx52)
15h	VCOM-(10mVx43)	35h	VCOM-(10mVx11)	55h	VCOM+(10mVx21)	75h	VCOM+(10mVx53)
16h	VCOM-(10mVx42)	36h	VCOM-(10mVx10)	56h	VCOM+(10mVx22)	76h	VCOM+(10mVx54)
17h	VCOM-(10mVx41)	37h	VCOM-(10mVx9)	57h	VCOM+(10mVx23)	77h	VCOM+(10mVx55)
18h	VCOM-(10mVx40)	38h	VCOM-(10mVx8)	58h	VCOM+(10mVx24)	78h	VCOM+(10mVx56)
19h	VCOM-(10mVx39)	39h	VCOM-(10mVx7)	59h	VCOM+(10mVx25)	79h	VCOM+(10mVx57)
1Ah	VCOM-(10mVx38)	3Ah	VCOM-(10mVx6)	5Ah	VCOM+(10mVx26)	7Ah	VCOM+(10mVx58)
1Bh	VCOM-(10mVx37)	3Bh	VCOM-(10mVx5)	5Bh	VCOM+(10mVx27)	7Bh	VCOM+(10mVx59)
1Ch	VCOM-(10mVx36)	3Ch	VCOM-(10mVx4)	5Ch	VCOM+(10mVx28)	7Ch	VCOM+(10mVx60)
1Dh	VCOM-(10mVx35)	3Dh	VCOM-(10mVx3)	5Dh	VCOM+(10mVx29)	7Dh	VCOM+(10mVx61)
1Eh	VCOM-(10mVx34)	3Eh	VCOM-(10mVx2)	5Eh	VCOM+(10mVx30)	7Eh	VCOM+(10mVx62)
1Fh	VCOM-(10mVx33)	3Fh	VCOM-(10mVx1)	5Fh	VCOM+(10mVx31)	7Fh	VCOM+(10mVx63)

Packaging Information

QFN3.5X3.5-28



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.6	0.0197	0.0217	0.0236
A1	0.00	0.02	0.05	0.0000	0.0008	0.0020
A2	0.15 REF			0.0059 REF		
D	3.40	3.50	3.60	0.1339	0.1378	0.1417
E	3.40	3.50	3.60	0.1339	0.1378	0.1417
D1	0.90	1.00	1.10	0.0354	0.0394	0.0433
E1	0.90	1.00	1.10	0.0354	0.0394	0.0433
b	0.15	0.20	0.25	0.0059	0.0079	0.098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Revision History

Revision	Date	Change Description
Rev 0.1p0	10/16/2024	Product Brief
Rev 0.2px	12/18/2024	Fixed some descriptive errors
Rev 0.3p45	03/20/2025	Add a version history description page
Rev 0.3p4	03/20/2025	Modify the Description of PIN19