



Features

- Wide Input Voltage Range: 1.8V to 5.5V
- Fixed Output Voltage: 1.2V, 1.8V, 2.8V, 3.3V
- Maximum Load Current: 300mA
- High PSRR at Full Frequency Range:
 - 85dB@1kHz
 - 66dB@10kHz
 - 59dB@100kHz
- Low Noise: $42\mu V_{RMS}$, $V_{OUTX}=2.8V$
- Low Quiescent Current: 120 μA typical
- Low Dropout Voltage:
 - 66mV @ 100mA Load, $V_{OUTX}=2.8V$
 - 200mV @ 300mA Load, $V_{OUTX}=2.8V$
- Output Voltage Accuracy: $\pm 2\%$ @ 1mA
- Short Circuit Current Limit: 110mA
- Thermal Shutdown Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.01%/V typical
- Load Regulation: 18mV typical (1mA to 300mA)
- Robust ESD capability:
 - Human Body Model: 4kV
 - Charged Device Model: 1kV
- Package: SOT23-6
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Digital cameras
- Audio devices
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Post regulation
- Wireless handsets

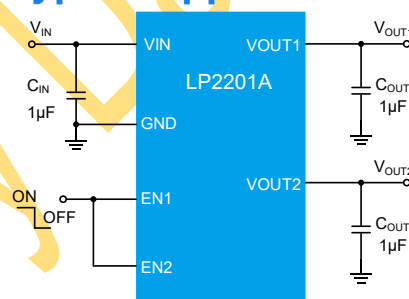
General Description

The LP2201A family are dual channel, high performance low dropout (LDO) voltage regulators with high PSRR, fast transient response, high accuracy, and low output noise. The devices with advanced CMOS process are suitable for many applications that require regulated supplies of up to 300mA load current each channel.

The family include standard fixed output voltages of 1.2V, 1.8V, 2.8V, and 3.3V. The devices are stable with a minimum effective 0.5 μF capacitance output capacitor. The devices are protected from short circuit by a current limit function and from over-heating by a thermal overload protection.

The devices are available in SOT23-6 package.

Typical Application Circuit



Order Information

LP2201A-

F: Pb Free
 Package Type
 B6: SOT23-6

OUT1/OUT2 Voltage
 18/28: 1.8V/2.8V
 18/33: 1.8V/3.3V
 28/12: 2.8V/1.2V
 12/28: 1.2V/2.8V
 12/33: 1.2V/3.3V



Device Information

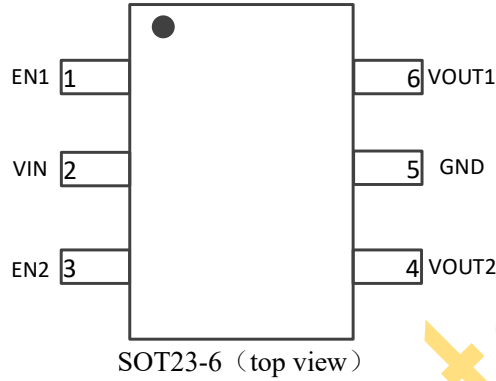
Part Number	Top Marking	OUT1/OUT2 Voltage	Moisture Sensitivity Level	Package	Shipping
LP2201A-28/12B6F	LPS HbYWX	2.8V/1.2V	MSL3	SOT23-6	3K/REEL
LP2201A-18/28B6F	LPS CHYWX	1.8V/2.8V	MSL3	SOT23-6	3K/REEL
LP2201A-12/28B6F	LPS BHYWX	1.2V/2.8V	MSL3	SOT23-6	3K/REEL
LP2201A-18/33B6F	LPS CEYWX	1.8V/3.3V	MSL3	SOT23-6	3K/REEL

Marking indication:

Y: Year code. W: Week code. X: Batch numbers.



Pin Diagram

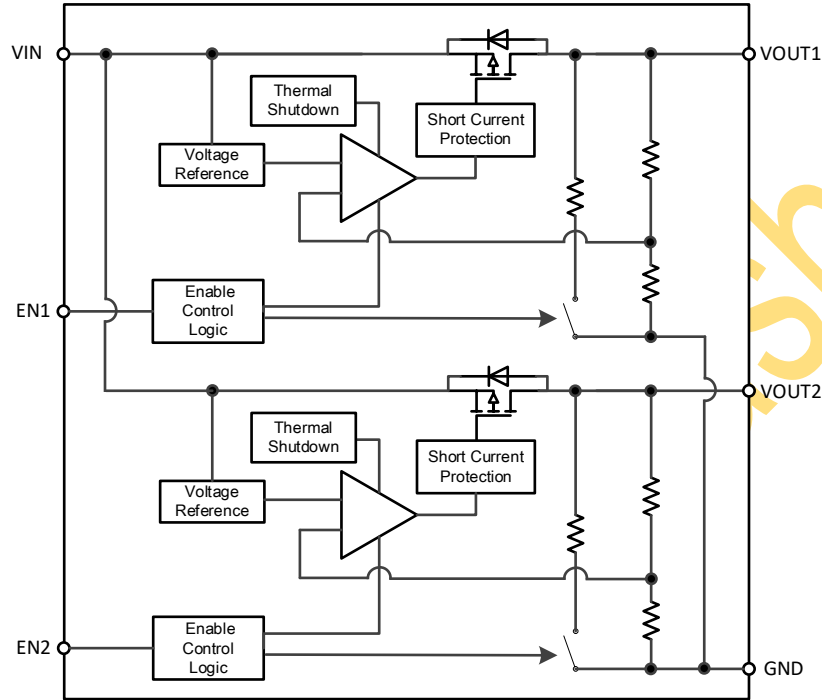


Pin Description

Pin	Name	Description
1	EN1	Channel 1 enable pin. Active high. Driving EN over 1V turns on the regulator 1. Driving EN below 0.4V puts the regulator 1 into shutdown mode. A built-in 200nA(typical) pull-up current is connected to the pin. If the pin is floating, the VOUT1 is active.
2	VIN	Supply input pin. Must be closely decoupled to GND with a 1 μ F or greater ceramic capacitor. Place the capacitor as close as to the pin as possible.
3	EN2	Channel 2 enable pin. Active high. Driving EN over 1V turns on the regulator 2. Driving EN below 0.4V puts the regulator 2 into shutdown mode. A built-in 200nA(typical) pull-up current is connected to the pin. If the pin is floating, the VOUT2 is active.
4	VOUT2	Channel 2 output pin. Bypass with a 1 μ F or greater ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.
5	GND	Ground.
6	VOUT1	Channel 1 output pin. Bypass with a 1 μ F or greater ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.



Functional Block Diagram



Absolute Maximum Ratings (Note 1)

VIN Pin to GND	-----	-0.3~6.5V
VOUTx, ENx Pin to GND	-----	-0.3~VIN
Maximum Junction Temperature (T _J)	-----	150°C
Operating Ambient Temperature Range (T _A)	-----	-40°C to 85°C
Maximum Soldering Temperature (at leads, 10 sec)	-----	260°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

Maximum Power Dissipation (SOT23-6, P _D , T _A ≤ 25°C)	-----	800mW
Thermal Resistance (SOT23-6, θ _{JA}) (Note 2)	-----	156 °C/W

Note 2: Measured using 2S2P JEDEC standard PCB with ambient temperature < 25°C

ESD Susceptibility

HBM (Human Body Model)	-----	4kV
CDM (Charged Device Model)	-----	1kV

Recommended Operating Conditions

Input Voltage	-----	1.8V to 5.5V
Operating Junction Temperature Range (T _J)	-----	-40°C to 150°C
Ambient Temperature Range	-----	-40°C to 85°C



Electrical Characteristics

(The specifications are at $T_A=25^\circ\text{C}$, $V_{IN} = V_{OUTX} + 1\text{V}$, $C_{IN}=C_{OUTX}=1\mu\text{F}$ for each channel, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Operation Range		1.8		5.5	V
I_{inrush}	Inrush Current	$V_{EN1}=V_{EN2}=V_{IN}$, $C_{OUT1}=C_{OUT2}=10\mu\text{F}$, 2-channels together		800		mA
I_Q	DC Supply Quiescent Current	$V_{EN1}=V_{EN2}=V_{IN}$, $I_{OUT1}=I_{OUT2}=0\text{mA}$ 2-channels together		120		μA
I_{SD}	Shutdown Current	$V_{EN1}=V_{EN2}=0\text{V}$, 2-channels together		1.2		μA
REGULATED OUTPUT						
$ACC_{V_{OUT}}$	Output Voltage Accuracy	$I_{OUT}=1\text{mA}$	-2%		2%	
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	Output Voltage Line Regulation	$V_{IN}=V_{OUT}+0.5\text{V}\sim 5.5\text{V}$ $I_{OUT}=1\text{mA}$		0.01		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{OUT} from 1mA to 300mA		18	36	mV
$T_{CV_{OUT}}$	V_{OUT} Temperature Coefficient	$I_{OUT}=1\text{mA}$		0.01		%/ $^\circ\text{C}$
I_{OUT_MAX}	Max Load Current	$V_{EN}=V_{IN}$	300			mA
I_{LIMIT}	Load Current Limit	$V_{EN}=V_{IN}$	400	550		mA
I_{SHORT}	Short Current	$V_{EN}=V_{IN}$ V_{OUT} short to GND		110		mA
V_{DROP}	Dropout Voltage	$V_{OUT}=1.8\text{V}$, $I_{OUT}=300\text{mA}$		320		mV
		$V_{OUT}=2.8\text{V}$, $I_{OUT}=300\text{mA}$		200		
		$V_{OUT}=3.3\text{V}$, $I_{OUT}=300\text{mA}$		180		
$PSRR$	Power Supply Rejection Ratio	$V_{IN}=(V_{OUT}+1\text{V})_{DC}$ +0.2V _{P-P} , $I_{OUT}=20\text{mA}$, $V_{OUT}=2.8\text{V}$	$f=100\text{Hz}$	82		dB
			$f=1\text{kHz}$	85		
			$f=10\text{kHz}$	66		
			$f=100\text{kHz}$	59		
e_N	Output Noise	10Hz~100kHz $I_{OUT}=20\text{mA}$	$V_{OUT}=1.2\text{V}$	29		μV_{RMS}
			$V_{OUT}=1.8\text{V}$	45		
			$V_{OUT}=2.8\text{V}$	42		
			$V_{OUT}=3.3\text{V}$	48		



THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			160		°C
ΔT_{SD}	Thermal Shutdown Hysteresis			20		°C
SOFTSTART AND DISCHARGE						
t_{RISE}	V_{OUT} Rise Time	$I_{OUT}=0mA$		30		μs
R_{DISC}	Auto-discharge On-Resistance			130		Ω
ENx PIN						
V_{ENH}	EN Logic High Voltage		1.0			V
V_{ENL}	EN Logic Low Voltage			0.4		V
I_{EN}	EN Input Current	$V_{EN}=0$ to 5.5V		120		nA



Typical Characteristics

(The specifications are at $T_A=25^\circ\text{C}$, $V_{IN} = V_{OUTX}+1\text{V}$, $C_{IN}=C_{OUTX}=1\mu\text{F}$ for each channel, unless otherwise noted.)

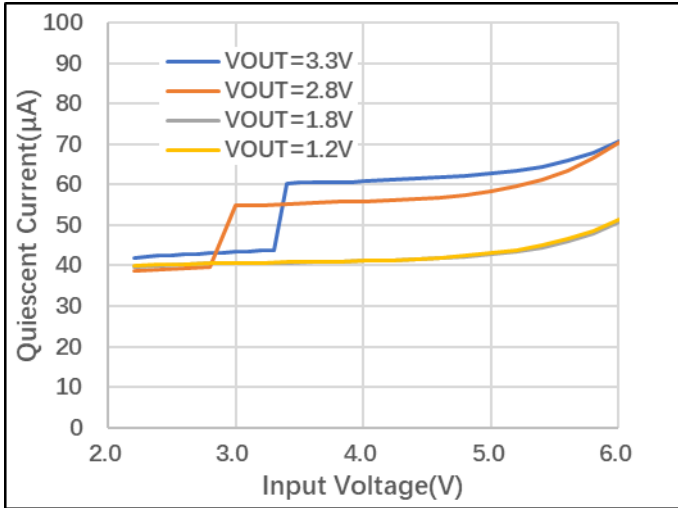


Figure 1. Quiescent current of each channel vs input voltage

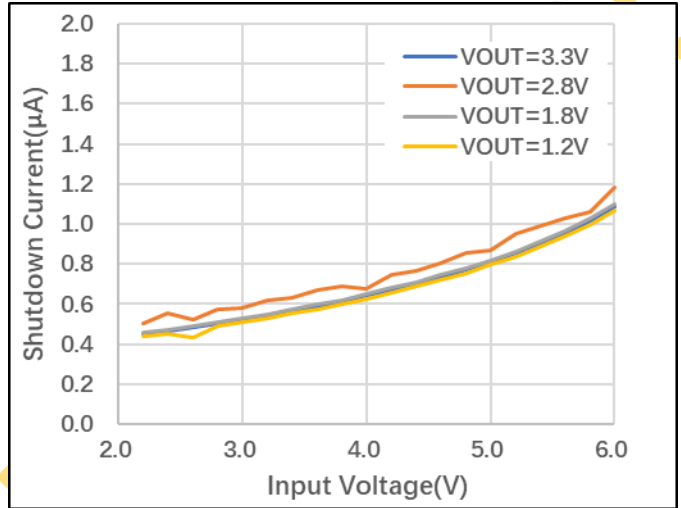


Figure 2. Shutdown current of each channel vs input voltage

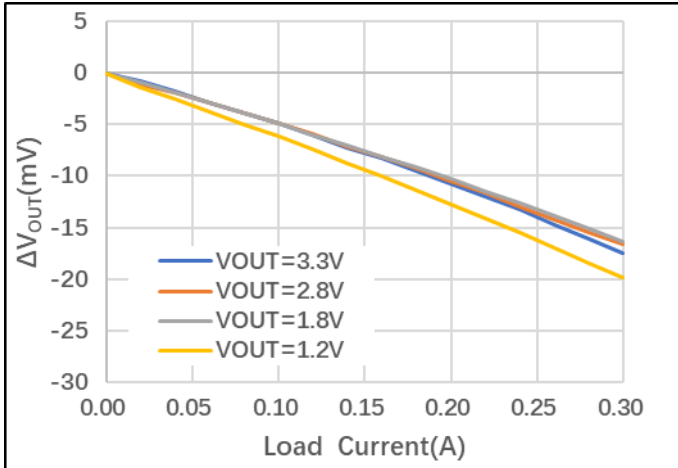


Figure 3. ΔV_{OUT} vs load current, $V_{IN}=V_{OUT}+1\text{V}$,

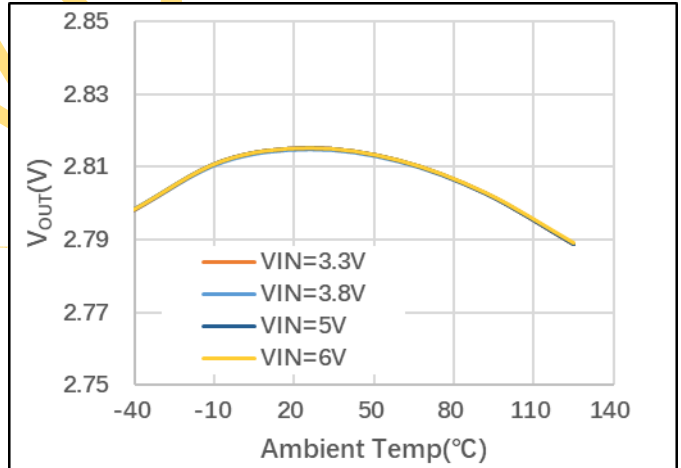


Figure 4. V_{OUT} vs Ambient Temperature,
 $V_{OUTX}=2.8\text{V}$, $I_{OUT}=1\text{mA}$

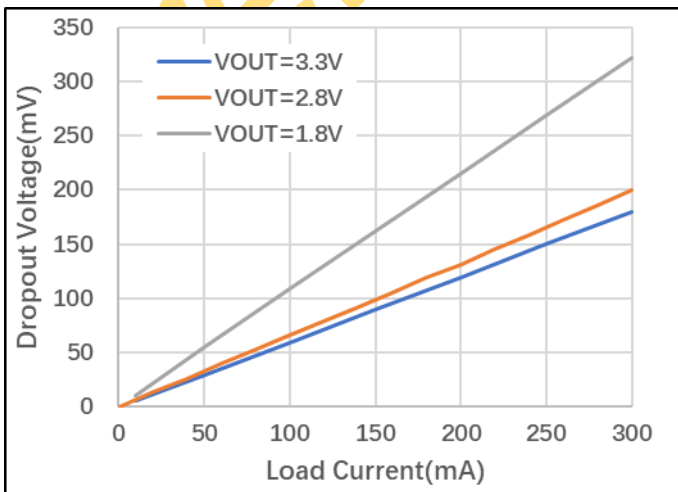


Figure 5. Dropout Voltage vs Load Current,

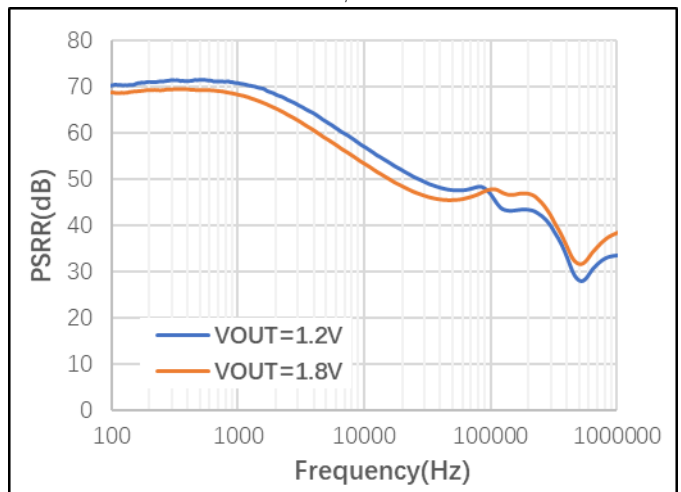


Figure 6. PSRR vs Frequency with $V_{OUT}=1.2\text{V}/1.8\text{V}$
 $I_{OUT}=20\text{mA}$, $V_{IN}=V_{OUT}+1\text{V}$, $C_{OUT}=1\mu\text{F}$,

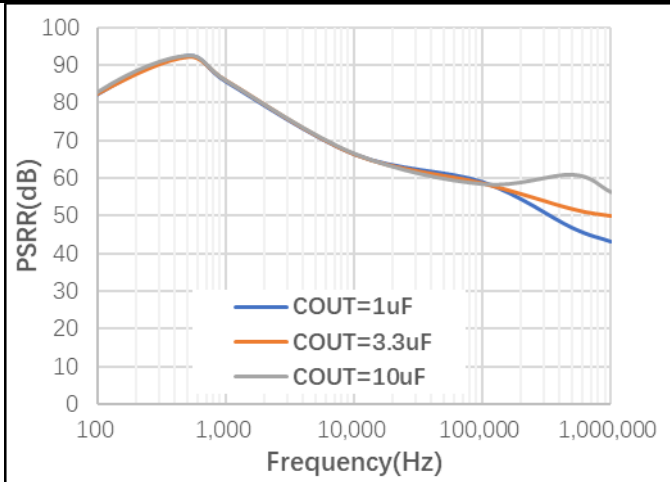


Figure 7. PSRR vs Frequency when $V_{OUT}=2.8V$
 $I_{OUT}=20mA$, $V_{IN}=V_{OUT}+1V$,

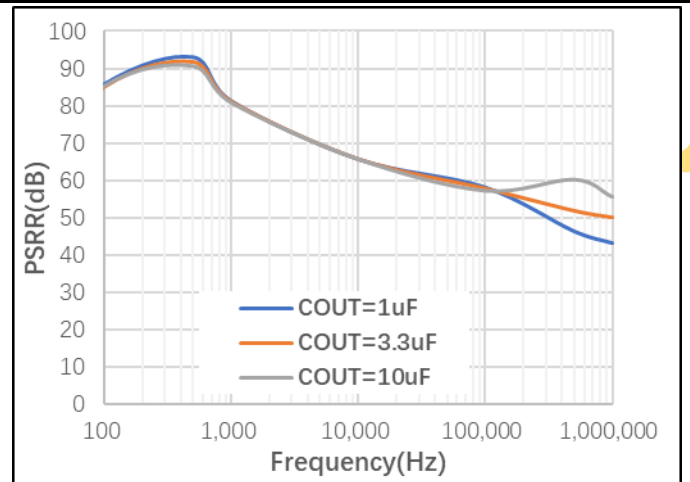


Figure 8. PSRR vs Frequency when $V_{OUT}=3.3V$
 $I_{OUT}=20mA$, $V_{IN}=V_{OUT}+1V$,

Preliminary Data



Load Transient: $I_{OUT}=1mA \leftrightarrow 300mA$ in $1\mu s$

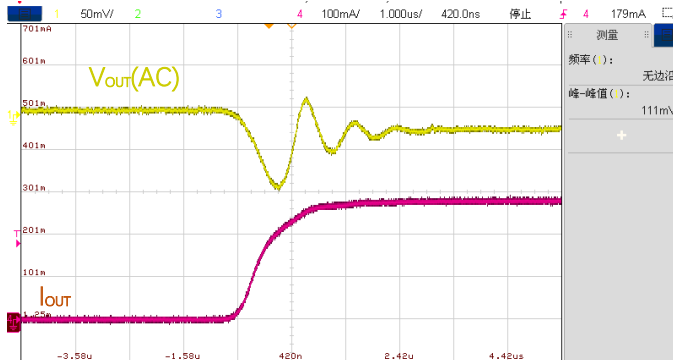


Figure 9. Load Transient 1mA->300mA,
 $V_{IN}=3.3V, V_{OUT}=1.2V$

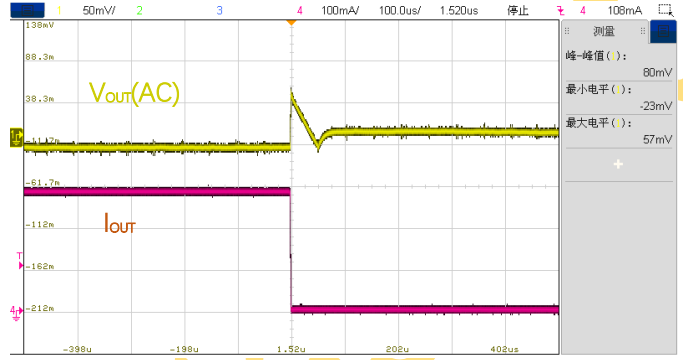


Figure 10. Load Transient 300mA->1mA,
 $V_{IN}=3.3V, V_{OUT}=1.2V$

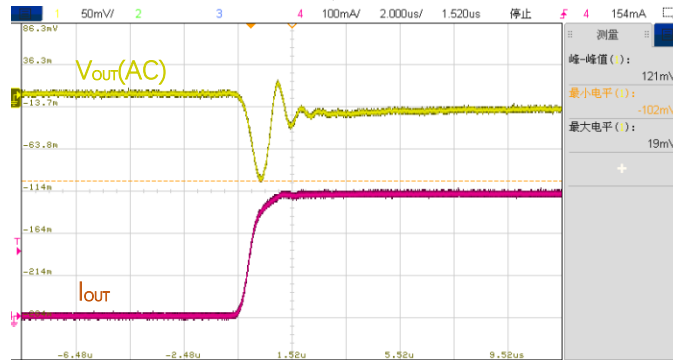


Figure 11. Load Transient 1mA->300mA,
 $V_{IN}=3.3V, V_{OUT}=1.8V$

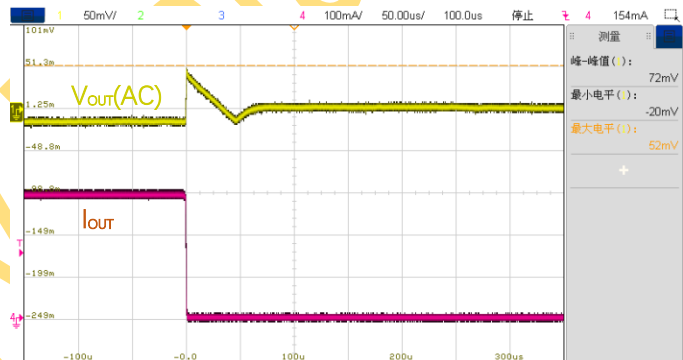


Figure 12. Load Transient 300mA->1mA,
 $V_{IN}=3.3V, V_{OUT}=1.8V$

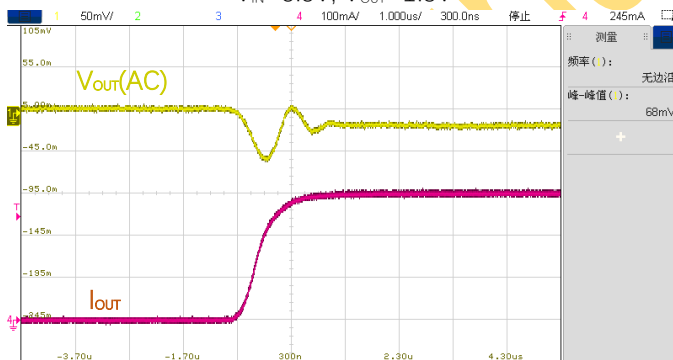


Figure 13. Load Transient 1mA->300mA,
 $V_{IN}=3.8V, V_{OUT}=2.8V$

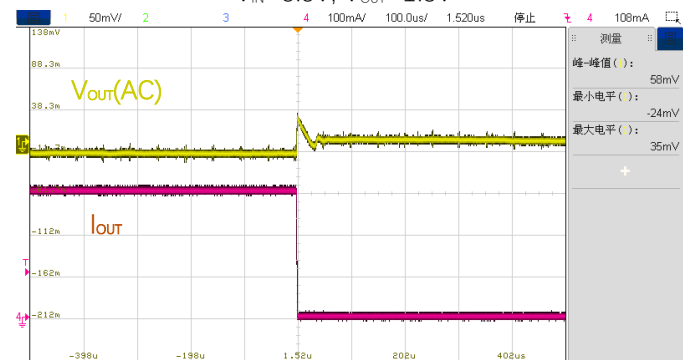


Figure 14. Load Transient 300mA->1mA,
 $V_{IN}=3.8V, V_{OUT}=2.8V$

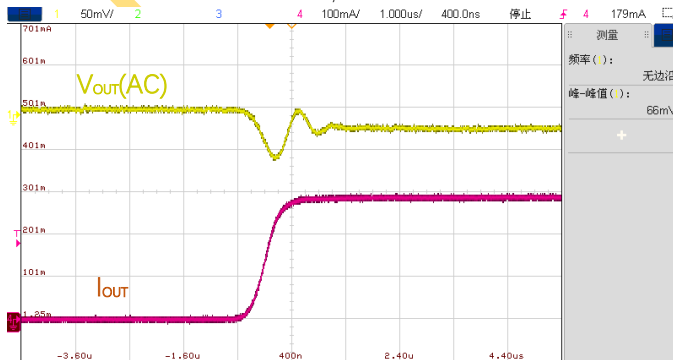


Figure 15. Load Transient 1mA->300mA,
 $V_{IN}=4.3V, V_{OUT}=3.3V$

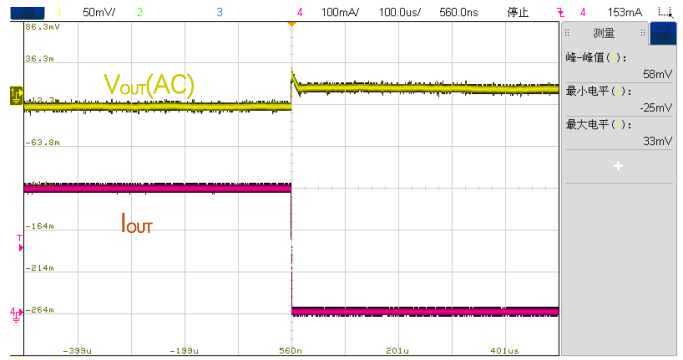


Figure 16. Load Transient 300mA->1mA,
 $V_{IN}=4.3V, V_{OUT}=3.3V$



Line Transient: $V_{IN}=V_{OUT}+1V \leftarrow \rightarrow V_{OUT}+2V$ in 10 μ s

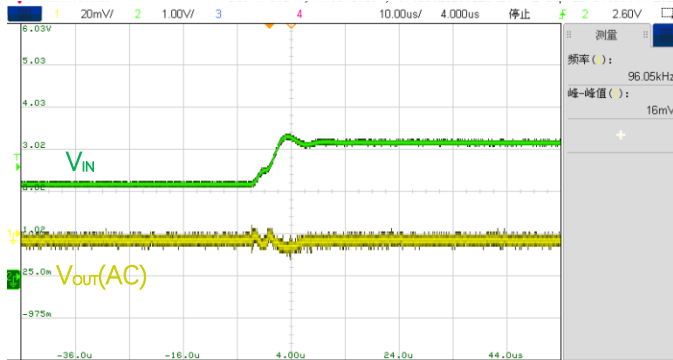


Figure 17. Line Transient $V_{IN}=2.2V \rightarrow 3.2V$,
 $V_{OUT}=1.2V$, $I_{OUT}=100mA$

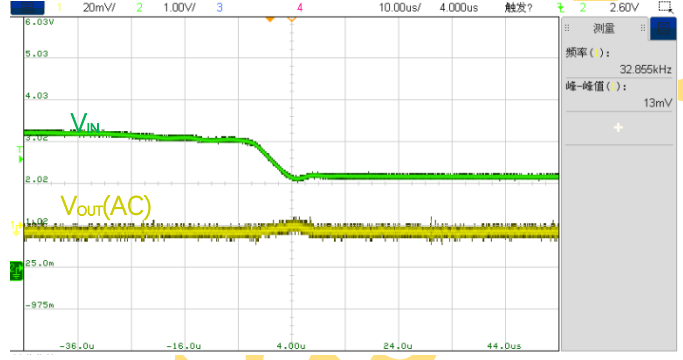


Figure 18. Line Transient $V_{IN}=3.2V \rightarrow 2.2V$,
 $V_{OUT}=1.2V$, $I_{OUT}=100mA$

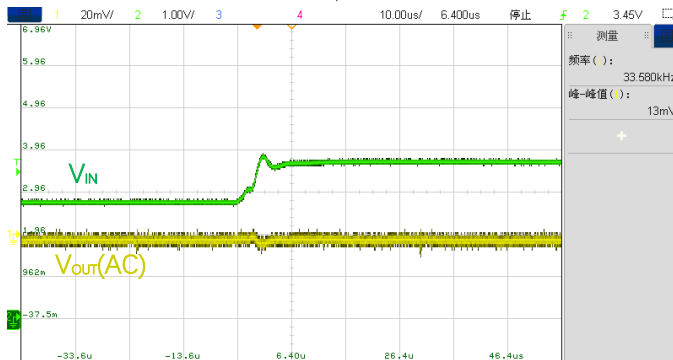


Figure 19. Line Transient $V_{IN}=2.8V \rightarrow 3.8V$,
 $V_{OUT}=1.8V$, $I_{OUT}=100mA$

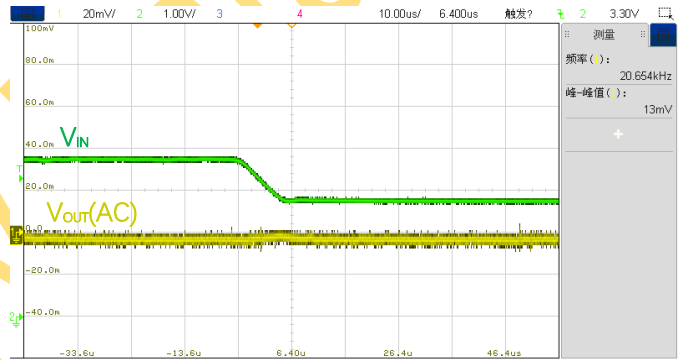


Figure 20. Line Transient $V_{IN}=3.8V \rightarrow 2.8V$,
 $V_{OUT}=1.8V$, $I_{OUT}=100mA$

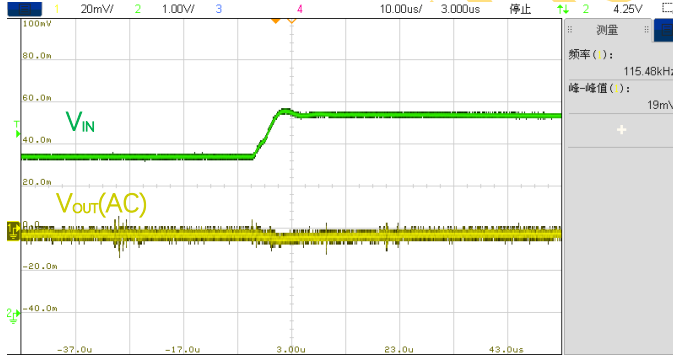


Figure 21. Line Transient $V_{IN}=3.8V \rightarrow 4.8V$,
 $V_{OUT}=2.8V$, $I_{OUT}=100mA$

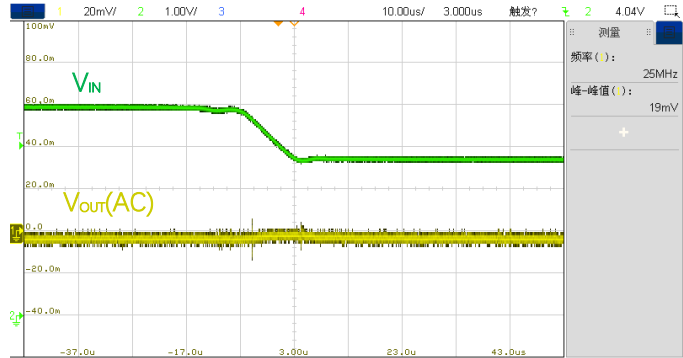


Figure 22. Line Transient $V_{IN}=4.8V \rightarrow 3.8V$,
 $V_{OUT}=2.8V$, $I_{OUT}=100mA$

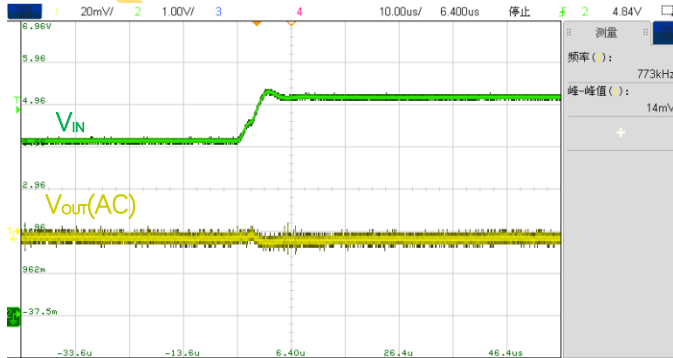


Figure 23. Line Transient $V_{IN}=4.3V \rightarrow 5.3V$,
 $V_{OUT}=3.3V$, $I_{OUT}=100mA$

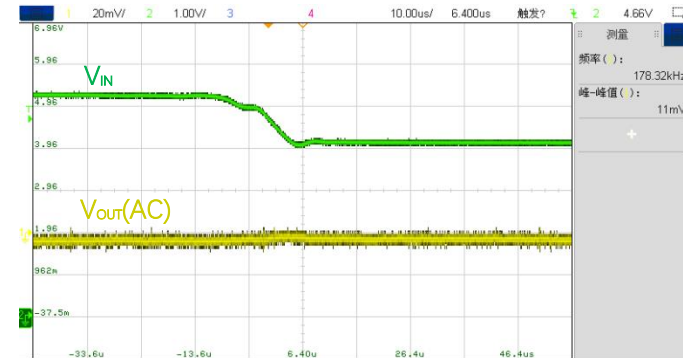


Figure 24. Line Transient $V_{IN}=5.3V \rightarrow 4.3V$,
 $V_{OUT}=3.3V$, $I_{OUT}=100mA$



Detailed Description

Overview

The LP2201A family are dual channel, high performance, low dropout linear regulators with fixed 1.2V, 1.8V, 2.8V, and 3.3V output voltages. The family with low output noise and high PSRR are suited for high performance applications. Optimized for using with ceramic capacitors, the device provides excellent transient performance.

Internally, each channel LDO consists of a voltage reference, an enable control logic, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares a reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

Enable Function

The EN_x pin is an active high logic input pin. The internal power element is turned off when EN_x pin is tied low. When the EN_x pin is pulled high, the corresponding channel will be activated and output voltage according to the setting. Please pay attention to that there is a built-in 200nA(typical) pull-up current connected to the EN_x pin. If the EN_x pin is floating, the chip will be active. If don't need enable the chip, please connect a pull-down resistor which the resistance should be lower than 1MΩ.

Auto Discharge

Each channel of LP2201A family have a quick discharge function. When the channel is disabled by the pulled-down EN_x pin, a discharge resistor is connected between VOUT_x and GND. The resistance is 850Ω typically.

Short Current Limit Protection

When the output current at the VOUT_x pin is higher than current limit threshold or the VOUT_x pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 110mA to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

When the internal junction temperature of LP2201A family devices exceed the junction thermal shutdown threshold (160°C typical), the devices will shut down the output, after the junction temperature falls below 140°C , the VOUT voltage will resume.



Application Description

Thermal Consideration

The reason that causes thermal shutdown protection of an LP2201A device is the power dissipation. Nearly all of the power dissipation is generated by the internal PMOS pass device. The power dissipation can be calculated approximately as,

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

where P_D is the power dissipation.

The worst-case situation is when the device has the maximum input voltage of 5.5V and the maximum load current of 300mA for each channel. In this situation, the device dissipates the maximum power,

$$P_{Dmax} = (5.5V - 1.2V) \times 300mA = 1.29W$$

This power dissipation of the LDO device in the SOT23-6 package will trigger thermal shutdown protection at high ambient temperature. Then a trade-off must be made between the output current, cost, and thermal requirements of the application.

Input Capacitor

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. A 1 μ F-10 μ F ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitches and noise. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

The LP2201A devices require a minimum output capacitance of 1 μ F for output voltage stability for each channel. The recommended output effective capacitance is from 1 μ F to 10 μ F, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as practically possible.

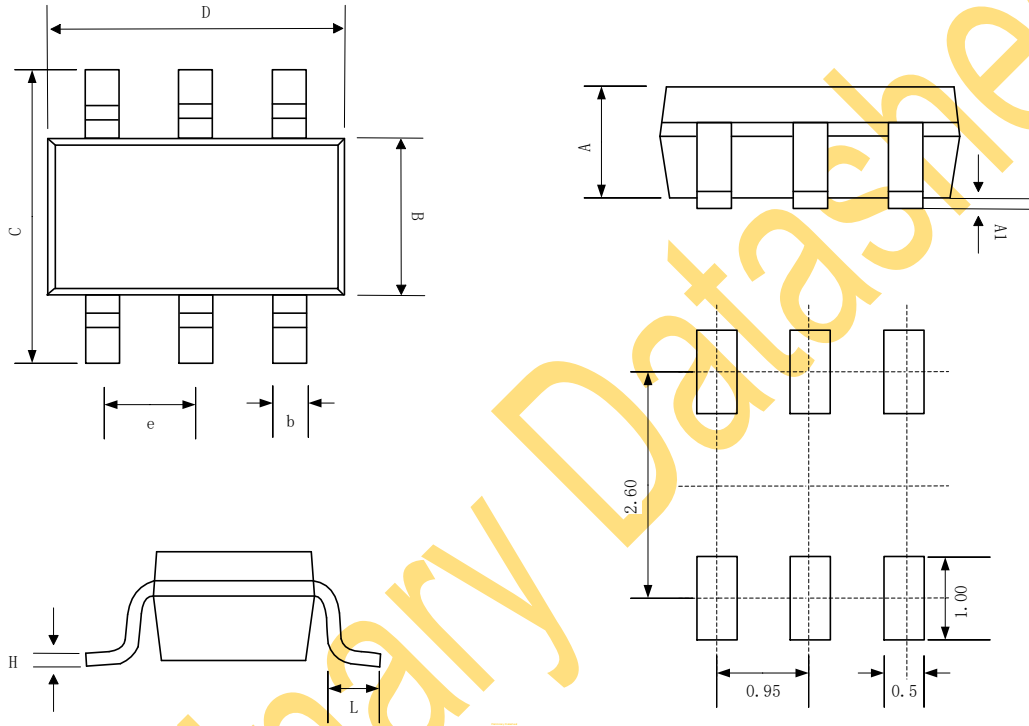
Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practically possible to the respective LDO pins. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible with a wide and component-side copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device.



Packaging Information

SOT23-6



Recommended Land Pattern

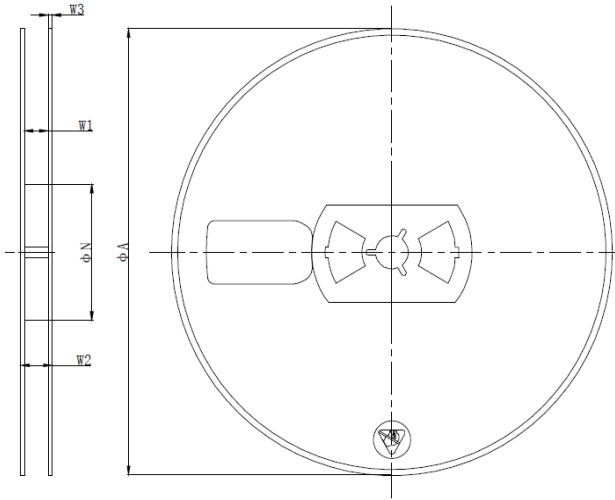
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610



Tape and Reel Information

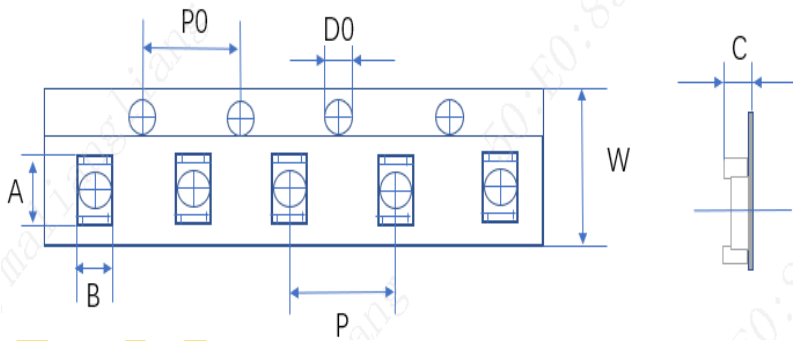
SOT23-6

REEL DIMENSIONS



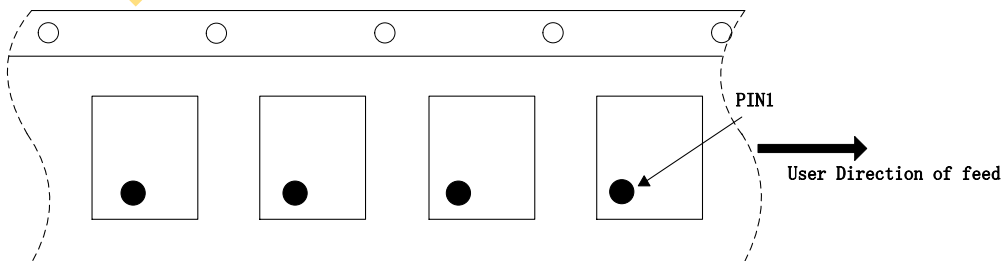
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	3.06	3.26	3.46
P0	3.90	4.00	4.10
P	3.90	4.00	4.10
D0	1.35	1.50	1.65
W	7.70	8.00	8.30
C	1.20	1.40	1.60

PIN1 AND TAPE FEEDING DIRECTION





Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100°C	150°C
Temperature Max(T_{SMAX})	150°C	200°C
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max	3°C/second max
Liquidous temperature(T_L)	183°C	217°C
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5°C of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6°C/second max	6°C/second max
Time 25°C to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1 Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5mm	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350~2000	Volume mm ³ ≥350
<1.6mm	260°C	260°C	260°C
1.6mm~2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

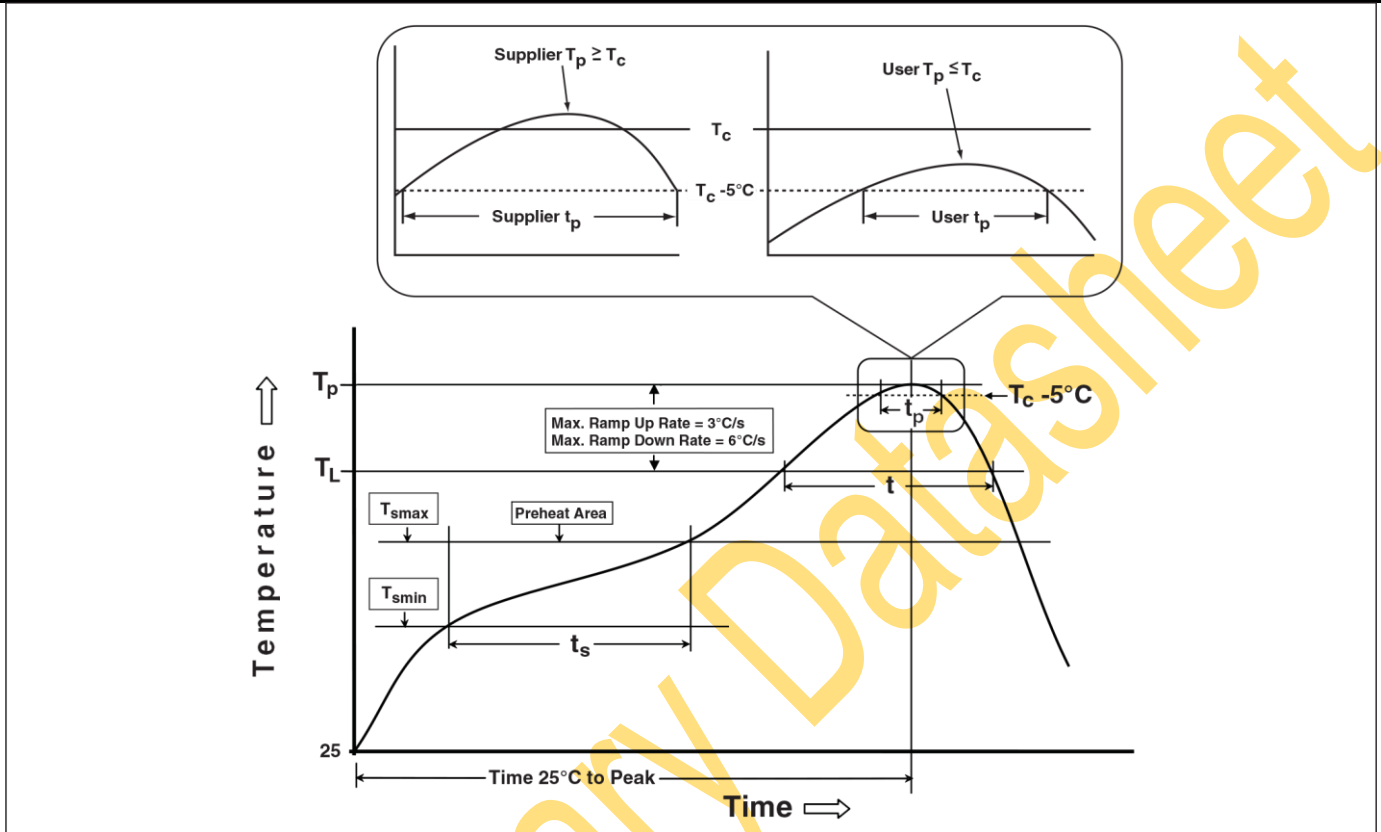


Figure1 Classification Profile (Not to scale)

Products conform to “JEDEC J-STD-020C” standards;

Products shipped conform to “Rohs” standards;

Moisture Sensitivity Level: MSL3 (CONDITION: $\leq 30\text{ }^{\circ}\text{C}/60\%\text{RH}$ 、Time control:168 hours) ;