300mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3983S is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3983S performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3983S also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3983S consumes less than 0.1μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. It is available in SOT23-5 packages.

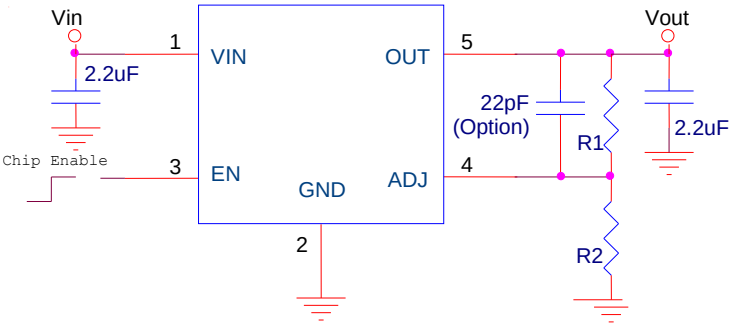
Features

- Ultra-Low-Noise for RF Application
- 2V- 6V Input Voltage Range
- Low Dropout : 210mV @ 300mA
- 300mA Output Current, 550mA Peak Current
- High PSRR: -70dB at 217Hz
- < 1uA Standby Current When Shutdown
- Available in SOT23-5 Package
- Current Limiting and Thermal Shutdown Protection

Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Typical Application Circuit



Order Information

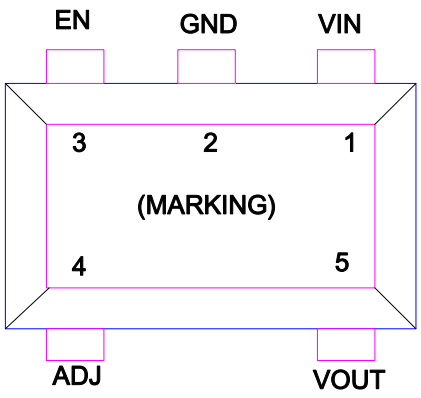
LP3983S □ □□ □ - □□

- FB Voltage: 08: 0.8V
- F: Pb-Free
- Package Type: B5: SOT23-5
- Output Type: A : Adjustable

Marking Information

Device	Marking	Package	Shipping
LP3983SAB5F-08	LPS 1FYWX	SOT23-5	3K/REEL
Marking indication: Y:Production year W:Production week X:Production batch			

Functional Pin Description

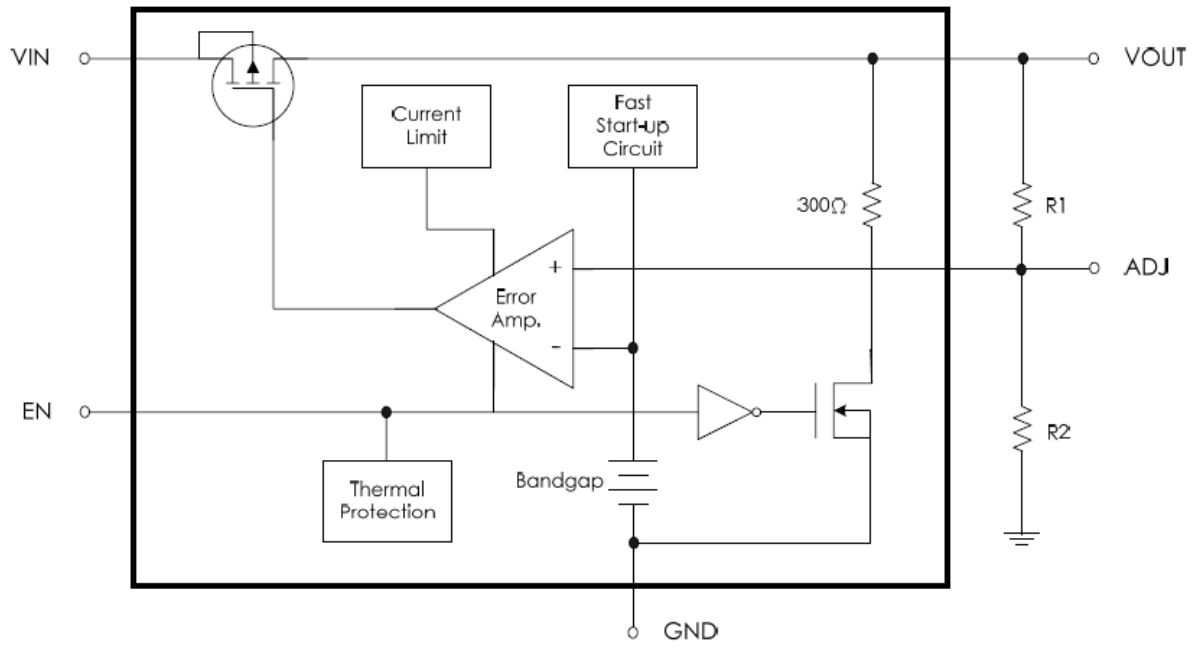
Package Type	Pin Configurations
SOT23-5	

SOT23-5

Pin Description

Pin	Name	Description
1	VIN	Power Input Voltage.
2	GND	Ground.
3	EN	Chip Enable (Active High). There is an integrated pull low 1MΩ resistor connected to GND when the control signal is floating.
4	ADJ	Adjustable pin.
5	VOUT	Output Voltage. $V_{out}=V_{FB}$ × (1+R1/R2)

Function Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ---------- 7V
- ✧ EN Pin Voltage ---------- -0.3V to Vin+0.3V

Power Dissipation, PD @ TA = 25℃

- ✧ Maximum Power Dissipation (PD,TA=25℃) ---------- 0.5W

Package Thermal Resistance

- ✧ Thermal Resistance (JA) ---------- 195℃/W
- ✧ Thermal Resistance (JC) ---------- 60℃/W
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
- ✧ Storage Temperature Range ---------- −60℃ to 125℃

ESD Susceptibility

- ✧ HBM (Human Body Mode) ---------- 2kV
- ✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

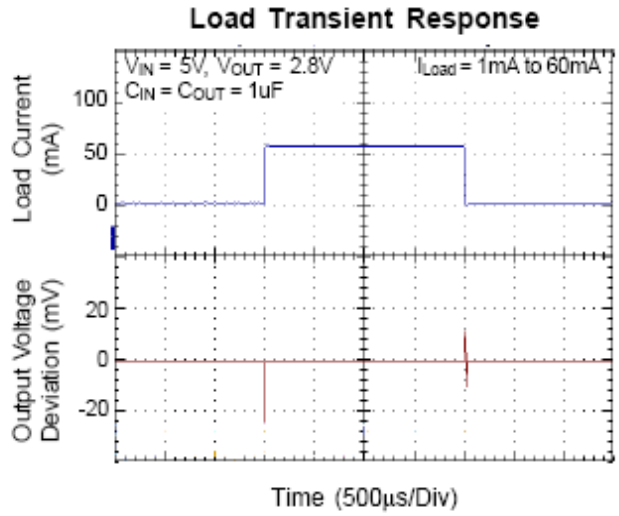
- ✧ Supply Input Voltage ---------- 2V to 6V
- ✧ Operation Junction Temperature Range ---------- −40℃ to 125℃
- ✧ Operation Ambient Temperature Range ---------- −40℃ to 85℃

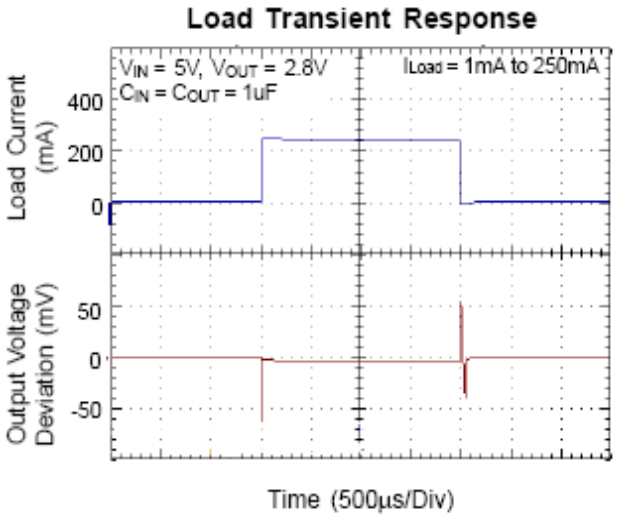
Electrical Characteristics

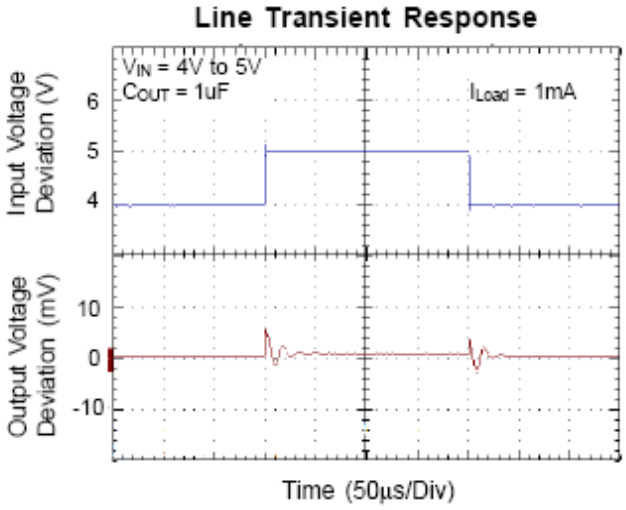
(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} =2.2μF, C_{FB} = 22pF, T_A = 25° C, unless otherwise specified)

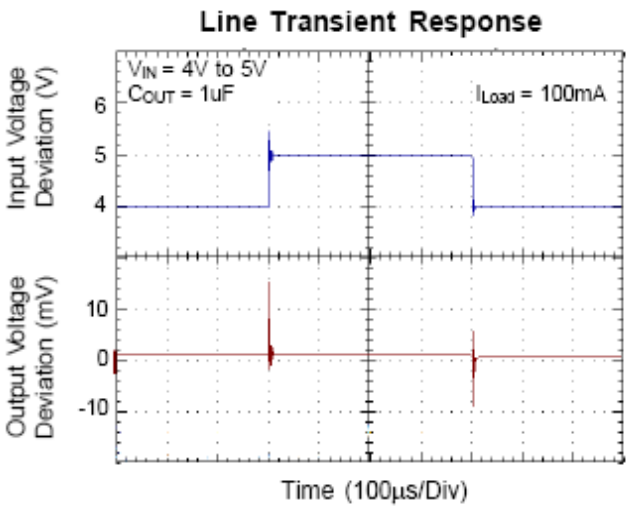
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Loading Current		I_{LOAD}	V_{EN}=V_{IN},V_{IN}>2.5V	300			mA
Current Limit		I_{LIM}	R_{LOAD} = 1Ω		550		mA
Adjustable voltage reference		V_{FB}	I_{OUT}=1mA	0.784	0.8	0.816	V
Quiescent Current		I_Q	V_{EN} ≥ 1.2V, I_{OUT} = 0mA		100	130	μA
Dropout Voltage		V_{DROP}	I_{OUT} = 200mA, V_{OUT} > 2.8V		140	180	mV
			I_{OUT} = 300mA, V_{OUT} > 2.8V		210	270	mV
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA			0.2	%
Load Regulation		ΔV_{LOAD}	1mA < IOUT < 300mA			2	%
Standby Current		I_{STBY}	V_{EN} = GND, Shutdown		0.1	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN} = GND or V_{IN}		5		uA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN}=3V to 5.5V, Start-Up	1.4		VIN+ 0.3	V
Output Noise Voltage			10Hz to 100kHz, I_{OUT}=200mA C_{OUT}=1μF		300		uVRMS
Power Supply Rejection Rate	f = 217Hz	PSRR	I_{OUT} = 100mA		−70		dB
	f = 1kHz				−58		dB
Thermal Shutdown Temperature		T_{SD}			150		℃

Typical Operating Characteristics





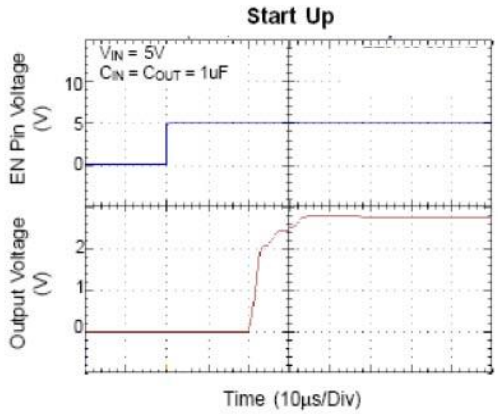




Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3983S must be carefully selected for regulator stability and performance. Using a capacitor whose value is >1μF on the LP3983S input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3983S is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LP3983S output ensures stability. The LP3983S still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the LP3983S and returned to a clean analog ground.

Start-up Function Enable Function



The LP3983S features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the LP3983S have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Feedback Capacitor

For adjustable version, connecting a 22pF between output pin and FB pin significantly reduces output voltage ripple, it is critical that the capacitor connection should be direct and PCB traces should be as short as possible.

The output voltage of LDO could be set by the formula below:

$$V_{out}=V_{FB} \times (1+R1/R2)$$

Considering the practical application, we may add a small capacitor with R1 in parallel which could be 22pF or 47pF.

Thermal Considerations

Thermal protection limits power dissipation in LP3983S. When the operation junction temperature exceeds 150℃, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25℃. For continue operation, do not exceed absolute maximum operation junction temperature 125℃.

The power dissipation definition in device is:

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

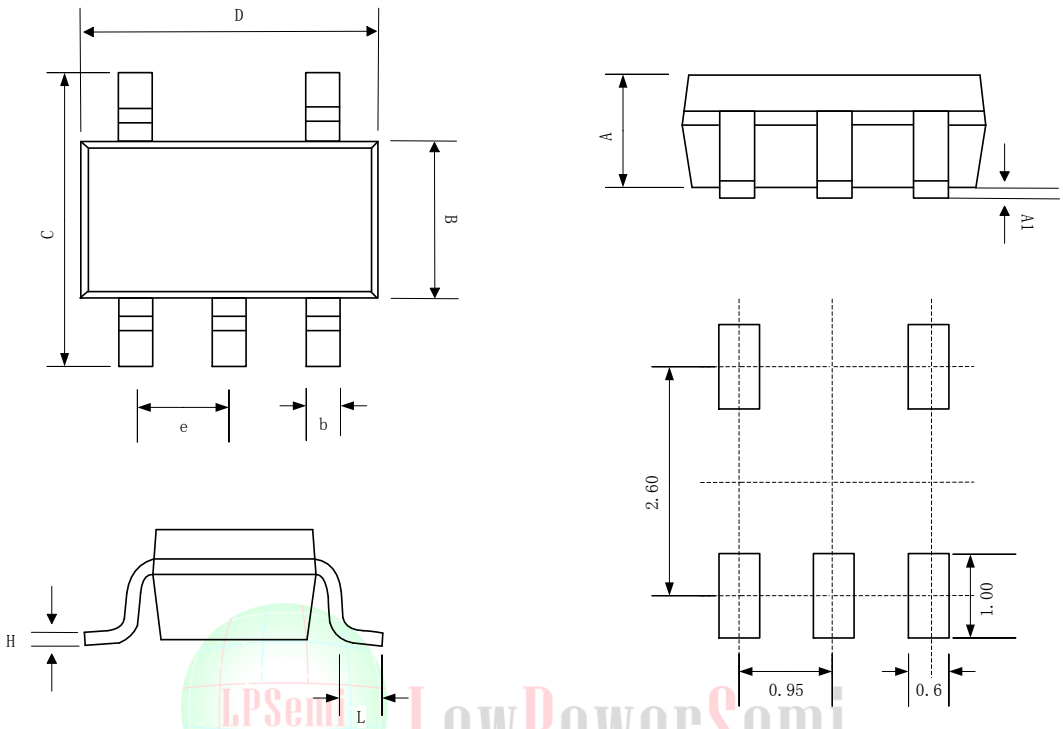
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125℃, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3983S, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125℃) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT23-5 package is 195℃/W.

$$P_{D(MAX)} = (125℃-25℃) /195 = 500mW$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}.

Packaging Information

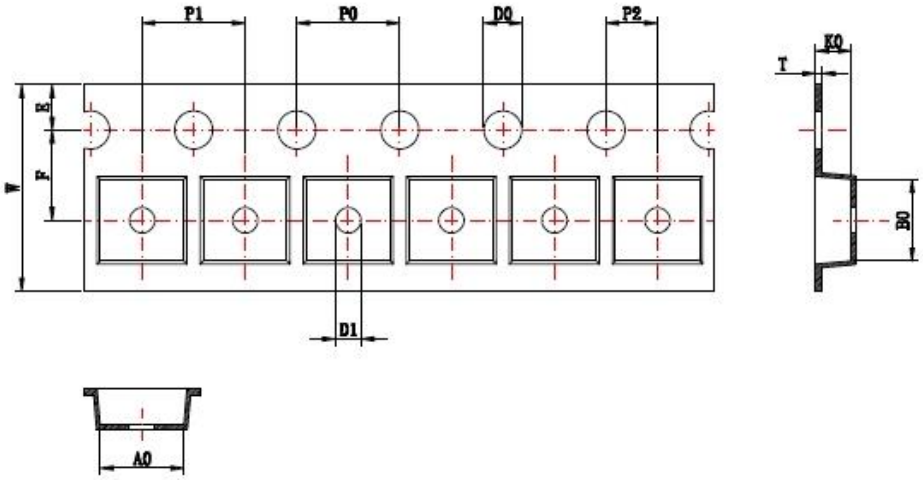
SOT23-5



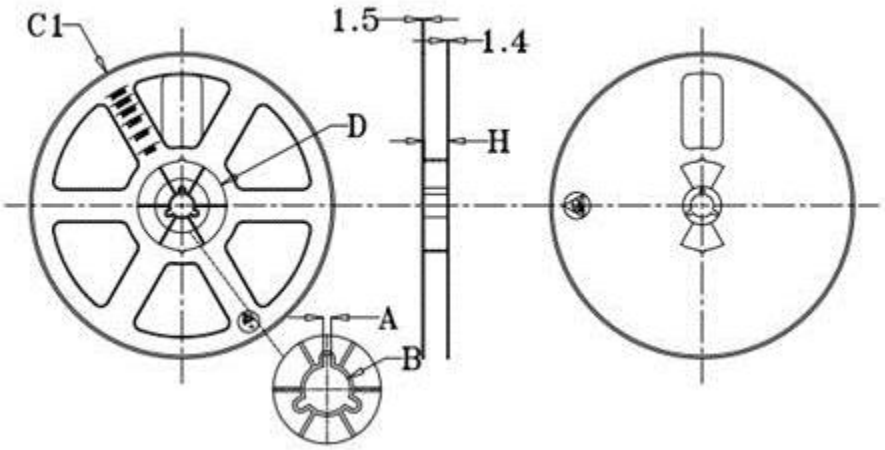
Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e		0.95BSC	
H	0.080	0.152	0.254
L	0.300	0.450	0.610

Tape And Reel Information



Symbol	Millimeters
A0	3.25±0.1
B0	3.17±0.1
D0	1.5
D1	1.0(MIN)
K0	1.4±0.1
P0	4.0±0.1
P1	4.0±0.1
P2	2.0±0.1
W	8.0±0.1
E	1.75±0.1
F	3.5±0.1



SPEC	8
C±1	178
A±0.2	3.6
B±0.2	14.6
D±0.5	52.8
H±0.2	8.5

Unit：mm

Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure 1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8 minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1 Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

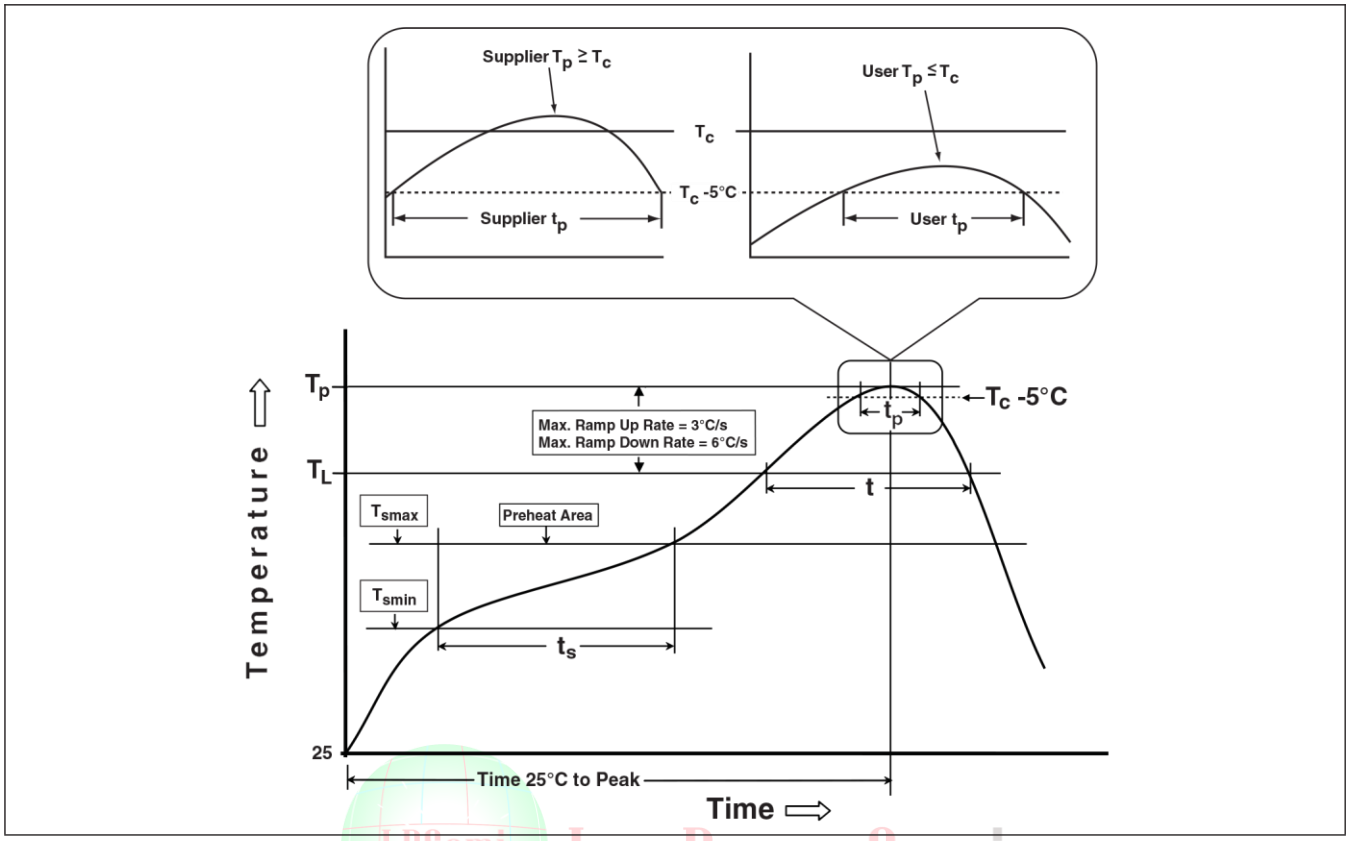


Figure 1 Classification Profile (Not to scale)

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control: 168 hours）;