

Features

- Input Supply Range
8.6V to 14.0V for TV
4.3V to 6.0V for MNT
- AVDD Async-Boost Converter:
13.5V to 19.8V for TV or 11.0V to 17.3V for MNT
500/750/1250KHz Switching Frequency
5A Switching Current limit
Controller by 0.3V Over-current Protection
- Programmable Internal/External V_{AVDD} Isolation PMOS
- VBK Sync Buck Converter: 1.8V to 3.35V
500/750/1250KHz Switching Frequency
2.0A Switching Current Limit
- HAVDD OP
1 Channel Programmable HAVDD OP
±250mA Output Current
7-bits DAC resolution
- VGH Async-Boost Converter Regulator: 20V to 42V
500/750/1250KHz Switching Frequency
1.5A Switching Current Limit
Temperature Compensation: 20V to 42V
- VGL Async-Inverting Converter: -3V to -18V
500/750/1250KHz Switching Frequency
1.5A Async Inverting Switching Current Limit
- VSS Negative Regulators: -3V to -16V
- 14-CH Gamma Buffers
14 Channels Rail-to-Rail Programmable Gamma Buffers
10 Bits Resolution for reach channel
- 1-CH VCOM1 Buffer
1 Channel Programmable VCOM Buffer
±150mA Output Current
7-Bits Resolution for reach Channel
- 1-CH VCOM2 Buffer
1 Channel Programmable VCOM DAC
±20mA Output Current
7-Bits Resolution for reach Channel
- Invtegrated MTP Non-Volatile Memory
- Over-Temperature Protection
- IIC Compatible Interface for Register Control
- Available in 6.5mmX4.5mm 46-pin QFN Package

General Description

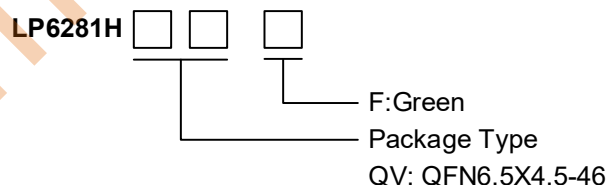
The LP6281H is a programmable multi-functional power solution with integrated gamma buffers, VCOM1 buffer for TFT-LCD. It contains one boost converter/controller (AVDD), one ISO MOSFET controller for AVDD power on sequence, one buck converter (VBK), one boost converter (VGH) with the temperature compensation, one inverting converter (VGL), one negative regulators (VSS), 14-CH gamma buffers, 2-CH VCOM buffer, All channel output level and sequence can be programmable by I2C interface and integrated Multiple-Time Programmable (MTP) non-volatile memory.

With its high current capabilities, the LP6281H is ideal for large screen LCD TV/MNT panel application with widely supply voltage range and also integrated complete protection functions including, OVP, UVP, OCP and OTP. The LP6281H available in a QFN6.5x4.5-46 pin package.

Applications

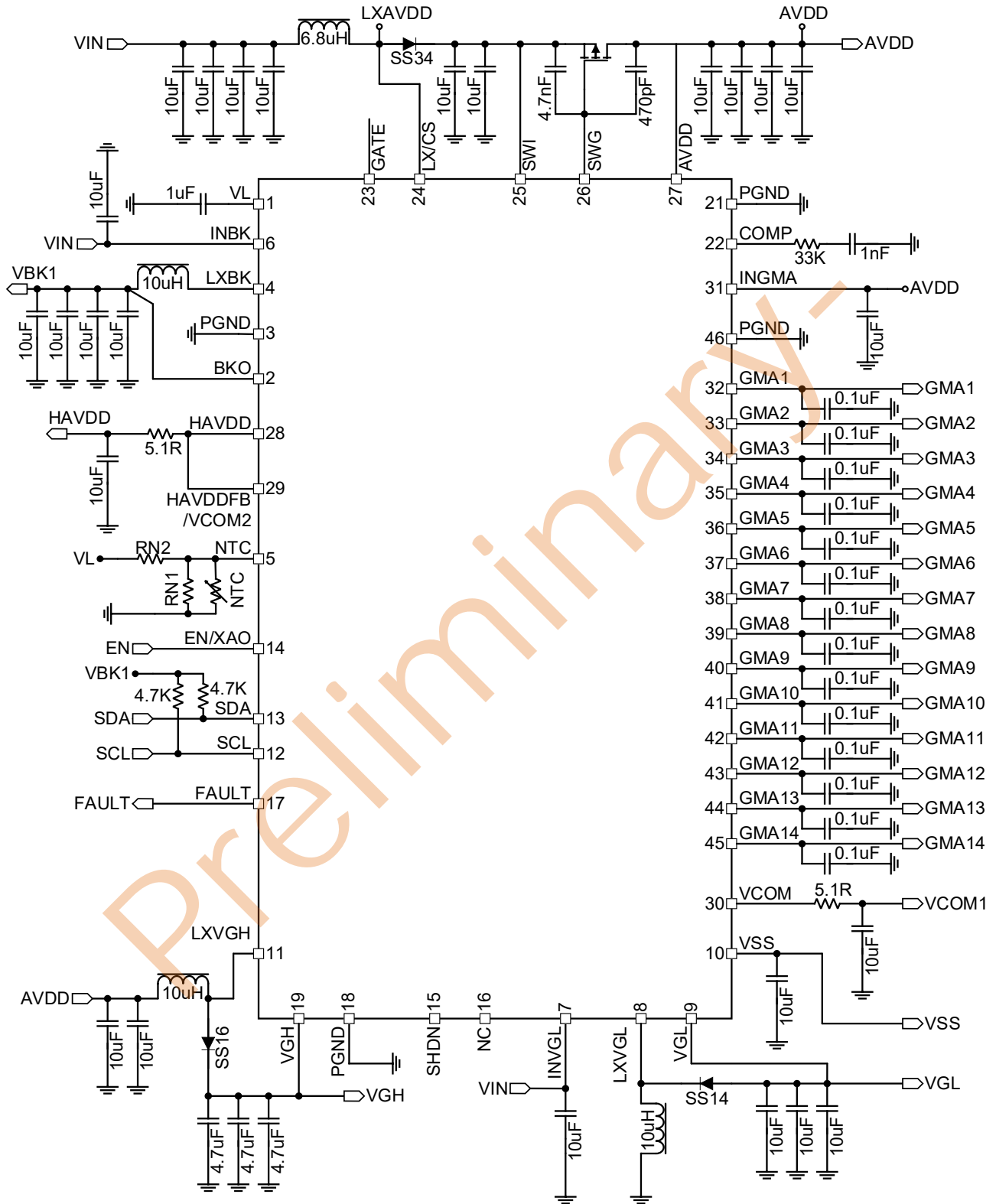
- TFT LCD Monitor Panel
- TFT LCD TV Panel

Order Information





Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6281HQVF	LPS LP6281 HYWX	MSL3	QFN6.5X4.5-46	3K/REEL

Marking indication:

Y: Year code. W: Week code. X: Batch numbers.

Pin Diagram



LP6281HQVF QFN6.5X4.5-46

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Pin Description

Pin#	Name	Description
1	VL	5V internal linear regulator output
2	BKO	Feedback voltage input for VBK buck converter
3	PGND	Power Ground
4	LXBK	Switch node of the VBK Buck converter
5	NTC	Temperature compensation node, Connect NTC thermistor and resistors to this pin to control the slope of VGH voltage for temperature compensation
6	INBK	Supply voltage input of VBK Buck converter
7	INVGL	Supply voltage input of the Inverting converter
8	LXVGL	VGL switch node of the inverting converter
9	VGL	VGL feedback voltage input and VSS Input Supply
10	VSS	Negative supply voltage output
11	NC	Floating this pin, Do not connect to any other pin or circuit
12	SCL	Clock input pin of the IIC serial interface
13	SDA	Data input pin of the IIC serial interface
14	EN/XAO	@31h,bit7=0, Enable pin of the AVDD,VGH,HAVDD,VCOM1,VCOM2 and Gamma. Enable pin must be connect high signal. 400Kohm pull down resistor connect from this pin to ground @31h,bit7=1, XON pin for the shutdown reset function output and open drain voltage detector output.
15	SHDN	Sleep MODE Control, When SHDN is high Level, The chip goes into sleep mode 4.7MΩ pull down resistor connect from this pin to ground
16	NC	Floating this pin, Do not connect to any other pin or circuit
17	FAULT	FAULT signal input/output pin. The FAULT pin is open drain output with internal pull up resistor. The output High/Low depended on protection functions. It also can be connected the open drain circuit to control IC operations. (1) Ouput channel UVP/SCP except VBK channel FAULT_O pin is Low active and all output channel shutdown except VBK (2) VBK UVP/SCP FAULT_O pin is Low active and all output channel shutdown (3) External signal FAULT_I pin is Low active and all output channel shutdown except VBK
18	PGND	Power ground
19	VGH	VGH feedback voltage input
20	LXVGH	VGH switch node of the boost converter

Pin Description(continued)

Pin#	Name	Description
21	PGND	Power ground
22	COMP	Compensation pin for AVDD Boost converter
23	GATE	External N MOSFET gate driver for AVDD external mode
24	LX/CS	LX: Switch node of the AVDD boost converter for AVDD internal mode CS: External current sense for AVDD external mode
25	SWI	Source input of the AVDD Boost converter isolation P MOSFET
26	SWG	Gate driver of the AVDD Boost converter External isolation P MOSFET
27	AVDD	Drain output of the AVDD Boost converter isolation P MOSFET and Feedback voltage input of the AVDD Boost converter
28	HAVDD	Output of the AVDD OPAMP
29	HAFB/VCOM2	HAFB: Negative input of the HAVDD OPAMP VCOM2: VCOM2 output
30	VCOM1	VCOM1 operational amplifier output
31	INGMA	Supply voltage input of Gamma buffer and VCOM OP
32	GMA1	Gamma buffer output 1.
33	GMA2	Gamma buffer output 2.
34	GMA3	Gamma buffer output 3.
35	GMA4	Gamma buffer output 4.
36	GMA5	Gamma buffer output 5.
37	GMA6	Gamma buffer output 6.
38	GMA7	Gamma buffer output 7.
39	GMA8	Gamma buffer output 8.
40	GMA9	Gamma buffer output 9.
41	GMA10	Gamma buffer output 10.
42	GMA11	Gamma buffer output 11.
43	GMA12	Gamma buffer output 12.
44	GMA13	Gamma buffer output 13.
45	GMA14	Gamma buffer output 14.
46	PGND	Power ground
47	EPAD	Exposed pad. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation

Absolute Maximum Ratings (Note1)

INBK,INVGL to PGND	-0.3V to +16.0V
SWI,SWG,AVDD to PGND	-0.3V to +22V
HAVDD, HAFB/VCOM2 to PGND	-0.3V to +22V
LX/CS to GND	-0.3V to +22V
LX/CS to SWI	-0.3V to +22V
SWI to AVDD	-0.3V to +22V
EN to PGND	-0.3V to +6V
VL to PGND	-0.3V to +6V
COMP,NTC,SDA,SCL to PGND	-0.3V to +6V
SHDN,FAULT to PGND	-0.3V to +6V
BKO to PGND	-0.3V to +6V
GATE to PGND	-0.3V to +6V
LXBK to PGND	-0.3V to INBK+0.3V
LXVGH,VGH to PGND	-0.3V to +50V
LXVGL,VGL to PGND	-20V to +0.3V
LXVGL to INVGL	-36V to +0.3V
VSS to PGND	-20V to +0.3V
VGH to VGL,VSS	-0.3V to +60V
VGL to VSS	-20V to +0.3V
INGMA to PGND	-0.3V to +22V
VCOM1 to PGND	-0.3V to INGMA+0.3V
GMA1-14 to PGND	-0.3V to INGMA+0.3V
AGND to PGND	-0.3V to +0.3V

Note1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings (Note2)

HBM (Human Body Model)	2KV
CDM (Charge Discharge Model)	500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ)	150°C
Operating Junction Temperature Range (TJ)	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec)	260°C
θ_{JA} (Junction-to-Ambient Thermal Resistance)	TBD°C/W

Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	Def.	MAX	UNIT
V _{IN}	VIN Supply Range		8.6	12	14.0	V
	VIN Supply Range		4.3	5	6.0	V
V _{AVDD}	AVDD Output Range1	Step:100mV _{REG 0x46[7]=0}	13.5	17.6	19.8	V
	AVDD Output Range2	Step:100mV _{REG 0x46[7]=1}	11	15.1	17.3	V
V _{BK}	VBK Output Range	Step:50mV	1.8	3.3	3.35	V
V _{VGL}	VGL Output Range	Step:250mV	-18	-12	-3.0	V
V _{VSS}	VSS Output Range	Step:250mV	-16	-8	-3.0	V
V _{VGH}	VGH Output Range	Step:1.0V	20	30	42	V
V _{HAVDD}	HAVDD Output Range	Resolution:AVDD/512	192*Res4		319*Res4	V
V _{VCOM1}	VCOM1 Output Range	Resolution: (Vcom.max-vcom.min)/127	V _{VCOM.MIN}		Res1*127+ V _{VCOM.MIN}	V
V _{VCOM2}	VCOM2 Output Range	Resolution: (Vcom.max-vcom.min)/127	V _{VCOM.MIN}		Res1*127+ V _{VCOM.MIN}	V
GMA1-14	GMA1-14 AVDD Range	AVDD/1024	0		V _{AVDD} /1024 *1023	V
V _{GHVTC2}	VGH&VGL VTC2	Step:0.2V	0.4	3.0	3.4	V
V _{GHVTC1}	VGH&VGL VTC1	Step:0.2V	0.4	2.0	3.4	V
V _{XAO}	XAO Discharge Threshold	Step:0.25V@0x46h[7]=0	6.5	7.00	10.25	V
	XAO Discharge Threshold	Step:0.14V@0x46h[7]=1	3.62	3.90	5.58	V

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A = 25^\circ C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{IN}	Input Voltage Range	Reg [46h] bit7=0	8.6		14.0	V
	Input Voltage Range	Reg [46h] bit7=1	4.3		6.0	V
I_{Q_TOTAL}	Quiescent Current of all module	$V_{IN}=12V$, Typical App. All Module turn on		30	40	mA
I_{SLEEP}	Sleep on Quiescent Current into V_{IN}	VL Shutdown		5	10	μA
V_{INUVLO_R}	V_{IN} under-voltage rising lockout Threshold Reg address=[46h] bit7=0	V_{IN} rising	8.1	8.3	8.5	V
V_{INUVLO_HYS}	V_{IN} under-voltage hysteresis lockout Threshold Reg address=[46h] bit7=0	Hysteresis	700	800	900	mV
V_{INUVLO_R}	V_{IN} under-voltage rising lockout Threshold Reg address=[46h] bit7=1	V_{IN} rising	4.1	4.2	4.3	V
V_{INUVLO_HYS}	V_{IN} under-voltage hysteresis lockout Threshold Reg address=[46h] bit7=1	Hysteresis	300	400	500	mV
V_L	VL Output Voltage at TV MODE	$V_{IN}=8.6V$ to $14.0V$	4.95	5.00	5.05	V
V_L	VL Output Voltage at MNT MODE	$V_{IN}=4.8V$ to $5.5V$	4.55	4.60	4.65	V
FOSC1	$V_{BK}, AVDD, VGH, VGL$ Frequency1	REG 0x29h[7] = 0	600	750	900	KHz
FOSC2	$V_{BK}, AVDD, VGH, VGL$ Frequency2	REG 0x29h[7] = 1	400	500	600	KHz
FOSC3	$V_{BK}, AVDD, VGH, VGL$ Frequency3	REG 0x29h[6] = 1	1000	1250	1500	KHz
T_{SD}	Thermal Shutdown Protection	Rising	140	150	160	$^\circ C$
LOGIC						
V_{IH}	SDA/SCL/EN Input High Level		1.6			V
V_{IL}	SDA/SCL/EN Input Low Level				0.6	V
I_{IH}, I_{IL}	SDA/SCL Input Leakage Current	$V_I=0V$ or $3.3V$	-1	0.01	+1	μA
R_{PD}	EN pull down resistor	Only EN Function	320	400	480	K Ω
	Input Capacitance			5		pF
V_{OL}	SDA Output Low Voltage	$I_{SINK}=6mA$	0.5			V

Electrical Characteristics

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 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ASYN. BOOST CONVERTER(AVDD)						
V_{AVDD1}	AVDD output voltage range1	Reg[46h] bit7=0	13.5		19.8	V
V_{AVDD2}	AVDD output voltage range2	Reg[46h] bit7=1	11		17.3	V
	AVDD Output Accuracy	No load, Default output	-1		+1	%
$R_{DS(ON)}$	N-MOSFET ON Resistance	$I_{LX/CS}=500mA$		90	130	m Ω
$R_{DS(ON)}$	P-MOSFET ON Resistance	$I_O=100mA$		500	700	m Ω
R_{CS}	Current-sense Transresistance			0.25		Ω
I_{LIM}	N-MOSFET switch current limit		5	6	7	A
SS_{AVDD}	Soft-start Period	Programmable softstart		10		ms
I_{LEAK}	Switch Leakage Current	$V_{LX/CS}=24V$		1	10	μA
V_{OVP}	SWI Over Voltage Protection	V_{SWI} Rising Hysteresis=1V	20.8	21.8	22.8	V
	AVDD Line Regulation	$V_{IN}=8.6V$ to $14.0V$ $I_{AVDD}=1mA$		0.04		%/V
	AVDD Load Regulation	$I_{AVDD}= 1mA$ to $1.5A$	-1		+1	%/A
	AVDD UVP Fault Trip Level	V_{AVDD} Falling	80	85	90	%
	AVDD UVP fault timer duration			50		ms
V_{SC}	SWO Short Circuit Level	V_{AVDD} Falling	15	20	25	%
	Maximum Duty Cycle		85	90		%
R_{SWO_DCGH}	Power off discharge resistance	REG. 0x2Ch[5]=0		1.4		K Ω
R_{SWO_DCGH}	Power off discharge resistance	REG. 0x2Ch[5]=1		4.7		K Ω
V_{PRE_AVDD}	AVDD Precharge detect voltage	REG. 0x2D[2]=0	0.55	0.60	0.65	V
V_{PRE_AVDD}	AVDD Precharge detect voltage	REG. 0x2D[2]=1	1.10	1.20	1.30	V

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A=25^{\circ}C$)
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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOLATION SWITCH						
	SWI supply voltage range		8		20	V
$R_{DS(ON)}$	Isolation PMOS switch on resistance	$V_{SWI}=16.8V, I_{SW}=0.5A$		150	250	m Ω
	Switch current		2	2.5	3	A
V_{GOH}	Gate Output Hi-level			SWI		V
V_{GOL}	Gate Oput Low-level			SWI-6		V
R_{AVDD}	Gate pull-high resistor			10	12	K Ω
I_{G_SINK}	Gate Sink Current			10	12	μA
External N-MOSFET Gate Drvier(Gate of AVDD)						
V_{GATE_OH}	Gate High Voltage		4.5	5	5.5	V
V_{GATE_OL}	Gate Low Voltage		0		0.3	V
V_{CS_OCP}	External NMOS Switch Current Limit	$R_{CS}=50m\Omega$	0.25	0.3	0.35	V
R_{DSON_GH}	Gate to VL High-Side On Resistance			5	20	Ω
R_{DSON_GL}	Gate to GND Low-side On Resistance			5	20	Ω
FAULT SIGNAL(FAULT)						
R_{FAULT}	FAULT Pull Up Resistance	up to VL	80	100	120	K Ω
V_{FAULT_HIV}	FAULT High Level Input Voltage		2			V
V_{FAULT_LIV}	FAULT Low Level Input Voltage				1	V
	FAULT Pull Low Voltage	$I_{IN}=3mA$			0.5	V

Electrical Characteristics

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ASYNCR BOOST CONVERTER(VGH)						
V_{GH_NT}	Adjustable Normal Temperature Output Voltage Range	Reg[03h],5bits/26 steps	20		42	V
V_{GH_LT}	Adjustable Low Temperature Output Voltage Range	Reg[04h],5bits/26 steps	20		42	V
V_{GHRES}	VGH Output voltage resolution			1		V
V_{GHACC}	VGH Output voltage accuracy		-2		+2	%
$R_{DS(ON)}$	Low-side NMOS Switch on resistance			0.45	0.55	Ω
I_{LIMIT}	NMOS Switch Current Limit	REG 0x03h[7]=0	1.5	2	2.5	A
I_{LEAK}	NMOS Switch Leakage Current	$V_{LXVGH}=45V$		1	10	μA
	Line Regulation	$V_{AVDD}=13.5V$ to $19.8V$ $V_{GH}=28V$, $I_{GH}=0.1A$		0.1		%/V
	Load Regulation	$V_{AVDD}=16.8V$, $V_{GH}=28V$ $I_{GH}=1mA$ to $0.1A$		0.3		%/A
T_{SS}	Soft-start Time	Programmable softstart		3		ms
	Output OVP Fault-Trip Level	V_{GH} rising, Hysteresis:2V	43	44	45	V
	Output UVP Fault-Trip Level	V_{GH} falling	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	V_{GH} falling	15	20	25	%
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[4]=0		1.5		K Ω
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[4]=1		30		K Ω

Electrical Characteristics

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGL INVERTING CONVERTER(VGL)						
V_{VGL}	VGL Output Voltage Range	Reg[05h], 5bits/31 steps	-18		-3	V
V_{VGL_OFFSET}	VGL Output Offset	Reg[05h], bit7=1		-0.25		V
	Output Voltage Tolerance	No load, Default output	-2		+2	%
	Maximum Duty Cycle		80	90		%
$R_{DS(ON)}$	PMOS Switch On-Resistance	$I_{VGL_SW}=100mA$		0.50	0.60	Ω
	Minimum On Time		90	100	110	ns
I_{LIMIT}	PMOS Switch Current Limit	REG 0x05h[6]=0	1.5	2.0	2.5	A
I_{LEAK}	PMOS Switch Leakage Current	$V_{VGL_SW}=V_{IN}$ or VGL		5		μA
	Line Regulation	$V_{IN}=8.6V$ to $14.0V$ $V_{VGL}=-7V$, $I_{GL}=0.1A$		0.1		%/V
	Load Regulation	$V_{IN}=12V$, $V_{VGL}=-8V$ $I_{GL}=1mA$ to $200mA$		0.3		%/A
T_{SS}	Soft-start time			3		ms
	VGL Output OVP Fault-Trip Level	V_{GL} falling, hysteresis:110%	115	120	125	%
	VGL Output UVP Fault-Trip Level	V_{GL} rising	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	V_{GL} rising	15	20	25	%
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[3]=1		10		K Ω

Electrical Characteristics

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSS NEGATIVE REGULATOR(VSS)						
VSS	Adjustable Output Voltage Range	Reg[07h], 5bits/27 steps	-16		-3	V
VSS _{OFFSET}	VSS Output Offset	Reg[07h], bit6=1		-0.25		V
	Output Voltage Tolerance	No load, Default output	-2		+2	%
I _{LIMIT}	Current Limit		50	100		mA
	Output UVP Fault-Trip Level	V _{SS} falling	75	80	85	%
	UVP fault timer duration			50		ms
INL	Integral Nonlinearity	No load	-1		+1	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
	Load Regulation	I _{VSS} =0mA to 50mA		0.5		mV/ mA
R _{DCGH}	Power off Discharge Resistance			1.2		KΩ
R _{SOURCE}	VSS to GND Source Resistance	105%*VSS trigger	500	600		Ω
THERMAL COMPENSATION(VGH)						
VTC1	VGH lower bound voltage of VTC1	Reg[2Eh], 4bits/16 steps	0.4		3.4	V
VTC2	VGH upper bound voltage of VTC2	Reg[2Eh], 4bits/16 steps	0.4		3.4	V

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A=25^\circ C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HAVDD OPAMP(HAVDD)						
	HAVDD voltage resolution			7		bits
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
V_{OH}	Output voltage swing high	$I_{HAVDD}=+100mA$		$V_{VAA}-2$		V
V_{OL}	Output voltage swing low	$I_{HAVDD}=-100mA$		2	2.5	V
I_{OUT}	Output Continuous Current		± 200			mA
I_{SC}	Short Circuit Current		± 200			mA
CMRR	Input common-mode rejection ratio	$AVDD=16.8V, f=10KHz$ 2V amplifude sin signal		80		dB
PSRR	Power supply rejection ratio	AVDD sweeps from 13.5V to 19.8V		60		dB
SR	Slew rate			45		V/us
BW	-3dB bandwidth			20		MHz
	Output OVP Fault-Trip Level	V_{HAVDD} rising	115	120	125	%
	Output UVP Fault-Trip Level	V_{HAVDD} falling	75	80	85	%
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[2]=1		10		K Ω

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A = 25^\circ C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNC BUCK CONVERTER(VBK)						
VBK	VBK Output Voltage Range	Reg[01h], 5bits/32 steps	1.8		3.35	V
	Output Voltage Tolerance	No load, Default output	-2		+2	%
	Maximum Duty Cycle		85	90		%
$R_{DS(ON)_HS}$	High-side PMOS switch on resistance	$I_{LXBK}=500mA$		400	500	m Ω
$R_{DS(ON)_LS}$	Low-side NMOS switch on resistance	SYNC. MODE $I_{LXBK}=-500mA$		200	300	m Ω
$R_{DS(ON)_LS}$	Low-side NMOS switch on resistance	ASYNC. MODE $I_{LXBK}=-100mA$		7	10	Ω
I_{LIMIT}	High-side PMOS switch current limit		2.0	2.5	3.0	A
I_{PEAK_HS}	High-side switch leakage current	$V_{LXBK}=0V$		1	10	μA
I_{PEAK_LS}	Low-side switch leakage current	$V_{LXBK_SW}=12V$		1	10	μA
	Line Regulation	$V_{IN}=8.6V$ to $14.0V$ $I_{VBK}=500mA$		0.05		%/V
	Load Regulation	$I_{VBK}=1mA$ to $2.0A$	-1		+1	%
T_{SS}	Soft-start Time			3		ms
	Output OVP Fault-Trip Level	V_{VBK} rising	115	120	125	%
	Output UVP Fault-Trip Level	V_{VBK} falling	75	80	85	%
	UVP fault timer duration	V_{VBK} falling		50		ms
	Output SCP Fault-Trip Level		15	20	25	%
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[6]=0		0.5		K Ω
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[6]=1		1		K Ω

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A=25^\circ C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAMMA BUFFERS(GMA1 TO GMA14)						
V_{SWO_GMA}	Supply Range		11		19.8	V
	Gamma Voltage Resolution	GMA1 to 14, 10bits/1024 steps		$V_{AVDD}/1024$		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
$V_{GMA1-14}$	Output Voltage Range	$I_{GMA1\ to\ 14}$ =sinking or source 5mA	GND +0.2		V_{AVDD} -0.2	V
I_{OUT}	Output Current	$V_{GMA1\ to\ 14}$ drop 0.5V	± 50			mA
I_{SC}	Short Circuit Current	$V_{GMA1\ to\ 14}$ to V_{SWO_GMA} or $V_{GMA1\ to\ 14}$ to GND	± 50			mA
T_{D_GMA}	Program to Output Delay	From ACK falling edge to programming gamma change 50% voltage at output		15		us
	Load Regulation	$I_{GMA1\ to\ 14} = -12mA\ to\ 12mA$		$\pm 0.5 + R_d$		mV/ mA

Preliminary

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A = 25^\circ C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCOM1 BUFFER						
V_{SWO_GMA}	Supply Range		11		19.8	V
V_{VCOM1}	Adjustable Output Voltage Range	Reg[08h], 7bits/128 steps Res1=(vcom.max-vcom.min)/127	0*res 1+ vcom .min		127*res 1+ vcom .min	V
V_{VCOM_MAX}	Adjustable VCOM_MAX	Reg[0Ah], 7bits/128 steps	1* V_{AVDD} /128		128* V_{AVDD} /127	V
$V_{VCOMMIN}$	Adjustable VCOM_MIN	Reg[0Bh], 7bits/128 steps	0* V_{AVDD} /128		127* V_{AVDD} /127	V
	VCOM1 voltage resolution	VCOM1 will be clamped between vcom.max and vcom.min		$V_{AVDD}/128$		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
V_{VCOM1}	Output Voltage Range	VCOM1&VCOM2 will be clamped between vcom.max and vcom.min	GND +0.5		V_{AVDD} -0.5	V
T_{D_VCOM1}	Program to Output Delay	From ACK falling edge to programming VCOM change 50% voltage at output		15		us
I_{OUT}	VCOM1 Output Continuous Current		± 150			mA
I_{sc}	VCOM1 Short Circuit Current		± 150			mA
	Load Regulation	$I_{VCOM1} = -100mA$ to $100mA$	-1		+1	mV/ mA
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[1:0]=01		20		Ω
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[1:0]=10		1.0		K Ω
R_{DCGH}	Power off Discharge Resistance	REG 0x2Ch[1:0]=11		8.0		K Ω

Electrical Characteristics

($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A=25^{\circ}C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^{\circ}C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCOM2 BUFFER						
V_{SWO_GMA}	Supply Range		11		19.8	V
V_{VCOM2}	Adjustable Output Voltage Range	Reg[45h], 7bits/128 steps Res1=(vcom.max-vcom.min)/127	0*res 1+ vcom .min		127*res 1+ vcom .min	V
V_{VCOM_MAX}	Adjustable VCOM_MAX	Reg[0Ah], 7bits/128 steps	1* V_{AVDD} /128		128* V_{AVDD} /127	V
$V_{VCOMMIN}$	Adjustable VCOM_MIN	Reg[0Bh], 7bits/128 steps	0* V_{AVDD} /128		127* V_{AVDD} /127	V
	VCOM2 voltage resolution	VCOM2 will be clamped between vcom.max and vcom.min		$V_{AVDD}/128$		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
V_{VCOM2}	Output Voltage Range	VCOM2 will be clamped between vcom.max and vcom.min	GND +0.5		V_{AVDD} -0.5	V
T_{D_VCOM2}	Program to Output Delay	From ACK falling edge to programming VCOM change 50% voltage at output		15		us
I_{OUT}	VCOM2 Output Continuous Current		± 20			mA
I_{sc}	VCOM2 Short Circuit Current		± 20			mA
	Load Regulation	$I_{VCOM1}=-20mA$ to $20mA$	-2		+2	mV/ mA

Electrical Characteristics

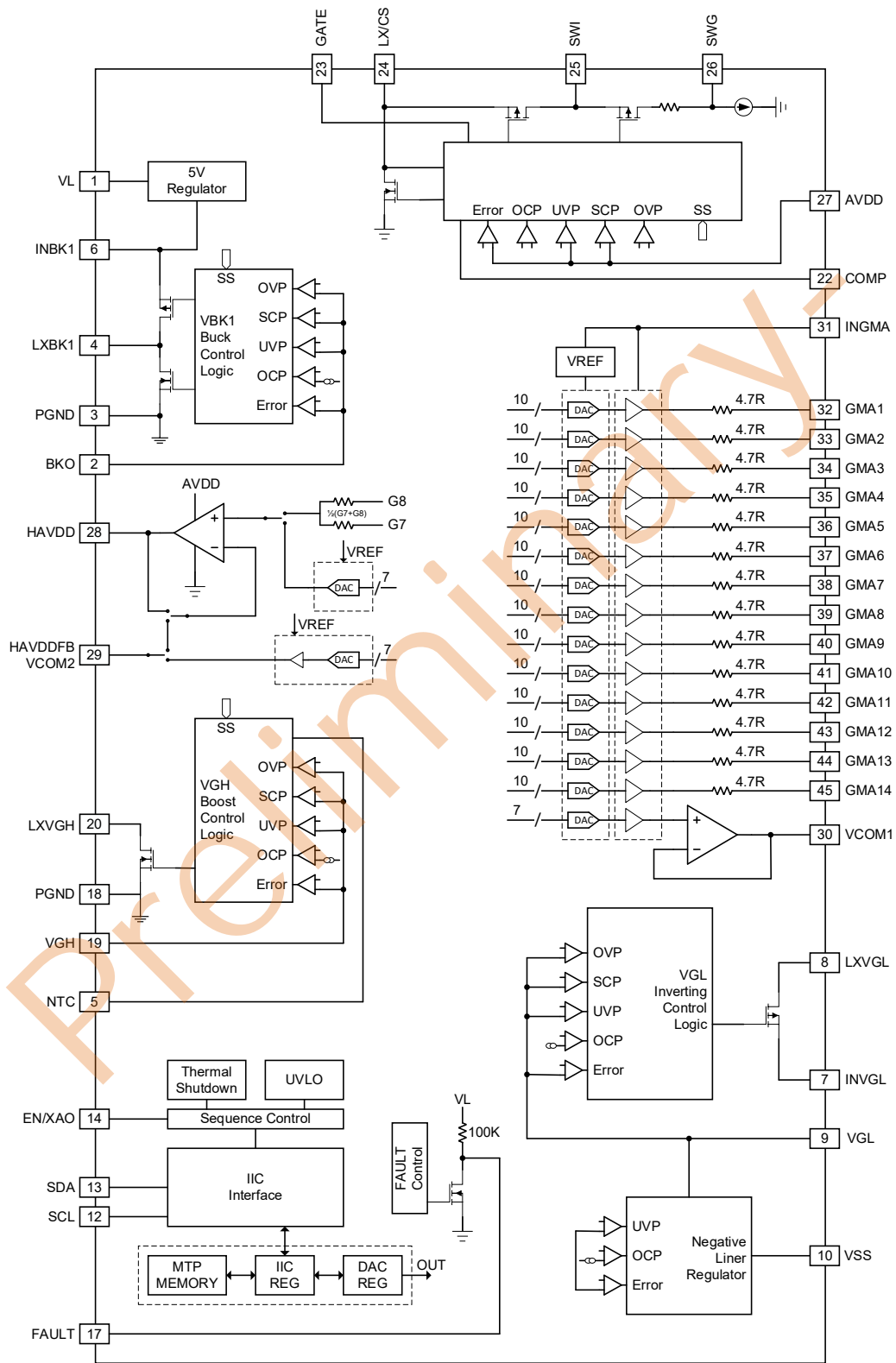
($V_{IN} = 12V$, $V_{AVDD} = 16V$, $V_{BK} = 3.3V$, $V_{HAVDD} = 8V$, $V_{VGH} = 28V$, $V_{VGL} = -10V$, $V_{VSS} = -6V$ with typical values $T_A=25^\circ C$)
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IIC INTERFACE(SDA,SCL)						
V_{IH}	High Level Input Voltage		1.6	---	---	V
V_{IL}	Low Level Input Voltage		---	---	0.5	V
IIC TIMING CHARCTERISTICS						
f_{SCL}	Serial-Clock Frequency		10	---	400	KHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		1300	---	---	nS
$t_{HD,STA}$	Hold Time(Repeated) START Condition		600	---	---	nS
t_{LOW}	SCL Pulse-Width Low		1300	---	---	nS
t_{HIGH}	SCL Pulse-Width High		600	---	---	nS
$t_{SU,STA}$	Setup Time for a Repeated START Condition		600	---	---	nS
$t_{HD,DAT}$	Data Hold Time		50	---	800	nS
$t_{SU,DAT}$	Data Setup Time		100	---	---	nS
t_R	SDA and SCL Receiving Rise Time	CB is IN pF	20+ 0.1CB	---	300	nS
t_F	SDA and SCL Receiving Fall Time	CB is IN pF	20+ 0.1CB	---	300	nS
C_{IN}	SDA and SCL Input Capacitance			---	400	pF
$t_{SU,STO}$	Setup Time for STOP Condition		600	---	---	nS
t_{AA}	Clock Low to Data Out Valid		100	---	900	nS
	Program MTP Blanking Time		500			ms
	Read MTP Blanking Time		10			ms
	IIC Time out			100		ms

I2C Serial-Interface

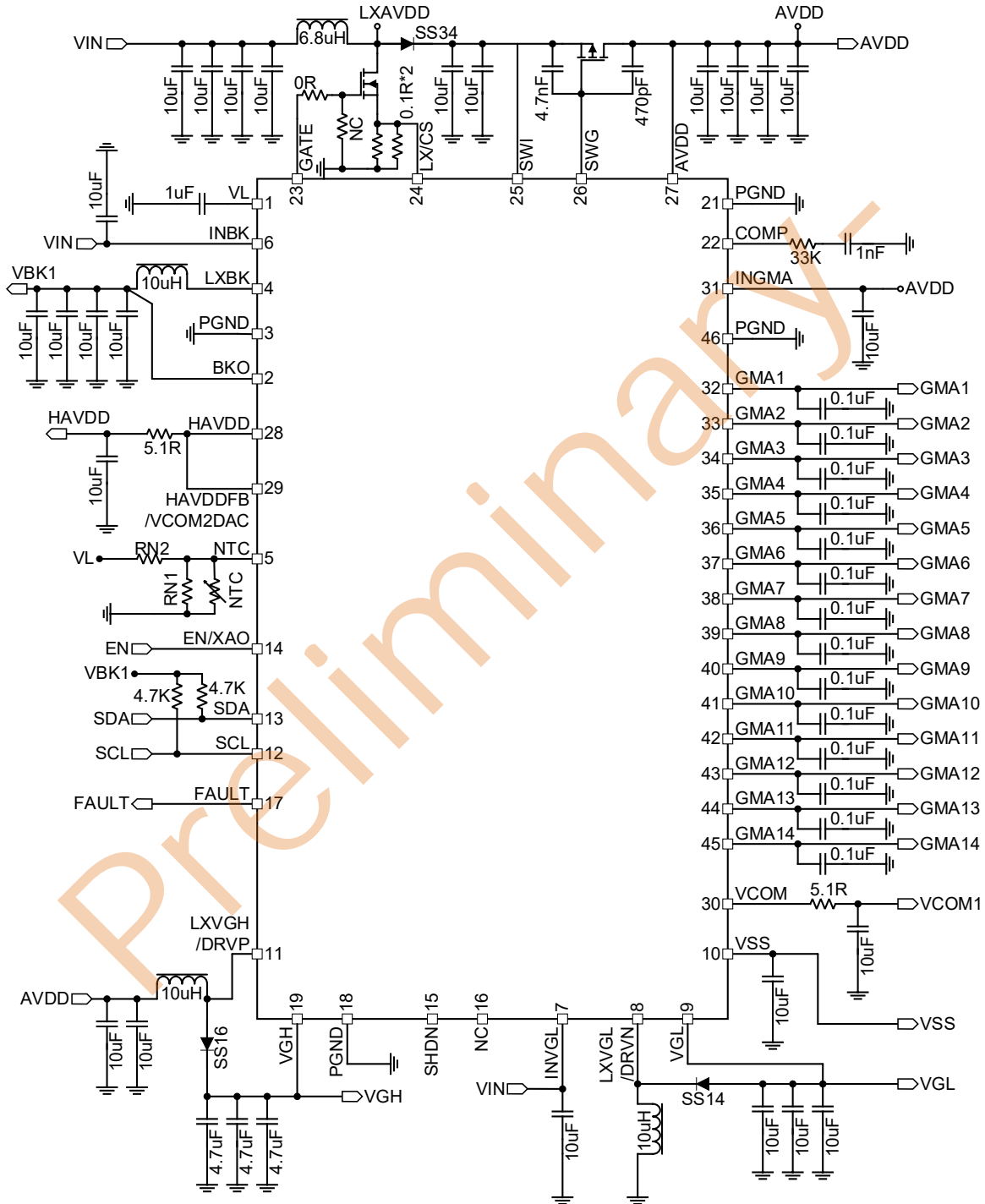
The LP6281H communicates through an industry standard 2-wire I2C serial-interface to receive data in slave mode. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. A master device, usually a microcontroller or a digital signal processor, controls the bus.

Functional Block Diagram



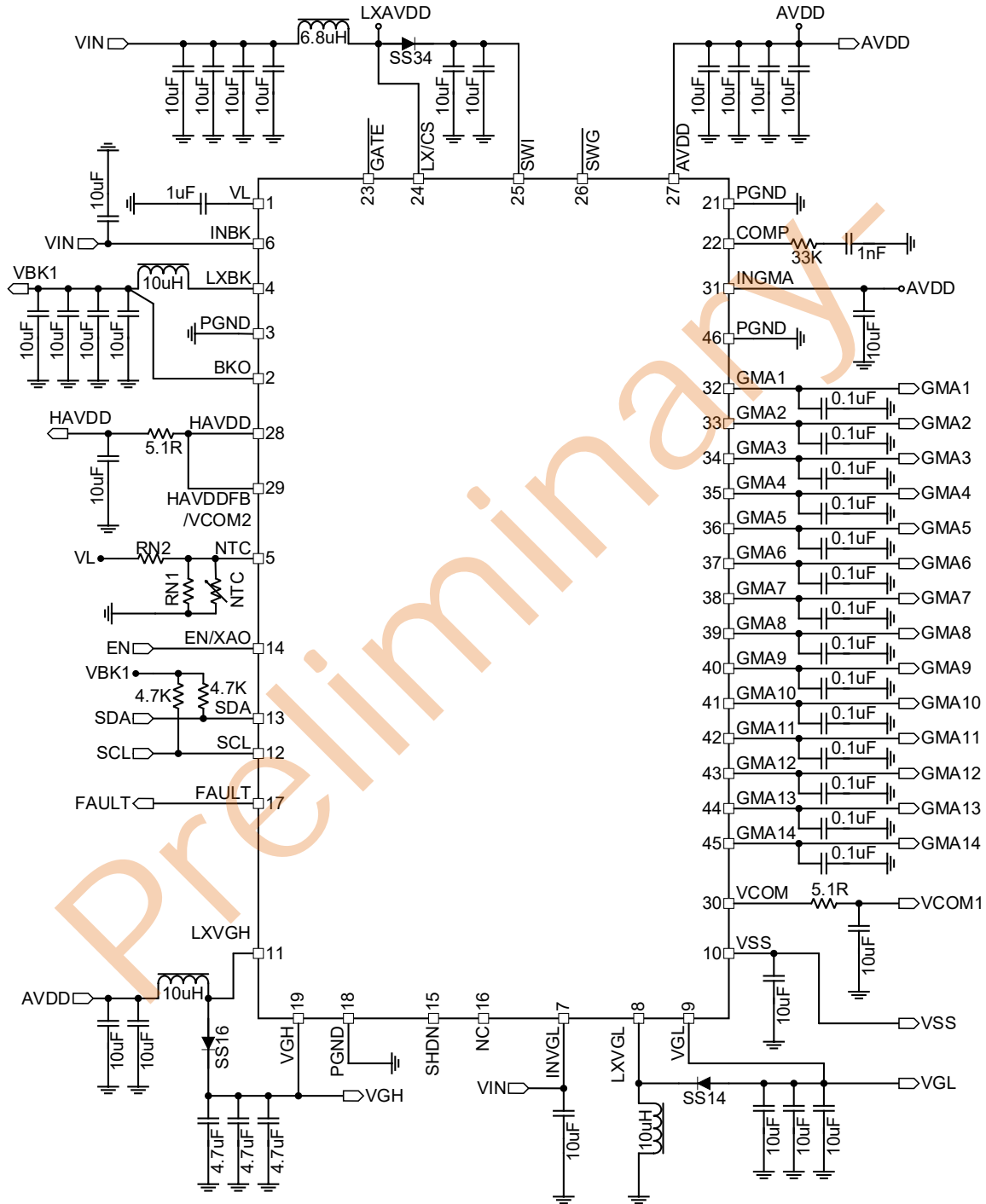
Typical Application Circuit_1

Channel	Type Selection
AVDD Converter	Boost Controller
AVDD Isolation Switch	External ISO-PMOS Switch

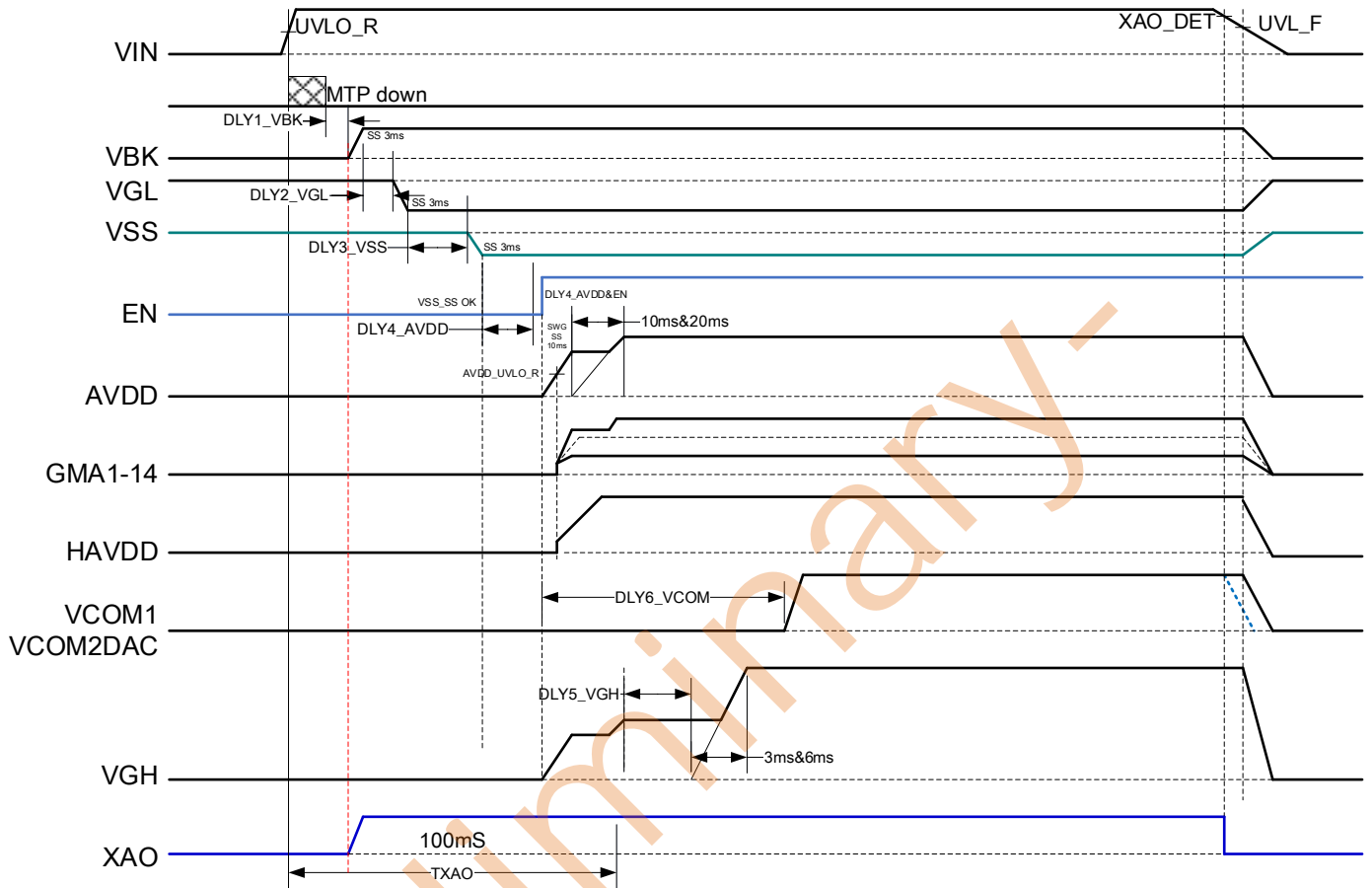


Typical Application Circuit_2

Channel	Type Selection
AVDD Converter	Boost Converter Internal power MOS
AVDD Isolation Switch	Internal ISO-PMOS Switch



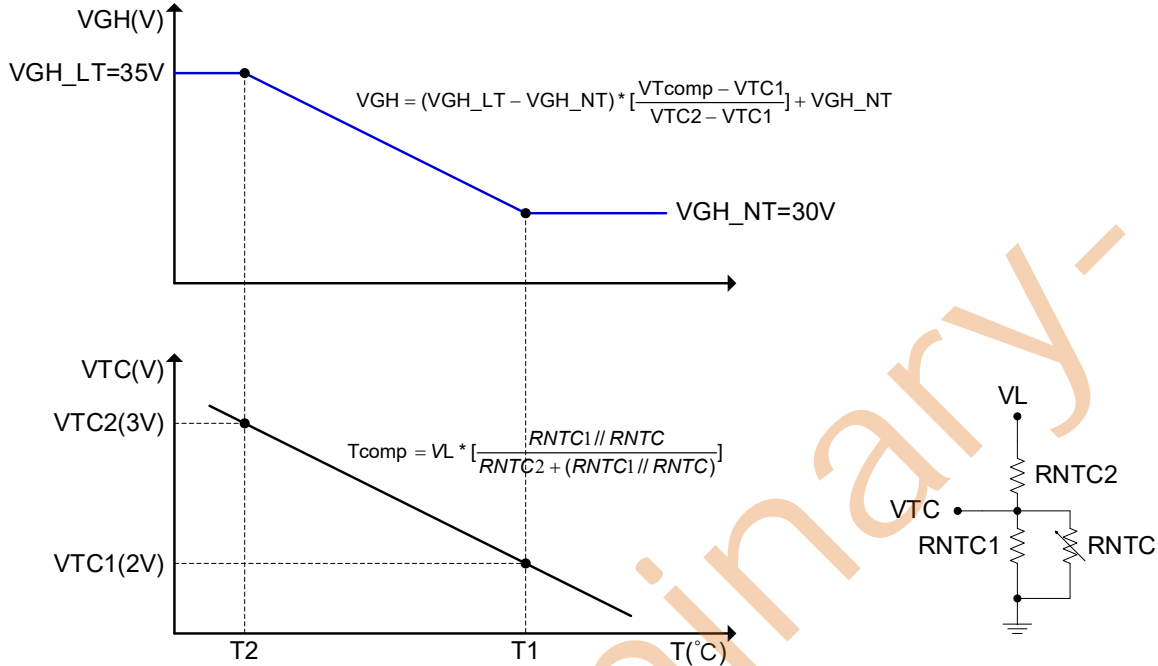
Timing Diagram



Temperature Compensation Function

VGH channel can be temperature compensated, allowing its output voltage to transition which monitor NTC voltage connected a NTC(Negative Temperature Coefficient) Resistor to GND (see Figures 1). VTC1 and VTC2 defines the high/low boundary Voltage as VNTC variation.

VGH temperature compensation curve



Device Address Setting

PMIC Device Slave Address (0x40h)

MSB							LSB
	0	1	0	0	0	0	R/W

Read Address	Write Address
01000001(41h)	01000000(40h)

Only for VCOM1 Device Slave Address (0xE8h)

MSB							LSB
	1	1	1	0	1	0	R/W

Read Address	Write Address
11101001(E9h)	11101000(E8h)

PMIC IIC Command Device address (40h/41h)

1. Write single byte of data to DAC register Example: Write 29h to DAC Address 07h

Start	01000000 Device address	Slave ACK	00000111 Register address	Slave ACK	00101001 Data	Slave ACK	Stop
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2. Write multiple byte of data to DAC register Example: Write 29h,2Ah,2Bh to DAC Address 06h,07h,08h

Start	01000000 Device	Slave ACK	00000110 Register	Slave ACK	00101001 Data1	Slave ACK	00101010 Data2	Slave ACK	00101011 Data3	Slave ACK	Stop
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3. Write All DAC Register into EEPROM

Start	01000000 Device address	Slave ACK	11111111 Register address	Slave ACK	10000000 Control	Slave ACK	Stop
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4. Write VCOM1 Data Register into EEPROM

Start	01000000 Device address	Slave ACK	11111111 Register address	Slave ACK	01000000 Control	Slave ACK	Stop
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5. Read single byte of data from DAC register

Start	01000000 Device address	Slave ACK	11111111 Register address	Slave ACK	00000000 Control	Slave ACK	Stop
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Start	01000000 Device	Slave ACK	00000110 Register	Slave ACK	01000001 Read	Slave ACK	D0-D7 Data1	Master ACK	Stop
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6. Read data from DAC register Example: Reading Data from DAC Register Address 08h,09h

Start	01000000 Device address	Slave ACK	11111111 Register address	Slave ACK	00000000 Control	Slave ACK	Stop
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Start	01000000 Device	Slave ACK	00001000 Register	Slave ACK	01000001 Read	Slave ACK	D0-D7 Data1	Master ACK	D0-D7 Data2	Master ACK	Stop
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7. Read single byte of data from MTP

Start	01000000 Device address	Slave ACK	11111111 Register address	Slave ACK	00000001 Control	Slave ACK	Stop
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Start	01000000 Device	Slave ACK	00000110 Register	Slave ACK	01000001 Read	Master ACK	D0-D7 Data1	Master ACK	Stop
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8. Read data from MTP Example: Reading Data from MTP Address 03h, 04h, 05h,06h

Start	01000000 Device address	Slave ACK	11111111 Register address	Slave ACK	00000001 Control	Slave ACK	Stop
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Start	01000000 Device	Slave ACK	00001000 Register	Slave ACK	01000001 Read	Slave ACK	D0-D7 Data1	Master ACK	D0-D7 Data2	Master ACK	Stop
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Only VCOM1 IIC Command Device address (E8h/E9h)

1. Load VCOM1 MTP data to DAC register(RESET)

Start	11101000 Device address	Slave ACK	00000000 Register address	Slave ACK	01000000 Control	Slave ACK	Stop
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2. Write VCOM1 DAC register into MTP (VCOM1_WR_MTP)

Start	11101000 Device address	Slave ACK	00000000 Register address	Slave ACK	00001000 Control	Slave ACK	Stop
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3. Set VCOM1 output enable=1(OUT_EN)

Start	11101000 Device address	Slave ACK	00000000 Register address	Slave ACK	00000010 Control	Slave ACK	Stop
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4. Write VCOM1 data to DAC register

Start	11101000 Device address	Slave ACK	00000001 Register address	Slave ACK	D0-D7 Data	Slave ACK	Stop
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5. Read single control byte or VCOM1 byte of data from DAC register

Start	11101000 Device	Slave ACK	00000000 Register	Slave ACK	11101001 Read	Master ACK	D0-D7 Data1	Master ACK	Stop
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PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1 Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x00h	[5:0] AVDD output voltage	AVDD	@[46h] bit7=0 13.5V(00h) to 19.8V(3Fh) @[46h] bit7=1 11V(00h) to 17.3V(3Fh)	0.1V	17.6V(29h)
0x01h	[7] VBK operating mode select	VBK_MODE	0: Synchronous 1: Asynchronous		0: SYNC.
	[4:0] VBK output voltage	VBK	1.8V(00h) to 3.35V(1Fh)	0.05V	3.3V(1Eh)
0x02h	[6:0] HAVDD output voltage	HAVDD	Res2*(192)(00h) to Res2*(319)(7Fh) Res2=AVDD/512	AVDD/512	Res2*256(40h)
0x03h	[4:0] VGH normal temperature voltage	VGH_NT	20V(00h) to 42V(16h)	1V	30V(0Ah)
0x04h	[7] VGH low temperature enable	VGH_LT_EN	0: Disable 1: Enable		0: Disable
	[4:0] VGH low temperature voltage	VGH_LT	20V(00h) to 42V(16h)	1V	35V(0Fh)
0x05h	[7] VGL Voltage offset	VGL_OFF_SET	0: Disable 1: -0.25V		0: Disable
	[4:0] VGL voltage	VGL	-3V(00h) to -18V(1Eh)	0.5V	-8V(0Ah)
0x06h	[7:0] Reserved				
0x07h	[7] Reserved				
	[6] VSS output voltage offset	VSS_OFF_SET	0: Disable 1: -0.25V		0: Disable
	[4:0] VSS output voltage	VSS	-3V(00h) to -16V(1Ah)	0.5V	-6V(06h)
0x08h	[7:1] VCOM1 voltage	VCOM1	VCOM.MIN to VCOM.MAX Res1=(vcom.max-vcom.min)/127	Res1	63*Res1+vcom.min (7Eh)
0x09h	[7:0] Reserved				
0x0Ah	[6:0] VCOM1&VCOM2 High limit voltage	VCOM_MAX	1*Res3(00h) to 128*Res3(7Fh) Res3=VAVDD/128	Res3	64*Res3 (3Fh)

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1 Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x0Bh	[6:0] VCOM1&VCOM2 Low limit voltage	VCOM_MIN	0*Res3(00h) to 127*Res3(7Fh) Res3=VAVDD/128	Res3	38*Res3 (26h)
0x0Ch 0x0Dh	[9:0] Gamma1 output voltage	GAMMA1	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x0Eh 0x0Fh	[9:0] Gamma2 output voltage	GAMMA2	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x10h 0x11h	[9:0] Gamma3 output voltage	GAMMA3	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x12h 0x13h	[9:0] Gamma4 output voltage	GAMMA4	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x14h 0x15h	[9:0] Gamma5 output voltage	GAMMA5	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x16h 0x17h	[9:0] Gamma6 output voltage	GAMMA6	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x18h 0x19h	[9:0] Gamma7 output voltage	GAMMA7	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x1Ah 0x1Bh	[9:0] Gamma8 output voltage	GAMMA8	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x1Ch 0x1Dh	[9:0] Gamma9 output voltage	GAMMA9	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x1Eh 0x1Fh	[9:0] Gamma10 output voltage	GAMMA10	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x20h 0x21h	[9:0] Gamma11 output voltage	GAMMA11	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x22h 0x23h	[9:0] Gamma12 output voltage	GAMMA12	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x24h 0x25h	[9:0] Gamma13 output voltage	GAMMA13	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x26h 0x27h	[9:0] Gamma14 output voltage	GAMMA14	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)

PMIC Register Map:

PMIC Device Address: 0x40h Only VCOM1 Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x28h	[7] Group B Enable (Group B: AVDD, HAVDD, VGH, VGL, VSS, PGMA, VCOM1, VCOM2)	Group_B_EN	0: Disable 1: Enable		0: Disable
	[6] VGL enable	VGL_EN	0: Disable 1: Enable		1: Enable
	[5] VSS enable	VSS_EN	0: Disable 1: Enable		1: Enable
	[4] AVDD enable	AVDD_EN	0: Disable 1: Enable		1: Enable
	[3] HAVDD enable	HAVDD_EN	0: Disable 1: Enable		1: Enable
	[2] Gamma enable	GMA_EN	0: Disable 1: Enable		1: Enable
	[1] VCOM1 enable	VCOM1_EN	0: Disable 1: Enable		1: Enable
	[0] VGH enable	VGH_EN	0: Disable 1: Enable		1: Enable
0x29h	[7] Frequency select (VBK,AVDD,VGH,VGL)	FREQ_SEL	0: 750KHz 1: 500KHz		0: 750KHz
	[6] Frequency select (VBK1, AVDD, VGH, VGL)	FREQ_SEL2	0: Follow 0x29h[7] set 1: 1250KHz		0: 0x29h[7]
	[5] Isolation PMOS Internal or External select	ISO_PMOS_INT/EXT	0: External 1: Internal		0: External
	[4] AVDD NMOS_ Internal or External select	AVDD_MOS_INT/EXT	0: Internal 1: External		0: Internal
	[3] Reserved				
	[2] Reserved				
	[1] Reserved				
	[0] Gamma channel type	GMA_CH_TYPE	0: 14_CH(1 to 14_CH) 1: 4_CH(1,7,8,14_CH) Other channel Hiz		0: 14_CH
0x2Ah	[5:4] Delay1_VBK	DLY1_VBK	@[46h] bit7=0,00(0ms) to 11(6ms) bit7=1,00(0ms)to11(120ms)	bit7=0,2ms bit7=1,40ms	00: 0ms
	[3:2] Delay2_VGL	DLY2_VGL	00(0ms) to 11(15ms)	5ms	01: 5ms
	[1:0] Delay3_VSS	DLY3_VSS	00(0ms) to 11(6ms)	2ms	01: 2ms

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1 Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x2Bh	[7] R/W VCOM1 Address Select	ADDR_SEL	0: E8/E9 address 1: EA/EB address		0: E8/E9
	[6:5] Delay4_AVDD	DLY4_AVDD	00(0ms) to 11(15ms)	5ms	01: 5ms
	[4:3] Delay5_VGH	DLY5_VGH	00(0ms) to 11(6ms)	2ms	01: 2ms
	[2:0] Delay6_VCOM1/2	DLY6_VCOM	000(0ms) to 111(210ms)	30ms	000: 0ms
0x2Ch	[7] All discharge enable	ALL_DIS_EN	0: Disable 1: Enable		1: Enable
	[6] Buck1 discharge	BK_DIS	0: 0.5KΩ 1: 1KΩ		1: 1KΩ
	[5] AVDD discharge	AVDD_DIS	0: 1.4KΩ 1: 4.7KΩ		1: 4.7KΩ
	[4] VGH discharge	VGH_DIS	0: 1.5KΩ 1: 30KΩ		1: 30KΩ
	[3] VGL discharge enable	VGL_DIS	0: Disable 1: 10KΩ		1: 10KΩ
	[2] HAVDD discharge enable	HAVDD_DIS	0: Disable 1: 10KΩ		1: 10KΩ
	[1:0] VCOM1 discharge enable	VCOM1_DIS	00: Disable 01: 20Ω 10: 1KΩ 11: 8KΩ		11: 8KΩ
0x2Dh	[7] VSS discharge enable	VSS_DIS	0: Disable 1: 1.2KΩ		1: 1.2KΩ
	[6] VIN discharge enable	VIN_DIS	0: Disable 1: 4.7KΩ		0: Disable
	[4] VCOM1 delay power off	VCOM1_DLY_OFF	0: VIN_UVLO_F 1: XON discharge threshold		0: VIN_UVLO_F
	[3] HAVDD feedback mode Select	HAVDD_FB	0: (G7+G8)/2 1: HAVDD DAC register		0: (G7+G8)/2
	[2] AVDD GDMOS SCP Select	AVDD_GD_SCP	0: GD_SC_Mode1 Power up of three fail attempts And AVDD FIMV1 detect 1: GD_SC_Mode2 Power Up of three fail attempts And AVDD FIMV2 detect		0: GD_SC_1
	[1] AVDD soft start	AVDD_SS	0: 10ms 1: 20ms		0: 10ms
	[0] VGH soft start	VGH_SS	0: 3ms 1: 6ms		1: 6ms
0x2Eh	[7:4] VGH&VGL_VTC2	VGH_VTC2	0000(0.4V) to 1111(3.4V)	0.2V	1101: 3.0V
	[3:0] VGL&VGL_VTC1	VGH_VTC1	0000(0.4V) to 1111(3.4V)	0.2V	1000: 2.0V
0x2Fh	[7:0] Reserved				

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1 Device Address: 0xE8h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x30h	[5:4] AVDD external Driving of gate	AVDD_EXT_DRV	00: EXT_DRV1_FF 01: EXT_DRV2_F 10: EXT_DRV3_S 11: EXT_ERV4_SS		01: EXT_DRV2_F
	[3:2] VGH boost Converter Compensation	VGH_Boost_COMP	00: VGH_COMP1_FF 01: VGH_COMP2_F 10: VGH_COMP3_S 11: VGH_COMP4_SS		10: VGH_COMP3_S
	[1:0] VGL Inverter Compensation	VGL_Inverter_COMP	00: VGL_COMP1_FF 01: VGL_COMP2_F 10: VGL_COMP3_S 11: VGL_COMP4_SS		10: VGL_COMP3_S
0x31h	[7] EN pin function select	EN_PIN_SEL	0: EN input function 1: XON output function		0: EN input
	[6] Reserved				
	[5] Reserved				
	[4] Reserved				
	[3:0] XON discharge Threshold	XON_DIS_THR	@[46h] bit7=0 00h(6.5V) to 0Fh(10.25V) @[46h] bit7=1 00h(3.63V)to 0Fh(vin_uvlo)	0.25V	0010: 7V
0x44h	[7] SLEEP MODE Enable	SLEEP_EN	0: Disable 1: Enable	0	0: Disable
	[6:5] Sleep power off delay time	SLEEP_POFF_DLY	2ms to 8ms	2ms	0: 2ms
	[2:0] Sleep XAO off delay time	SLEEP_XAO_DLY	0ms to 7ms	1ms	0: SHDN_H
0x45h	[7:1] VCOM2 Normal voltage	VCOM2	VCOM.MIN to VCOM.MAX Res1= (vcom.max-vcom.min)/127	Res1	63*Res1+ VCOM.MIN (7Fh)
0x46h	[7] MNT MODE select	MNT_MODE_EN	0: TV MODE (VIN=12V) 1: MNT MODE (VIN=5V)		0: TV
	[0] VCOM2 Enable	VCOM2_EN	0: Disable 1: Enable		0: Disable

Dummy Byte can by write to mtp and DAC.

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1 Device Address: 0xE8h

Register Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
0xFF	[7:6]&[0] Control Register								00 : Read data from DAC register 01 : Reset data from MTP to DAC register 40 : Write VCOM1 data from DAC to MTP 80 : Write all DAC into EEPROM

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PMIC Register Map:

Only VCOM1 Device Address: 0xE8h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x00h	[4] Down load VCOM1 Data From MTP to DAC register	RESET	0: Disable 1: Enable		0: Disable
	[3] Write VCOM1 data From DAC register to MTP	VCOM1_WR_MTP	0: Disable 1: Enable		0: Disable
	[1] VCOM1 Output Enable	OUT_EN	0: Disable(VCOM1 Hiz) 1: Enable		1: Enable
0x01h	[7:1] VCOM1 voltage	VCOM1	VCOM.MIN to VCOM.MAX Res1= $(vcom.max-vcom.min)/127$	Res1	$63*Res1+VCOMMIN(7Eh)$
0x02h (*Only REG.)	[7] OTP	OTP_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[6] NC	NC			
	[5] VBK UVP or SCP	VBK_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[4] AVDD UVP or SCP	AVDD_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[3] VGH UVP or SCP	VGH_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[2] VGL UVP or SCP	VGL_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[1] VSS UVP	VSS_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[0] HAVDD UVP or SCP	HAVDD_FT	0: Normal 1: Fault Only Fault Indication		0: Normal

VCOM1 control --- 00h,(02h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	RESET	WR to MTP	Reserved	OUT_EN	Reserved
0	0	0	0	0	0	1	0

Bit	Name	Description	
Bit4	RESET	Code	Down load VCOM1 data from MTP to DAC register
		0	Disable
		1	Enable
Bit[3]	WR to MTP	Code	Write VCOM1 data from DAC register to MTP
		0	Disable
		1	Enable
Bit[1]	OUT_EN	Code	VCOM1 DAC output Enable
		0	Disable
		1	Enable

VCOM1 --- 01h,(7Eh)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM1 Normal Voltage Output							Reserved
0	1	1	1	1	1	1	0

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Registers and DAC settings

AVDD output voltage(0x00h) --- Default Code 29h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	AVDD Voltage					
0	0	1	0	1	0	0	1

Bit	Name	Description	
[5:0]	AVDD Voltage	Code	AVDD Switching Current Limit
		00-3F	Table x.1 shows the detailed voltage setup.

Table x.1 AVDD output voltage at TV Mode

DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)
00h	13.5	10h	15.1	20h	16.7	30h	18.3
01h	13.6	11h	15.2	21h	16.8	31h	18.4
02h	13.7	12h	15.3	22h	16.9	32h	18.5
03h	13.8	13h	15.4	23h	17.0	33h	18.6
04h	13.9	14h	15.5	24h	17.1	34h	18.7
05h	14.0	15h	15.6	25h	17.2	35h	18.8
06h	14.1	16h	15.7	26h	17.3	36h	18.9
07h	14.2	17h	15.8	27h	17.4	37h	19.0
08h	14.3	18h	15.9	28h	17.5	38h	19.1
09h	14.4	19h	16.0	29h	17.6	39h	19.2
0Ah	14.5	1Ah	16.1	2Ah	17.7	3Ah	19.3
0Bh	14.6	1Bh	16.2	2Bh	17.8	3Bh	19.4
0Ch	14.7	1Ch	16.3	2Ch	17.9	3Ch	19.5
0Dh	14.8	1Dh	16.4	2Dh	18.0	3Dh	19.6
0Eh	14.9	1Eh	16.5	2Eh	18.1	3Eh	19.7
0Fh	15.0	1Fh	16.6	2Fh	18.2	3Fh	19.8

Table x.1 AVDD output voltage at MNT Mode

DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)
00h	11	10h	12.6	20h	14.2	30h	15.8
01h	11.1	11h	12.7	21h	14.3	31h	15.9
02h	11.2	12h	12.8	22h	14.4	32h	16.0
03h	11.3	13h	12.9	23h	14.5	33h	16.1
04h	11.4	14h	13.0	24h	14.6	34h	16.2
05h	11.5	15h	13.1	25h	14.7	35h	16.3
06h	11.6	16h	13.2	26h	14.8	36h	16.4
07h	11.7	17h	13.3	27h	14.9	37h	16.5
08h	11.8	18h	13.4	28h	15.0	38h	16.6
09h	11.9	19h	13.5	29h	15.1	39h	16.7
0Ah	12.0	1Ah	13.6	2Ah	15.2	3Ah	16.8
0Bh	12.1	1Bh	13.7	2Bh	15.3	3Bh	16.9
0Ch	12.2	1Ch	13.8	2Ch	15.4	3Ch	17.0
0Dh	12.3	1Dh	13.9	2Dh	15.5	3Dh	17.1
0Eh	12.4	1Eh	14.0	2Eh	15.6	3Eh	17.2
0Fh	12.5	1Fh	14.1	2Fh	15.7	3Fh	17.3

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VBK output voltage(0x01h) --- Default Code 1Eh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VBK_MODE	Reserved	Reserved	VBK Voltage				
0	0	0	1	1	1	1	0

Bit	Name	Description	
[7]	VBK MODE		VBK operation mode select
		0	Synchronous
		1	Asynchronous
[4:0]	VBK Voltage	Code	VBK Voltage Output
		00-1F	Table x.2 shows the detailed voltage setup.

Table x.2 VBK output voltage

DAC Value	VBK Voltage(V)	DAC Value	VBK Voltage(V)	DAC Value	VBK Voltage(V)	DAC Value	VBK Voltage(V)
00h	1.80	08h	2.20	10h	2.60	18h	3.00
01h	1.85	09h	2.25	11h	2.65	19h	3.05
02h	1.90	0Ah	2.30	12h	2.70	1Ah	3.10
03h	1.95	0Bh	2.35	13h	2.75	1Bh	3.15
04h	2.00	0Ch	2.40	14h	2.80	1Ch	3.20
05h	2.05	0Dh	2.45	15h	2.85	1Dh	3.25
06h	2.10	0Eh	2.50	16h	2.90	1Eh	3.30
07h	2.15	0Fh	2.55	17h	2.95	1Fh	3.35

HAVDD output voltage(0x02h) --- Default Code 40h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	HAVDD Output Voltage						
0	1	0	0	0	0	0	0

HAVDD=Res2*(HAVDD_CODE+192)

Res2=AVDD/512

HAVDD_CODE=0 ~ 127

DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)
00h	Res2*(0+192)	20h	Res2*(32+192)	40h	Res2*(64+192)	60h	Res2*(96+192)
01h	Res2*(1+192)	21h	Res2*(33+192)	41h	Res2*(65+192)	61h	Res2*(97+192)
02h	Res2*(2+192)	22h	Res2*(34+192)	42h	Res2*(66+192)	62h	Res2*(98+192)
03h	Res2*(3+192)	23h	Res2*(35+192)	43h	Res2*(67+192)	63h	Res2*(99+192)
04h	Res2*(4+192)	24h	Res2*(36+192)	44h	Res2*(68+192)	64h	Res2*(100+192)
05h	Res2*(5+192)	25h	Res2*(37+192)	45h	Res2*(69+192)	65h	Res2*(101+192)
06h	Res2*(6+192)	26h	Res2*(38+192)	46h	Res2*(70+192)	66h	Res2*(102+192)
07h	Res2*(7+192)	27h	Res2*(39+192)	47h	Res2*(71+192)	67h	Res2*(103+192)
08h	Res2*(8+192)	28h	Res2*(40+192)	48h	Res2*(72+192)	68h	Res2*(104+192)
09h	Res2*(9+192)	29h	Res2*(41+192)	49h	Res2*(73+192)	69h	Res2*(105+192)
0Ah	Res2*(10+192)	2Ah	Res2*(42+192)	4Ah	Res2*(74+192)	6Ah	Res2*(106+192)
0Bh	Res2*(11+192)	2Bh	Res2*(43+192)	4Bh	Res2*(75+192)	6Bh	Res2*(107+192)
0Ch	Res2*(12+192)	2Ch	Res2*(44+192)	4Ch	Res2*(76+192)	6Ch	Res2*(108+192)
0Dh	Res2*(13+192)	2Dh	Res2*(45+192)	4Dh	Res2*(77+192)	6Dh	Res2*(109+192)
0Eh	Res2*(14+192)	2Eh	Res2*(46+192)	4Eh	Res2*(78+192)	6Eh	Res2*(110+192)
0Fh	Res2*(15+192)	2Fh	Res2*(47+192)	4Fh	Res2*(79+192)	6Fh	Res2*(111+192)
10h	Res2*(16+192)	30h	Res2*(48+192)	50h	Res2*(80+192)	70h	Res2*(112+192)
11h	Res2*(17+192)	31h	Res2*(49+192)	51h	Res2*(81+192)	71h	Res2*(113+192)
12h	Res2*(18+192)	32h	Res2*(50+192)	52h	Res2*(82+192)	72h	Res2*(114+192)
13h	Res2*(19+192)	33h	Res2*(51+192)	53h	Res2*(83+192)	73h	Res2*(115+192)
14h	Res2*(20+192)	34h	Res2*(52+192)	54h	Res2*(84+192)	74h	Res2*(116+192)
15h	Res2*(21+192)	35h	Res2*(53+192)	55h	Res2*(85+192)	75h	Res2*(117+192)
16h	Res2*(22+192)	36h	Res2*(54+192)	56h	Res2*(86+192)	76h	Res2*(118+192)
17h	Res2*(23+192)	37h	Res2*(55+192)	57h	Res2*(87+192)	77h	Res2*(119+192)
18h	Res2*(24+192)	38h	Res2*(56+192)	58h	Res2*(88+192)	78h	Res2*(120+192)
19h	Res2*(25+192)	39h	Res2*(57+192)	59h	Res2*(89+192)	79h	Res2*(121+192)
1Ah	Res2*(26+192)	3Ah	Res2*(58+192)	5Ah	Res2*(90+192)	7Ah	Res2*(122+192)
1Bh	Res2*(27+192)	3Bh	Res2*(59+192)	5Bh	Res2*(91+192)	7Bh	Res2*(123+192)
1Ch	Res2*(28+192)	3Ch	Res2*(60+192)	5Ch	Res2*(92+192)	7Ch	Res2*(124+192)
1Dh	Res2*(29+192)	3Dh	Res2*(61+192)	5Dh	Res2*(93+192)	7Dh	Res2*(125+192)
1Eh	Res2*(30+192)	3Eh	Res2*(62+192)	5Eh	Res2*(94+192)	7Eh	Res2*(126+192)
1Fh	Res2*(31+192)	3Fh	Res2*(63+192)	5Fh	Res2*(95+192)	7Fh	Res2*(127+192)

VGH_NT output voltage(0x03h) --- Default Code 0Ah

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	VGH_NT				
0	0	0	0	1	0	1	0

Bit	Name	Description
[4:0]	VGH Voltage	Code
		00-1F

VGH Normal Output Voltage
Table x.3 shows the detailed voltage setup.

Table x.3 VGH Normal Output Voltage

DAC Value	VGH_NT Voltage(V)	DAC Value	VGH_NT Voltage(V)	DAC Value	VGH_NT Voltage(V)	DAC Value	VGH_NT Voltage(V)
00h	20	08h	28	10h	36	18h	42
01h	21	09h	29	11h	37	19h	42
02h	22	0Ah	30	12h	38	1Ah	42
03h	23	0Bh	31	13h	39	1Bh	42
04h	24	0Ch	32	14h	40	1Ch	42
05h	25	0Dh	33	15h	41	1Dh	42
06h	26	0Eh	34	16h	42	1Eh	42
07h	27	0Fh	35	17h	42	1Fh	42

VGH_LT output voltage(0x04h) --- Default Code 0Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGH_LT_EN	Reserved	Reserved	VGH_LT[4:0]				
0	0	0	0	1	1	1	1

Bit	Name	Description	
[7]	VGH Temp. Comp.	Code	VGH Temperature Compensation Control
		0	Disable
		1	Enable
[4:0]	VGH LT Voltage	Code	VGH Low Temperature Output Voltage
		00-1F	Table x.4 shows the detailed voltage setup.

Table x.4 VGH Low Temperature Output Voltage

DAC Value	VGH_LT Voltage(V)	DAC Value	VGH_LT Voltage(V)	DAC Value	VGH_LT Voltage(V)	DAC Value	VGH_LT Voltage(V)
00h	20	08h	28	10h	36	18h	42
01h	21	09h	29	11h	37	19h	42
02h	22	0Ah	30	12h	38	1Ah	42
03h	23	0Bh	31	13h	39	1Bh	42
04h	24	0Ch	32	14h	40	1Ch	42
05h	25	0Dh	33	15h	41	1Dh	42
06h	26	0Eh	34	16h	42	1Eh	42
07h	27	0Fh	35	17h	42	1Fh	42

VGL output voltage(0x05h) --- Default Code 0Ah

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGL_NT_OFF	Reserved	Reserved	VGL_NT				
0	0	0	0	1	0	1	0

Bit	Name	Description	
[7]	VGL Output offset	Code	VGL Normal Output Voltage Offset
		0	Disable
		1	Enable VGL_NT-0.25V
[4:0]	VGH Normal OUT	Code	VGL Normal Output Voltage
		00-1F	Table x.5 shows the detailed voltage setup.

Table x.5 VGL Normal Output Voltage

DAC Value	VGL_NT Voltage(V)	DAC Value	VGL_NT Voltage(V)	DAC Value	VGL_NT Voltage(V)	DAC Value	VGL_NT Voltage(V)
00h	-3.0	08h	-7.0	10h	-11.0	18h	-15.0
01h	-3.5	09h	-7.5	11h	-11.5	19h	-15.5
02h	-4.0	0Ah	-8.0	12h	-12.0	1Ah	-16.0
03h	-4.5	0Bh	-8.5	13h	-12.5	1Bh	-16.5
04h	-5.0	0Ch	-9.0	14h	-13.0	1Ch	-17.0
05h	-5.5	0Dh	-9.5	15h	-13.5	1Dh	-17.5
06h	-6.0	0Eh	-10.0	16h	-14.0	1Eh	-18.0
07h	-6.5	0Fh	-10.5	17h	-14.5	1Fh	-18.0

Dummy Byte (0x06h) --- Default Code 12h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy
0	0	0	1	0	0	1	0

Dummy Byte can be written to mtp and DAC.

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VSS output voltage(0x07h) --- Default Code 06h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Dummy	VSS_OFF	Reserved	VSS				
0	0	0	0	0	1	1	0

Bit	Name	Description	
[6]	VSS Offset	Code	VSS Output Voltage Offset
		0	Disable Offset
		1	Enable Offset, VSS-0.25V
[4:0]	VSS Normal OUT	Code	VSS Normal Output Voltage
		00-1F	Table x.7 shows the detailed voltage setup.

Table x.7 VSS Normal Output Voltage

DAC Value	VSS Voltage(V)	DAC Value	VSS Voltage(V)	DAC Value	VSS Voltage(V)	DAC Value	VSS Voltage(V)
00h	-3.0	08h	-7.0	10h	-11.0	18h	-15.0
01h	-3.5	09h	-7.5	11h	-11.5	19h	-15.5
02h	-4.0	0Ah	-8.0	12h	-12.0	1Ah	-16.0
03h	-4.5	0Bh	-8.5	13h	-12.5	1Bh	-16.0
04h	-5.0	0Ch	-9.0	14h	-13.0	1Ch	-16.0
05h	-5.5	0Dh	-9.5	15h	-13.5	1Dh	-16.0
06h	-6.0	0Eh	-10.0	16h	-14.0	1Eh	-16.0
07h	-6.5	0Fh	-10.5	17h	-14.5	1Fh	-16.0

Dummy bit can be write to MTP and DAC.

VCOM1 output voltage(0x08h) --- Default Code 7Eh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM1 Output Voltage							Reserved
0	1	1	1	1	1	1	0

DAC Value	VCOM1 Voltage(V)	DAC Value	VCOM1 Voltage(V)	DAC Value	VCOM1 Voltage(V)	DAC Value	VCOM1 Voltage(V)
00h	0*Res1+V.MIN	40h	32*Res1+V.MIN	80h	64*Res1+V.MIN	C0h	96*Res1+V.MIN
02h	1*Res1+V.MIN	42h	33*Res1+V.MIN	82h	65*Res1+V.MIN	C2h	97*Res1+V.MIN
04h	2*Res1+V.MIN	44h	34*Res1+V.MIN	84h	66*Res1+V.MIN	C4h	98*Res1+V.MIN
06h	3*Res1+V.MIN	46h	35*Res1+V.MIN	86h	67*Res1+V.MIN	C6h	99*Res1+V.MIN
08h	4*Res1+V.MIN	48h	36*Res1+V.MIN	88h	68*Res1+V.MIN	C8h	100*Res1+V.MIN
0Ah	5*Res1+V.MIN	4Ah	37*Res1+V.MIN	8Ah	69*Res1+V.MIN	CAh	101*Res1+V.MIN
0Ch	6*Res1+V.MIN	4Ch	38*Res1+V.MIN	8Ch	70*Res1+V.MIN	CCh	102*Res1+V.MIN
0Eh	7*Res1+V.MIN	4Eh	39*Res1+V.MIN	8Eh	71*Res1+V.MIN	CEh	103*Res1+V.MIN
10h	8*Res1+V.MIN	50h	40*Res1+V.MIN	90h	72*Res1+V.MIN	D0h	104*Res1+V.MIN
12h	9*Res1+V.MIN	52h	41*Res1+V.MIN	92h	73*Res1+V.MIN	D2h	105*Res1+V.MIN
14h	10*Res1+V.MIN	54h	42*Res1+V.MIN	94h	74*Res1+V.MIN	D4h	106*Res1+V.MIN
16h	11*Res1+V.MIN	56h	43*Res1+V.MIN	96h	75*Res1+V.MIN	D6h	107*Res1+V.MIN
18h	12*Res1+V.MIN	58h	44*Res1+V.MIN	98h	76*Res1+V.MIN	D8h	108*Res1+V.MIN
1Ah	13*Res1+V.MIN	5Ah	45*Res1+V.MIN	9Ah	77*Res1+V.MIN	DAh	109*Res1+V.MIN
1Ch	14*Res1+V.MIN	5Ch	46*Res1+V.MIN	9Ch	78*Res1+V.MIN	DCh	110*Res1+V.MIN
1Eh	15*Res1+V.MIN	5Eh	47*Res1+V.MIN	9Eh	79*Res1+V.MIN	DEh	111*Res1+V.MIN
20h	16*Res1+V.MIN	60h	48*Res1+V.MIN	A0h	80*Res1+V.MIN	E0h	112*Res1+V.MIN
22h	17*Res1+V.MIN	62h	49*Res1+V.MIN	A2h	81*Res1+V.MIN	E2h	113*Res1+V.MIN
24h	18*Res1+V.MIN	64h	50*Res1+V.MIN	A4h	82*Res1+V.MIN	E4h	114*Res1+V.MIN
26h	19*Res1+V.MIN	66h	51*Res1+V.MIN	A6h	83*Res1+V.MIN	E6h	115*Res1+V.MIN
28h	20*Res1+V.MIN	68h	52*Res1+V.MIN	A8h	84*Res1+V.MIN	E8h	116*Res1+V.MIN
2Ah	21*Res1+V.MIN	6Ah	53*Res1+V.MIN	AAh	85*Res1+V.MIN	EAh	117*Res1+V.MIN
2Ch	22*Res1+V.MIN	6Ch	54*Res1+V.MIN	ACh	86*Res1+V.MIN	ECh	118*Res1+V.MIN
2Eh	23*Res1+V.MIN	6Eh	55*Res1+V.MIN	A Eh	87*Res1+V.MIN	EEh	119*Res1+V.MIN
30h	24*Res1+V.MIN	70h	56*Res1+V.MIN	B0h	88*Res1+V.MIN	F0h	120*Res1+V.MIN
32h	25*Res1+V.MIN	72h	57*Res1+V.MIN	B2h	89*Res1+V.MIN	F2h	121*Res1+V.MIN
34h	26*Res1+V.MIN	74h	58*Res1+V.MIN	B4h	90*Res1+V.MIN	F4h	122*Res1+V.MIN
36h	27*Res1+V.MIN	76h	59*Res1+V.MIN	B6h	91*Res1+V.MIN	F6h	123*Res1+V.MIN
38h	28*Res1+V.MIN	78h	60*Res1+V.MIN	B8h	92*Res1+V.MIN	F8h	124*Res1+V.MIN
3Ah	29*Res1+V.MIN	7Ah	61*Res1+V.MIN	BAh	93*Res1+V.MIN	FAh	125*Res1+V.MIN
3Ch	30*Res1+V.MIN	7Ch	62*Res1+V.MIN	BCh	94*Res1+V.MIN	FCh	126*Res1+V.MIN
3Eh	31*Res1+V.MIN	7Eh	63*Res1+V.MIN	BEh	95*Res1+V.MIN	FEh	127*Res1+V.MIN

VCOM1 voltage formula

$VCOM1 = Res1 * VCOM1\ CODE + VCOMMIN$

$Res1 = (VCOMMAX - VCOMMIN) / 127$

VCOM1 CODE=0 ~ 127

Dummy Byte (0x09h) --- Default Code BAh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy
1	0	1	1	1	0	1	0

Dummy Byte can be written to mtp and DAC.

Preliminary

VCOM_MAX output voltage(0x0Ah) --- Default Code 3Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	VCOM_MAX						
0	0	1	1	1	1	1	1

DAC Value	VCOM_MAX Voltage(V)	DAC Value	VCOM_MAX Voltage(V)	DAC Value	VCOM_MAX Voltage(V)	DAC Value	VCOM_MAX Voltage(V)
00h	1*Res3	20h	33*Res3	40h	65*Res3	60h	97*Res3
01h	2*Res3	21h	34*Res3	41h	66*Res3	61h	98*Res3
02h	3*Res3	22h	35*Res3	42h	67*Res3	62h	99*Res3
03h	4*Res3	23h	36*Res3	43h	68*Res3	63h	100*Res3
04h	5*Res3	24h	37*Res3	44h	69*Res3	64h	101*Res3
05h	6*Res3	25h	38*Res3	45h	70*Res3	65h	102*Res3
06h	7*Res3	26h	39*Res3	46h	71*Res3	66h	103*Res3
07h	8*Res3	27h	40*Res3	47h	72*Res3	67h	104*Res3
08h	9*Res3	28h	41*Res3	48h	73*Res3	68h	105*Res3
09h	10*Res3	29h	42*Res3	49h	74*Res3	69h	106*Res3
0Ah	11*Res3	2Ah	43*Res3	4Ah	75*Res3	6Ah	107*Res3
0Bh	12*Res3	2Bh	44*Res3	4Bh	76*Res3	6Bh	108*Res3
0Ch	13*Res3	2Ch	45*Res3	4Ch	77*Res3	6Ch	109*Res3
0Dh	14*Res3	2Dh	46*Res3	4Dh	78*Res3	6Dh	110*Res3
0Eh	15*Res3	2Eh	47*Res3	4Eh	79*Res3	6Eh	111*Res3
0Fh	16*Res3	2Fh	48*Res3	4Fh	80*Res3	6Fh	112*Res3
10h	17*Res3	30h	49*Res3	50h	81*Res3	70h	113*Res3
11h	18*Res3	31h	50*Res3	51h	82*Res3	71h	114*Res3
12h	19*Res3	32h	51*Res3	52h	83*Res3	72h	115*Res3
13h	20*Res3	33h	52*Res3	53h	84*Res3	73h	116*Res3
14h	21*Res3	34h	53*Res3	54h	85*Res3	74h	117*Res3
15h	22*Res3	35h	54*Res3	55h	86*Res3	75h	118*Res3
16h	23*Res3	36h	55*Res3	56h	87*Res3	76h	119*Res3
17h	24*Res3	37h	56*Res3	57h	88*Res3	77h	120*Res3
18h	25*Res3	38h	57*Res3	58h	89*Res3	78h	121*Res3
19h	26*Res3	39h	58*Res3	59h	90*Res3	79h	122*Res3
1Ah	27*Res3	3Ah	59*Res3	5Ah	91*Res3	7Ah	123*Res3
1Bh	28*Res3	3Bh	60*Res3	5Bh	92*Res3	7Bh	124*Res3
1Ch	29*Res3	3Ch	61*Res3	5Ch	93*Res3	7Ch	125*Res3
1Dh	30*Res3	3Dh	62*Res3	5Dh	94*Res3	7Dh	126*Res3
1Eh	31*Res3	3Eh	63*Res3	5Eh	95*Res3	7Eh	127*Res3
1Fh	32*Res3	3Fh	63*Res3	5Fh	96*Res3	7Fh	128*Res3

VCOM_MAX voltage formula
 $VCOM_MAX = Res3 * [(VCOM_MAX\ CODE) + 1]$
 $Res3 = VA_{VDD} / 128$

VCOM_MIN output voltage(0x0Bh) --- Default Code 26h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	VCOM_MIN						
0	0	1	0	0	1	1	0

DAC Value	VCOM_MIN Voltage(V)	DAC Value	VCOM_MIN Voltage(V)	DAC Value	VCOM_MIN Voltage(V)	DAC Value	VCOM_MIN Voltage(V)
00h	0*Res3	20h	32*Res3	40h	64*Res3	60h	96*Res3
01h	1*Res3	21h	33*Res3	41h	65*Res3	61h	97*Res3
02h	2*Res3	22h	34*Res3	42h	66*Res3	62h	98*Res3
03h	3*Res3	23h	35*Res3	43h	67*Res3	63h	99*Res3
04h	4*Res3	24h	36*Res3	44h	68*Res3	64h	100*Res3
05h	5*Res3	25h	37*Res3	45h	69*Res3	65h	101*Res3
06h	6*Res3	26h	38*Res3	46h	70*Res3	66h	102*Res3
07h	7*Res3	27h	39*Res3	47h	71*Res3	67h	103*Res3
08h	8*Res3	28h	40*Res3	48h	72*Res3	68h	104*Res3
09h	9*Res3	29h	41*Res3	49h	73*Res3	69h	105*Res3
0Ah	10*Res3	2Ah	42*Res3	4Ah	74*Res3	6Ah	106*Res3
0Bh	11*Res3	2Bh	43*Res3	4Bh	75*Res3	6Bh	107*Res3
0Ch	12*Res3	2Ch	44*Res3	4Ch	76*Res3	6Ch	108*Res3
0Dh	13*Res3	2Dh	45*Res3	4Dh	77*Res3	6Dh	109*Res3
0Eh	14*Res3	2Eh	46*Res3	4Eh	78*Res3	6Eh	110*Res3
0Fh	15*Res3	2Fh	47*Res3	4Fh	79*Res3	6Fh	111*Res3
10h	16*Res3	30h	48*Res3	50h	80*Res3	70h	112*Res3
11h	17*Res3	31h	49*Res3	51h	81*Res3	71h	113*Res3
12h	18*Res3	32h	50*Res3	52h	82*Res3	72h	114*Res3
13h	19*Res3	33h	51*Res3	53h	83*Res3	73h	115*Res3
14h	20*Res3	34h	52*Res3	54h	84*Res3	74h	116*Res3
15h	21*Res3	35h	53*Res3	55h	85*Res3	75h	117*Res3
16h	22*Res3	36h	54*Res3	56h	86*Res3	76h	118*Res3
17h	23*Res3	37h	55*Res3	57h	87*Res3	77h	119*Res3
18h	24*Res3	38h	56*Res3	58h	88*Res3	78h	120*Res3
19h	25*Res3	39h	57*Res3	59h	89*Res3	79h	121*Res3
1Ah	26*Res3	3Ah	58*Res3	5Ah	90*Res3	7Ah	122*Res3
1Bh	27*Res3	3Bh	59*Res3	5Bh	91*Res3	7Bh	123*Res3
1Ch	28*Res3	3Ch	60*Res3	5Ch	92*Res3	7Ch	124*Res3
1Dh	29*Res3	3Dh	61*Res3	5Dh	93*Res3	7Dh	125*Res3
1Eh	30*Res3	3Eh	62*Res3	5Eh	94*Res3	7Eh	126*Res3
1Fh	31*Res3	3Fh	63*Res3	5Fh	95*Res3	7Fh	127*Res3

VCOM_MIN voltage formula
 $VCOM_MIN = Res3 * (VCOM_MIN\ CODE)$
 $Res3 = VA_{VDD} / 128$

GAMMA 1~14 output voltage(0x0Ch~0x27h)

Address	Name	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0Ch	GMA1	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x0Dh	GMA1	00h	0	0	0	0	0	0	0	0
0x0Eh	GMA2	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x0Fh	GMA2	00h	0	0	0	0	0	0	0	0
0x10h	GMA3	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x11h	GMA3	00h	0	0	0	0	0	0	0	0
0x12h	GMA4	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x13h	GMA4	00h	0	0	0	0	0	0	0	0
0x14h	GMA5	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x15h	GMA5	00h	0	0	0	0	0	0	0	0
0x16h	GMA6	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x17h	GMA6	00h	0	0	0	0	0	0	0	0
0x18h	GMA7	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x19h	GMA7	00h	0	0	0	0	0	0	0	0
0x1Ah	GMA8	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x1Bh	GMA8	00h	0	0	0	0	0	0	0	0
0x1Ch	GMA9	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x1Dh	GMA9	00h	0	0	0	0	0	0	0	0
0x1Eh	GMA10	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x1Fh	GMA10	00h	0	0	0	0	0	0	0	0
0x20h	GMA11	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x21h	GMA11	00h	0	0	0	0	0	0	0	0
0x22h	GMA12	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x23h	GMA12	00h	0	0	0	0	0	0	0	0
0x24h	GMA13	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x25h	GMA13	00h	0	0	0	0	0	0	0	0
0x26h	GMA14	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x27h	GMA14	00h	0	0	0	0	0	0	0	0

VGAMMA 1~14 voltage formula

$$V_{\text{GAMMA 1~14}} = \text{Res4} * V_{\text{GAMMA 1~14_CODE}}$$

$$\text{Res4} = V_{\text{AVDD}} / 1024$$

GAMMA 1~14 output voltage (Unit:V)

DAC value	GAMMA 1~14	DAC value	GAMMA 1~14
0000h	0	0200h	Res4*512
0001h	Res4*1	0201h	Res4*513
0002h	Res4*2	0202h	Res4*514
0003h	Res4*3	0203h	Res4*515
0004h	Res4*4	0204h	Res4*516
0005h	Res4*5	0205h	Res4*517
0006h	Res4*6	0206h	Res4*518
0007h	Res4*7	0207h	Res4*519
0008h	Res4*8	0208h	Res4*520
0009h	Res4*9	0209h	Res4*521
000Ah	Res4*10	020Ah	Res4*522
000Bh	Res4*11	020Bh	Res4*523
000Ch	Res4*12	020Ch	Res4*524
000Dh	Res4*13	020Dh	Res4*525
000Eh	Res4*14	020Eh	Res4*526
000Fh	Res4*15	020Fh	Res4*527
.....
.....
01F0h	Res4*496	03F0h	Res4*1008
01F1h	Res4*497	03F1h	Res4*1009
01F2h	Res4*498	03F2h	Res4*1010
01F3h	Res4*499	03F3h	Res4*1011
01F4h	Res4*500	03F4h	Res4*1012
01F5h	Res4*501	03F5h	Res4*1013
01F6h	Res4*502	03F6h	Res4*1014
01F7h	Res4*503	03F7h	Res4*1015
01F8h	Res4*504	03F8h	Res4*1016
01F9h	Res4*505	03F9h	Res4*1017
01FAh	Res4*506	03FAh	Res4*1018
01FBh	Res4*507	03FBh	Res4*1019
01FCh	Res4*508	03FCh	Res4*1020
01FDh	Res4*509	03FDh	Res4*1021
01FEh	Res4*510	03FEh	Res4*1022
01FFh	Res4*511	03FFh	Res4*1023

Channel Enable Register(0x28h) --- Default Code 7Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GroupB_EN	VGL_EN	VSS_EN	AVDD_EN	HAVDD_EN	GMA_EN	VCOM1_EN	VGH_EN
0	1	1	1	1	1	1	1

Bit	Name	Description	
[7]	Group_B_EN	Code	Group B Enable Control (Group B: AVDD,HAVDD,VGH,VGL,VSS,GMA _n ,VCOM1,VCOM2)
		0	Disable
		1	Enable
[6]	VGL_EN	Code	VGL Enable Control
		0	Disable
		1	Enable
[5]	VSS_EN	Code	VSS Enable Control
		0	Disable
		1	Enable
[4]	AVDD_EN	Code	AVDD Enable Control
		0	Disable
		1	Enable
[3]	HAVDD_EN	Code	HAVDD Enable Control
		0	Disable
		1	Enable
[2]	GMA_EN	Code	GMA _n Enable Control
		0	Disable
		1	Enable
[1]	VCOM1_EN	Code	VCOM1 Enable Control
		0	Disable
		1	Enable
[0]	VGH_EN	Code	VGH Enable Control
		0	Disable
		1	Enable

Function Setting(0x29h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FREQ1	FREQ2	ISO_MOS_SEL	AVDD_MOS_SEL	Reserved	Reserved	Dummy	GMA_CH_SEL
0	0	0	0	0	0	0	0

Bit	Name	Description
[7]	FREQ_SEL1	Code Operation Frequency select (VBK, AVDD, VGH, VGL)
		0 750KHz
		1 500KHz
[6]	FREQ_SEL2	Code Operation Frequency select (VBK, AVDD, VGH, VGL)
		0 Follow 0x29h[7] setting
		1 1250KHz
[5]	ISO_MOS_SEL	Code Isolation PMOS Internal/External select
		0 External Isolation PMOS
		1 Internal Isolation PMOS
[4]	AVDD_NMOS_SEL	Code AVDD Switching NMOS Internal/External select
		0 Internal Switching NMOS
		1 External Switching NMOS
[0]	GMA_CH_SEL	Code The number of output GMA channels is selected
		0 14 Channels GMA Output
		1 4 Channels GMA Output (GMA1, GMA7, GMA8, GMA14)

Preliminary

Delay time Setting(0x2Ah) --- Default Code 05h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	DLY1_VBK		DLY2_VGL		DLY3_VSS	
0	0	0	0	0	1	0	1

Bit	Name	Description
[5:4]	DLY1_VBK	Code VBK Power on Delay time at TV Mode (0x46h[7]=0)
		00 0ms
		01 2ms
		10 4ms
		11 6ms
		Code VBK Power on Delay time at MNT Mode (0x46h[7]=1)
		00 0ms
		01 40ms
		10 80ms
		11 120ms
[3:2]	DLY2_VGL	Code VGL Power on Delay Time
		00 0ms
		01 5ms
		10 10ms
		11 15ms
[1:0]	DLY3_VSS	Code VSS Power on Delay Time
		00 0ms
		01 2ms
		10 4ms
		11 6ms

Delay time Setting(0x2Bh) --- Default Code 28h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDR_SEL	DLY4_AVDD		DLY5_VGH		DLY6_VCOM		
0	0	1	0	1	0	0	0

Bit	Name	Description	
[7]	Write VCOM Addr. Select	Code	Programming VCOM1 address selection
		0	Address is 0xE8h Write VCOM1
		1	Address is 0xE9h Write VCOM1
[5:4]	DLY4_AVDD	Code	AVDD Power on Delay Time
		00	0ms
		01	5ms
		10	10ms
		11	15ms
[3:2]	DLY5_VGH	Code	VGH Power on Delay Time
		00	0ms
		01	2ms
		10	4ms
		11	6ms
[1:0]	DLY6_VCOM1/2	Code	VCOM1&VCOM2 Power on Delay Time
		000	0ms
		001	30ms
		010	60ms
		011	90ms
		100	120ms
		101	150ms
		110	180ms
		111	210ms

Discharge Setting(0x2Ch) --- Default Code FFh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ALL_DCGH_EN	BK_DCGH	AVDD_DCGH	VGH_DCGH	VGL_DCGH	HAVDD_DCGH	VCOM1_DCGH	
1	1	1	1	1	1	1	1

Bit	Name	Description	
[7]	ALL_DCGH_EN	Code	All Output Channel Discharge Control
		0	Enable Discharge Function
		1	Disable Discharge Function
[6]	BK_DCGH	Code	VBK Discharge Select
		0	0.5KΩ
		1	1.0KΩ
[5]	AVDD_DCGH	Code	AVDD Discharge Select
		0	1.4KΩ
		1	4.7KΩ
[4]	VGH_DCGH	Code	VGH Discharge Select
		0	1.5KΩ
		1	30KΩ
[3]	VGL_DCGH	Code	VGL Discharge Select
		0	Disable Discharge Function
		1	10KΩ
[2]	HAVDD_DCGH	Code	HAVDD Discharge Select
		0	Disable Discharge Function
		1	1.0KΩ
[1:0]	VCOM1_DCGH	Code	VCOM1 Discharge Select
		00	Disable Discharge Function
		01	20Ω
		10	1.0KΩ
		11	8.0KΩ

Function Setting (0x2Dh) --- Default Code 80h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VSS_DCGH	VIN_DCGH	Reserved	VCOM1_POFF_DLY	HAVDD_FB	AVDD_GD_SCP	AVDD_SS	VGH_SS
1	0	0	0	0	0	0	0

Bit	Name	Description
[7]	VSS_DCGH	Code VSS Discharge Select
		0 Disable Discharge Function
		1 1.2KΩ
[6]	VIN_DCGH	Code INBK Discharge Select
		0 Disable Discharge Function
		1 4.7KΩ
[4]	VCOM1_POFF_DLY	Code VCOM1 Power off Follow
		0 Power off Follow VIN_UVLO_F
		1 Power off Follow XAO Discharge Threshold
[3]	HAVDD_FB	Code HAVDD Feedback Mode Select
		0 HAVDD Feedback Voltage is (GMA7+GMA8)/2
		1 HAVDD Feedback Voltage is Follow HAVDD DAC Code
[2]	AVDD_GD_SCP	Code AVDD Power on GDMOS SCP select
		0 GD_SCP_MODE1 Power up of three fail attempts and AVDD FIMV1 detect
		1 GD_SCP_MODE2 Power up of three fail attempts and AVDD FIMV2 detect
[1]	AVDD_SS	Code AVDD Power on Softstart Time
		0 10ms
		1 20ms
[0]	VGH_SS	Code VGH Power on Softstart Time
		0 3ms
		1 6ms

VGH&VGL_VTC1 & VTC2 (0x2Eh) --- Default Code D8h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGH_VTC2				VGH_VTC1			
1	1	0	1	1	0	0	0

Bit	Name	Description	
[7:4]	VGH_VTC2	Code	VGH Temperature Compensated Detect Voltage 2
		0000	0.4V
		0001	0.6V
		0010	0.8V
		0011	1.0V
		0100	1.2V
		0101	1.4V
		0110	1.6V
		0111	1.8V
		1000	2.0V
		1001	2.2V
		1010	2.4V
		1011	2.6V
		1100	2.8V
		1101	3.0V
		1110	3.2V
1111	3.4V		
[3:0]	VGH_VTC1	Code	VGH Temperature Compensated Detect Voltage 1
		0000	0.4V
		0001	0.6V
		0010	0.8V
		0011	1.0V
		0100	1.2V
		0101	1.4V
		0110	1.6V
		0111	1.8V
		1000	2.0V
		1001	2.2V
		1010	2.4V
		1011	2.6V
		1100	2.8V
		1101	3.0V
		1110	3.2V
1111	3.4V		

Dummy Byte (0x2Fh) --- Default Code 41h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy
0	1	0	0	0	0	0	1

Dummy Byte can be written to mtp and DAC.

Preliminary

Compensation Control (0x30h) --- Default Code 1Ah

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	AVDD_EXT_DRV		VGH_COMP		VGL_COMP	
0	0	0	1	1	0	1	0

Bit	Name	Description	
[5:4]	AVDD_EXT_DRV	Code	AVDD external driving of Gate
		00	AVDD External Gate Driver FF
		01	AVDD External Gate Driver F
		10	AVDD External Gate Driver S
		11	AVDD External Gate Driver SS
[3:2]	VGH_COMP	Code	VGH boost converter internal compensation
		00	VGH_COMP1_FF
		01	VGH_COMP2_F
		10	VGH_COMP3_S
		11	VGH_COMP4_SS
[1:0]	VGL_COMP	Code	VGL inverting internal compensation
		00	VGL_COMP1_FF
		01	VGL_COMP2_F
		10	VGL_COMP3_S
		11	VGL_COMP4_SS

Preliminary

XON discharge threshold (0x31h) --- Default Code 02h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_PIN_SEL	Dummy	Dummy	Dummy	XON_DIS_TH			
0	0	0	0	0	0	1	0

Bit	Name	Description	
[7]	EN_PIN_SEL	Code	EN Pin Function Select
		0	EN Input Control Function
		1	XAO Output Function

Dummy Byte can by write to MTP and DAC.

Preliminary

Bit	Name	Description	
[3:0]	XAO_TH	Code	XAO detects the threshold voltage at TV MODE
		0000	6.50V
		0001	6.75V
		0010	7.00V
		0011	7.25V
		0100	7.50V
		0101	7.75V
		0110	8.00V
		0111	8.25V
		1000	8.50V
		1001	8.75V
		1010	9.00V
		1011	9.25V
		1100	9.50V
		1101	9.75V
		1110	10.00V
		1111	10.25V
		Code	XAO detects the threshold voltage at MNT MODE
		0000	3.62
		0001	3.76
		0010	3.90
		0011	4.04
		0100	4.18
		0101	4.32
		0110	4.46
		0111	4.60
		1000	4.74
		1001	4.88
		1010	5.02
		1011	5.16
		1100	5.30
		1101	5.44
1110	5.58		
1111	VIN_UVLO_Falling		

Sleep Control (0x44h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SLEEP_EN	SLEEP_POFF_DLY		Reserved	SLEEP_XAO_DLY			
0	0	0	0	0	0	0	0

Bit	Name	Description	
[7]	SLEEP_EN	Code	Sleep Mode Enable Control
		0	Disable
		1	Enable (SHDN Pin High Level Control Enter Sleep)
[6:5]	SLEEP_POFF_DLY	Code	Sleep Enable Power off Delay Time
		00	2ms (Start with the SHDN pull up level)
		01	4ms (Start with the SHDN pull up level)
		10	6ms (Start with the SHDN pull up level)
		11	8ms (Start with the SHDN pull up level)
[2:0]	SLEEP_XAO_POFF_DLY	Code	Sleep Enable XAO Pull Low Delay Time
		000	0ms (Start with the SHDN pull up level)
		001	1ms (Start with the SHDN pull up level)
		010	2ms (Start with the SHDN pull up level)
		011	3ms (Start with the SHDN pull up level)
		100	4ms (Start with the SHDN pull up level)
		101	5ms (Start with the SHDN pull up level)
		110	6ms (Start with the SHDN pull up level)
		111	7ms (Start with the SHDN pull up level)

VCOM2 output voltage(0x45h) --- Default Code 7Eh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM2							Reserved
0	1	1	1	1	1	1	0

DAC Value	VCOM2 Voltage(V)	DAC Value	VCOM2 Voltage(V)	DAC Value	VCOM2 Voltage(V)	DAC Value	VCOM2 Voltage(V)
00h	0*Res1+V.MIN	40h	32*Res1+V.MIN	80h	64*Res1+V.MIN	C0h	96*Res1+V.MIN
02h	1*Res1+V.MIN	42h	33*Res1+V.MIN	82h	65*Res1+V.MIN	C2h	97*Res1+V.MIN
04h	2*Res1+V.MIN	44h	34*Res1+V.MIN	84h	66*Res1+V.MIN	C4h	98*Res1+V.MIN
06h	3*Res1+V.MIN	46h	35*Res1+V.MIN	86h	67*Res1+V.MIN	C6h	99*Res1+V.MIN
08h	4*Res1+V.MIN	48h	36*Res1+V.MIN	88h	68*Res1+V.MIN	C8h	100*Res1+V.MIN
0Ah	5*Res1+V.MIN	4Ah	37*Res1+V.MIN	8Ah	69*Res1+V.MIN	CAh	101*Res1+V.MIN
0Ch	6*Res1+V.MIN	4Ch	38*Res1+V.MIN	8Ch	70*Res1+V.MIN	CCh	102*Res1+V.MIN
0Eh	7*Res1+V.MIN	4Eh	39*Res1+V.MIN	8Eh	71*Res1+V.MIN	CEh	103*Res1+V.MIN
10h	8*Res1+V.MIN	50h	40*Res1+V.MIN	90h	72*Res1+V.MIN	D0h	104*Res1+V.MIN
12h	9*Res1+V.MIN	52h	41*Res1+V.MIN	92h	73*Res1+V.MIN	D2h	105*Res1+V.MIN
14h	10*Res1+V.MIN	54h	42*Res1+V.MIN	94h	74*Res1+V.MIN	D4h	106*Res1+V.MIN
16h	11*Res1+V.MIN	56h	43*Res1+V.MIN	96h	75*Res1+V.MIN	D6h	107*Res1+V.MIN
18h	12*Res1+V.MIN	58h	44*Res1+V.MIN	98h	76*Res1+V.MIN	D8h	108*Res1+V.MIN
1Ah	13*Res1+V.MIN	5Ah	45*Res1+V.MIN	9Ah	77*Res1+V.MIN	DAh	109*Res1+V.MIN
1Ch	14*Res1+V.MIN	5Ch	46*Res1+V.MIN	9Ch	78*Res1+V.MIN	DCh	110*Res1+V.MIN
1Eh	15*Res1+V.MIN	5Eh	47*Res1+V.MIN	9Eh	79*Res1+V.MIN	DEh	111*Res1+V.MIN
20h	16*Res1+V.MIN	60h	48*Res1+V.MIN	A0h	80*Res1+V.MIN	E0h	112*Res1+V.MIN
22h	17*Res1+V.MIN	62h	49*Res1+V.MIN	A2h	81*Res1+V.MIN	E2h	113*Res1+V.MIN
24h	18*Res1+V.MIN	64h	50*Res1+V.MIN	A4h	82*Res1+V.MIN	E4h	114*Res1+V.MIN
26h	19*Res1+V.MIN	66h	51*Res1+V.MIN	A6h	83*Res1+V.MIN	E6h	115*Res1+V.MIN
28h	20*Res1+V.MIN	68h	52*Res1+V.MIN	A8h	84*Res1+V.MIN	E8h	116*Res1+V.MIN
2Ah	21*Res1+V.MIN	6Ah	53*Res1+V.MIN	AAh	85*Res1+V.MIN	EAh	117*Res1+V.MIN
2Ch	22*Res1+V.MIN	6Ch	54*Res1+V.MIN	ACh	86*Res1+V.MIN	ECh	118*Res1+V.MIN
2Eh	23*Res1+V.MIN	6Eh	55*Res1+V.MIN	A Eh	87*Res1+V.MIN	EEh	119*Res1+V.MIN
30h	24*Res1+V.MIN	70h	56*Res1+V.MIN	B0h	88*Res1+V.MIN	F0h	120*Res1+V.MIN
32h	25*Res1+V.MIN	72h	57*Res1+V.MIN	B2h	89*Res1+V.MIN	F2h	121*Res1+V.MIN
34h	26*Res1+V.MIN	74h	58*Res1+V.MIN	B4h	90*Res1+V.MIN	F4h	122*Res1+V.MIN
36h	27*Res1+V.MIN	76h	59*Res1+V.MIN	B6h	91*Res1+V.MIN	F6h	123*Res1+V.MIN
38h	28*Res1+V.MIN	78h	60*Res1+V.MIN	B8h	92*Res1+V.MIN	F8h	124*Res1+V.MIN
3Ah	29*Res1+V.MIN	7Ah	61*Res1+V.MIN	BAh	93*Res1+V.MIN	FAh	125*Res1+V.MIN
3Ch	30*Res1+V.MIN	7Ch	62*Res1+V.MIN	BCh	94*Res1+V.MIN	FCh	126*Res1+V.MIN
3Eh	31*Res1+V.MIN	7Eh	63*Res1+V.MIN	BEh	95*Res1+V.MIN	FEh	127*Res1+V.MIN

VCOM2 voltage formula

$VCOM2 = Res1 * VCOM2\ CODE + VCOMMIN$

$Res1 = (VCOMMAX - VCOMMIN) / 127$

VCOM2 CODE=0 ~ 127

MNT&TV (0x46h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MODE_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCOM2_EN
0	0	0	0	0	0	0	0

Bit	Name	Description	
[7]	MNT/TV_MODE_SEL	Code	MNT&TV Mode Select
		0	TV MODE (VIN=12.0V Typical)
		1	MNT MODE (VIN=5.0V Typical)
[0]	VCOM2_EN	Code	VCOM2 Enable Control
		0	Disable
		1	Enable (HAVDD FB Pin Output VCOM2)

Preliminary

Protection Table

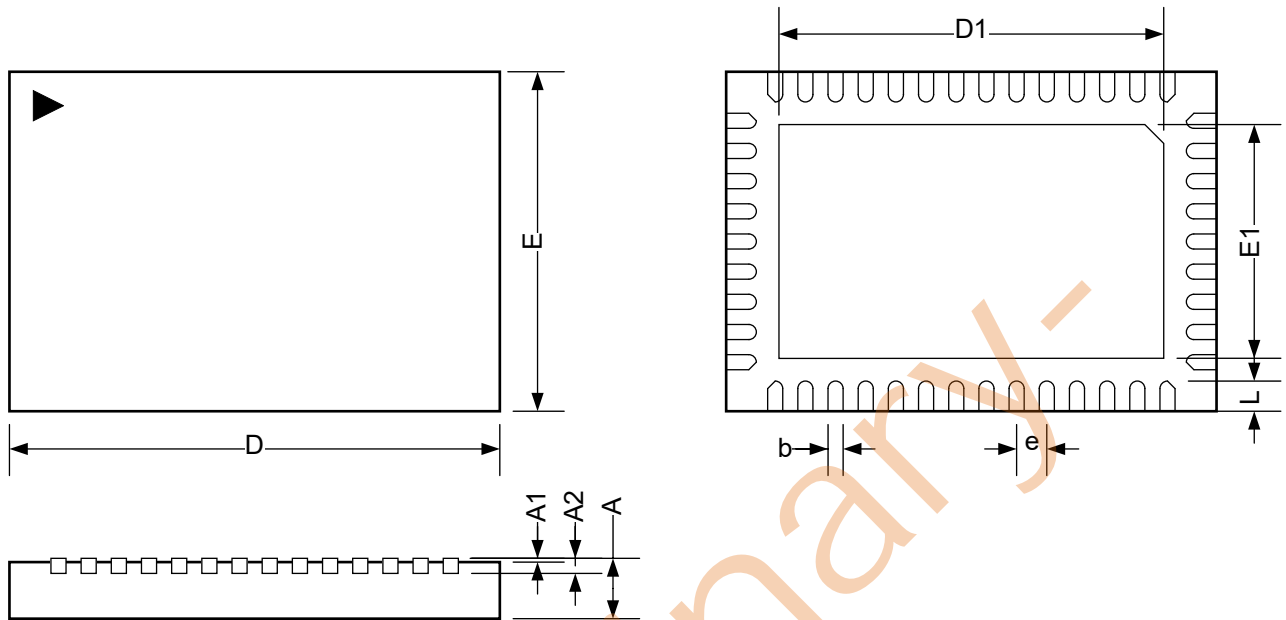
Group A: VBK

Group B: AVDD, HAVDD, VGH, VGL, VSS, GAMMA, VCOM1, VCOM2

Block	Protection	Work Condition	Action
VBK	OCP	2.0A	
	UVP	VBK<80%, after 50ms	IC Group A/B shut down,Latch Release IC restart
	SCP	VBK<20%	IC Group A/B shut down,Latch Release IC restart
	OVP	VBK>120%	LXBK stop switching, Release OVP-hysteresis
AVDD	OCP	5.0A	
	UVP	AVDD<85%, after 50ms	IC Group B shut down,Latch Release IC restart
	SCP1	AVDD<20%	IC Group B shut down,Latch Release IC restart
	SCP2	AVDD<VIN-0.15V	IC Group B shut down,Latch Release IC restart
	OVP	AVDD>21.8V	LX/CS stop switching, Release OVP-hysteresis
VGH	OCP	1.5A	
	UVP	VGH<80%, after 50ms	IC Group B shut down,Latch Release IC restart
	SCP	VGH<20%	IC Group B shut down,Latch Release IC restart
	OVP	VGH>44V	LXVGH stop switching, Release OVP-hysteresis
VGL	OCP	1.5A	
	UVP	VGL<80%, after 50ms	IC Group B shut down,Latch Release IC restart
	SCP	VGL<20%	IC Group B shut down,Latch Release IC restart
	OVP	VGL>120%	LXVGL stop switching, Release OVP-hysteresis
VSS	OCP	50mA	
	OVP	105%	VSS to GND source current path turn on
	UVP	VSS<80%, after 50ms	IC Group B shut down,Latch Release IC restart
HAVDD	SCP	±200mA	Current limit keep
VCOM1	SCP	±150mA	Current limit keep
VCOM2	SCP	±20mA	Current limit keep
GMA(14ch)	SCP	±50mA	Current limit keep
PMIC	OTP	IC temp > 150	IC Group A/B shut down,Latch

Packaging Information

QFN6.5X4.5-46



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	6.40	6.50	6.60	0.2520	0.2559	0.2598
E	4.40	4.50	4.60	0.1732	0.1772	0.1811
D1	5.00	5.10	5.20	0.1969	0.2008	0.2048
E1	3.00	3.10	3.20	0.1181	0.1220	0.1260
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177