Features

- Wide input voltage range: 4.2V – 16V
- Output voltage range: V_{ref} – 7V
- 5-A continues output current
- High efficiency operation
  - Integrated an 18-mΩ LS-MOSFET and an 30-mΩ HS-MOSFET
  - 93% efficiency at 5A load from 12V to 5V conversion
- Automatic PFM mode at light load
- ±1% Vref accuracy at 25ºC
- Typical 400-kHz switching frequency
- COT control scheme with fast load transient response
- Output discharge function integrated
- Cycle by cycle current limit and hiccup protection
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- 1.5ms typical soft-start time
- DFN2×2-6FC package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV and TV box
- 12V Industrial bus applications

General Description

The LP6455 is a synchronous buck converter supporting up to 5A output current. The LP6455 employs an adaptive constant-on-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP6455 supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP6455 integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP6455 also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), over-voltage protection (OVP)and short circuit protection (SCP).

The LP6455 is available in a small 6-pin DFN2×2-6FC package.

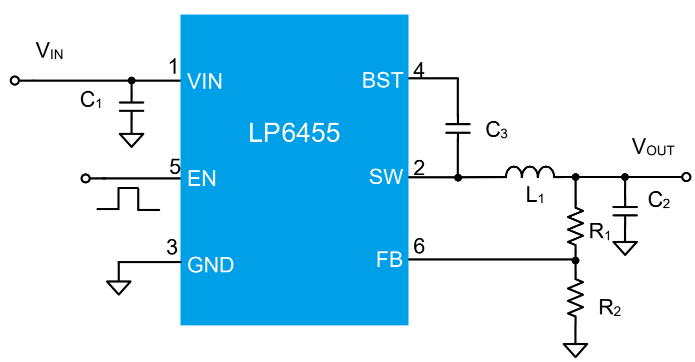
Order Information

LP6455 □□ □

F: Green/Pb-Free

Package Type
QV : DFN

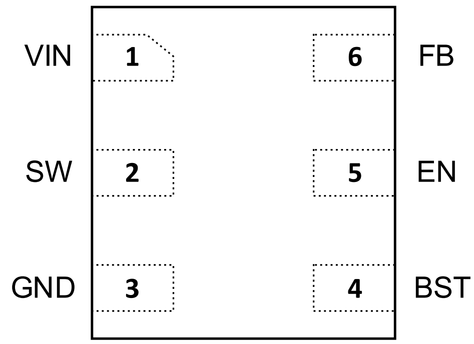
Typical Application Circuit



Device Information

Part Number	Top Marking	Vref	MODE	Frequency	Package	Shipping	MSL
LP6455QVF	TBD	0.6V	FPWM	400kHz	DFN2×2-6FC	3K/REEL	LEVEL-3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. MSL: Moisture Sensitivity Level according to JEDEC Standard.							

Pin Diagram



TOP View

Pin Description

Pin #	Name	Description
1	VIN	IC power supply input.
2	SW	The switching node of the converter.
3	GND	Power ground of the IC.
4	BST	Bootstrap pin. Power supply for high-side MOSFET gate driver. A 0.1-μF capacitor must be connected between this pin and SW pin.
5	EN	Enable input. This pin can be used to control the system power sequence as well.
6	FB	Feedback pin. Use a resistor divider to set the desired output voltage.

Absolute Maximum Ratings (Note)

VIN, SW, and EN to GND -- -0.3V to 18V
FB to GND -- -0.3V to 6.5V
BST to SW -- -0.3V to 6.5V
SW to GND （20ns transient） -- -3.5V to 18V
Junction Temperature Range (T_J)-- -40°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec) ---260℃

Note: Stresses beyond those listed under "AbsoluteMaximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditionsbeyond those indicated in the operational sections of the specifications is not implied. Exposure to absolutemaximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM(Human Body Model) -- 2kV
CDM (Charged-device Model) --- 500V

Thermal Information

θ_{JA}(Junction-to-Ambient Thermal Resistance, JESD51-7) --85℃/W
θ_{JC}(Junction-to-Case Thermal Resistance, JESD51-7) ---40℃/W
$\theta_{JA\_effective}$(Junction-to-Ambient Thermal Resistance, EVM, 2layer,1.6mm, 2oz copper) -----------------------------57℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.2		16	V
V_{OUT}	Output voltage	V_{ref}		7	V
L	Inductor	0.7		6.0	μH
T_A	Ambient temperature range	-40		105	°C
C_{IN}	Input decoupling capacitor	4.7		100	μF
C_{OUT}	Output capacitor	10		100	μF

Electrical Characteristics

(The specifications are measured under conditions V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_R}	Input under voltage lockout threshold	V_{IN} rising threshold		3.9	4.2	V
V_{ULVO_H}	UVLO hysteresis	V_{IN}falling threshold		0.15		V
V_{OVP_R}	Input over voltage protection threshold	V_{IN} rising threshold	16.5	17	17.5	V
V_{OVP_H}	OVP hysteresis	V_{IN}falling threshold		0.5		V
I_{q_VIN}	Input quiescent current	No switching, EN=3V, FB=1.0V		300	500	µA
I_{SD}	Shutdown current	EN=0V		1.2	5	µA
BUCK CONVERTER						
I_{LIM}	Low-side valley current limit		6.6	9.4		A
V_{ref}	Reference voltage	T_A=25°C	0.594	0.6	0.606	V
		T_A=-40~125°C	0.585		0.615	V
R_{dson_HS}	High-side FET on resistance	V_{IN}=12V		30		mΩ
R_{dson_LS}	Low-side FET on resistance	V_{IN}=12V		18		mΩ
R_{dis_FET}	SW discharge FET on resistance	V_{OUT}=1V, EN=0		150		Ω
F_{sw}	Switching frequency			400		kHz
$t_{on\text{-}min}$	Minimum on-time[1]			100		ns
$t_{off\text{-}min}$	Minimum off-time[1]	V_{FB}=V_{ref}- 0.2V		100		ns
D_{max}	Maximum duty cycle[1]	VIN=5.0V		97		%
$t_{on\text{-}hiccup}$	Hiccup on time[1]			3.2		ms
$t_{off\text{-}hiccup}$	Hiccup waiting time[1]			40		ms

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	EN delay time[1]	From EN high to first switching		250		us
t_{ss}	Soft-start time[1]	From first switching to 95%Vref		1.25		ms
I_{leak_FB}	FB pin leakage current			0.01	0.1	µA
FB UVP and OVP						
V_{UVP_fall}	UVP threshold	FB falling edge, reference to Vref	40	50	60	%
V_{UVP_rise}	UVP hysteresis	FB rising edge, reference to Vref		60		%
V_{OVP_rise}	OVP threshold	FB rising edge, reference to Vref	110	113	116	%
V_{OVP_fall}	OVP hysteresis	FB falling edge, reference to Vref		108		%
EN Logic						
V_H	EN pin logic high threshold	EN rising edge	1.15	1.2	1.25	V
V_{EN_hys}	EN pin threshold hysteresis	EN falling edge		0.1		V
R_{EN}	EN pin internal pull-down resistance			1100		kΩ
Thermal Protection						
T_{jsd}	Thermal shutdown threshold	Rising threshold		160		°C
	Thermal shutdown hysteresis	Falling threshold		135		°C

[1]: Not production tested. Guaranteed by design.

Typical Characteristics

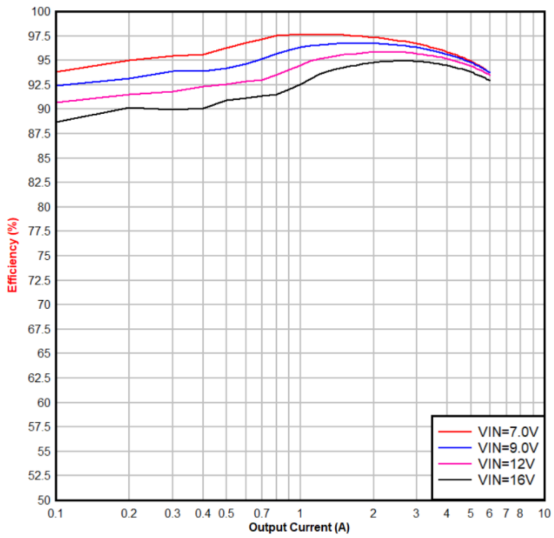


Figure 1.Efficiency, V_{OUT}=5V, L=4.7uH, DCR=25mΩ

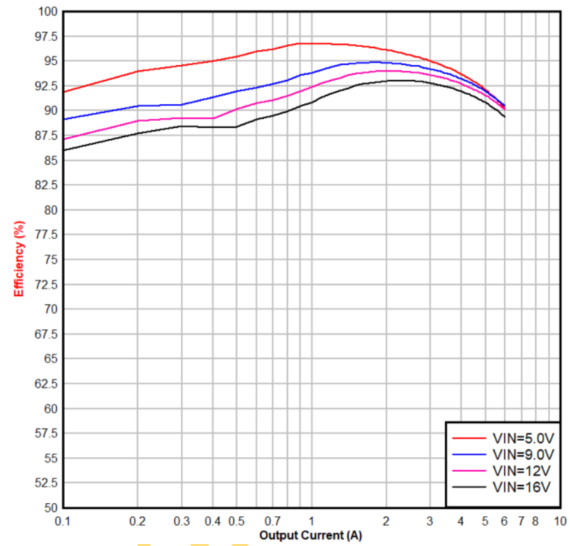


Figure 2. Efficiency, V_{OUT}=3.3V, L=2.2uH, DCR=15mΩ

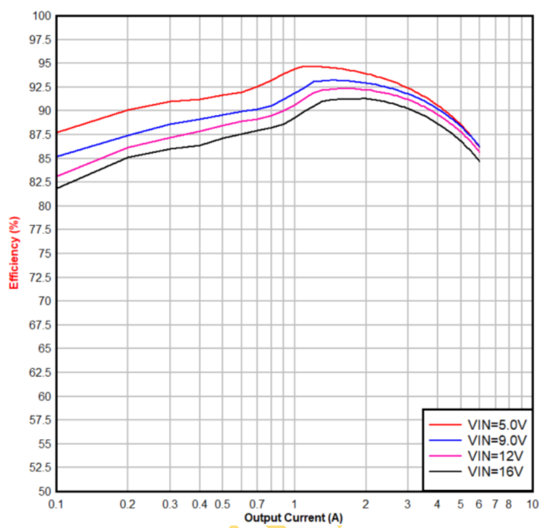


Figure 3.Efficiency, VOUT=1.8V, L=1uH, DCR=8mΩ

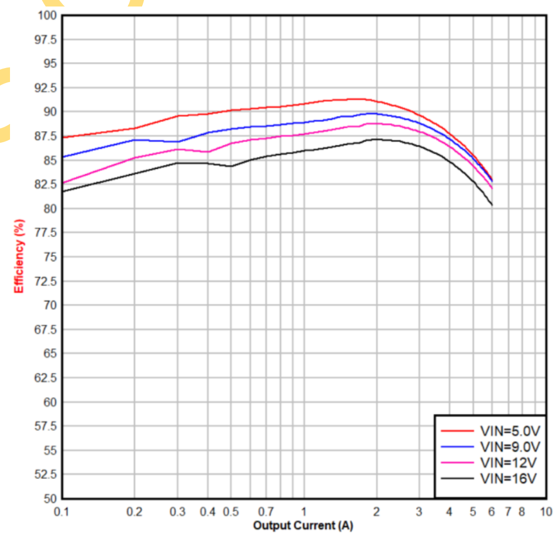


Figure 4.Efficiency, VOUT=1.2V, L=1uH, DCR=8mΩ

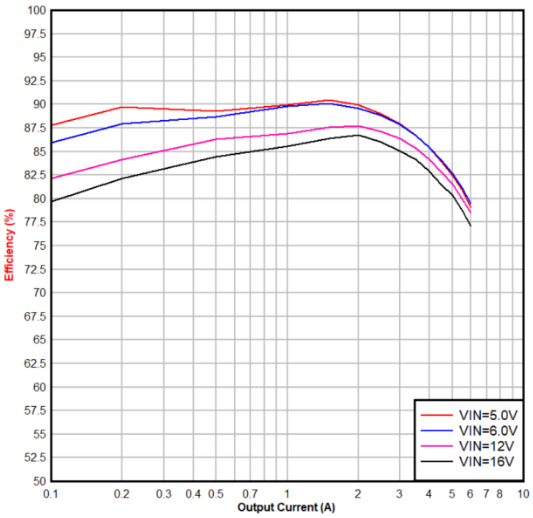


Figure 5.Efficiency, VOUT=1.05V, L=1.0uH, DCR=8mΩ

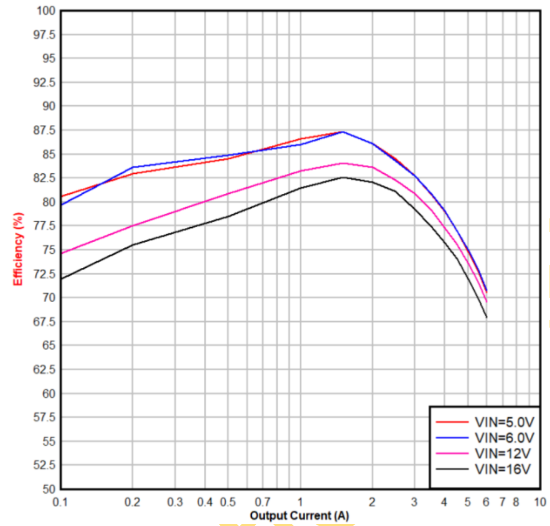


Figure 6.Efficiency, VOUT=0.6V, L=1uH, DCR=8mΩ

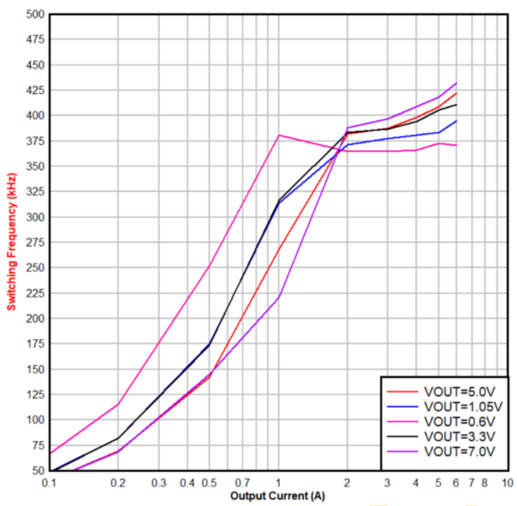


Figure 7. Switching Frequency VS. Output Current VIN=12.0V

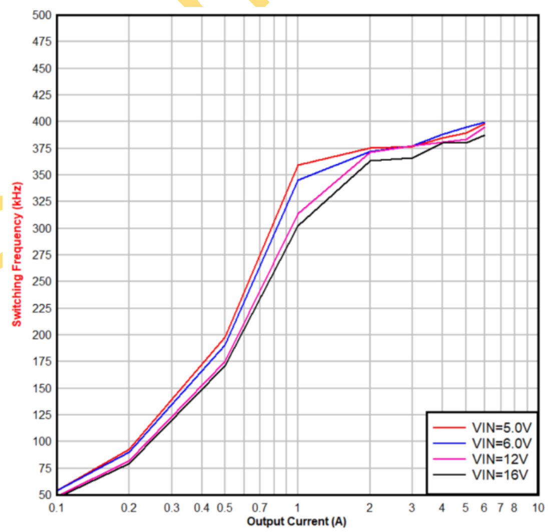


Figure 8. Switching Frequency VS. Output Current VOUT=1.05V

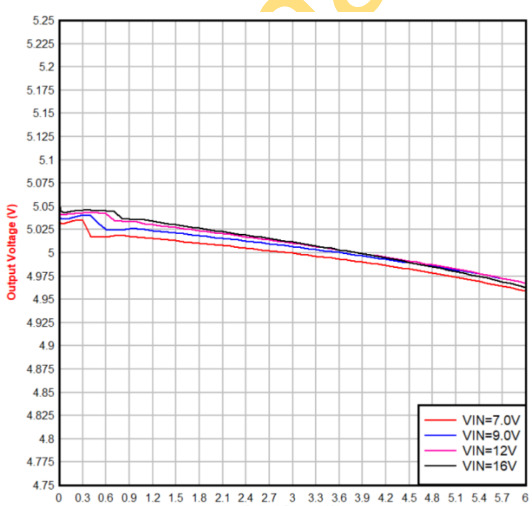


Figure 9. VOUT=5V, Regulation

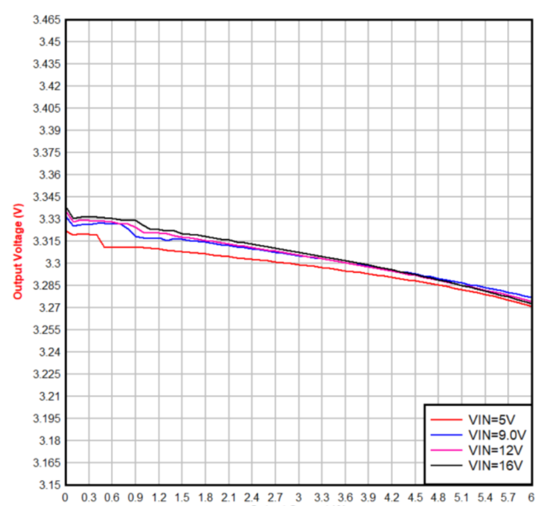


Figure 10. VOUT=3.3V, Regulation

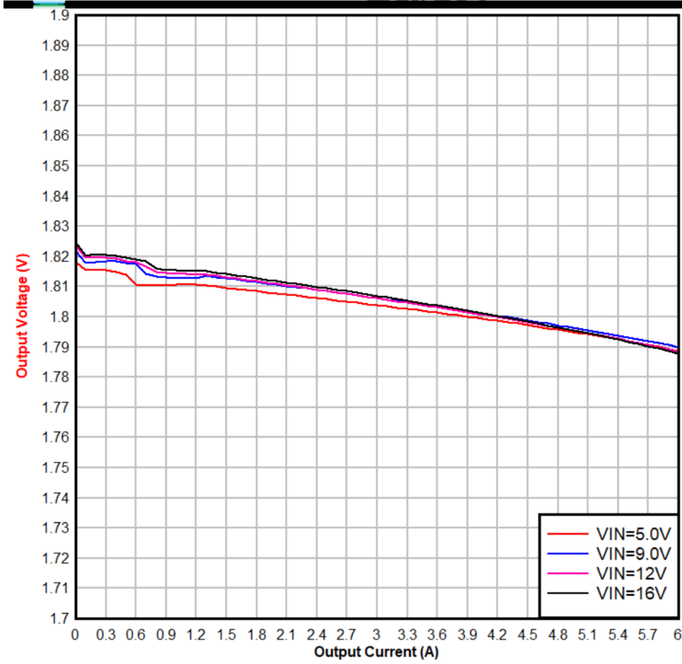


Figure 11. VOUT=1.8V, Regulation

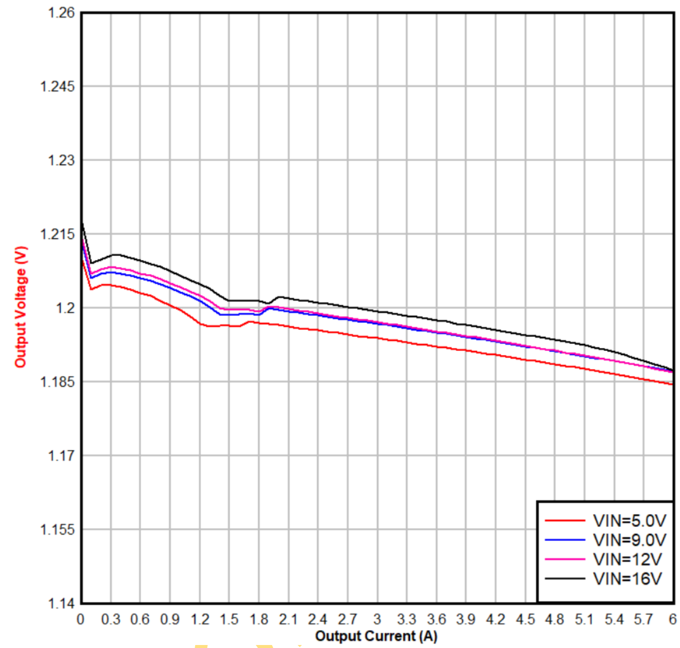


Figure 12. VOUT=1.2V, Regulation, L=1uH

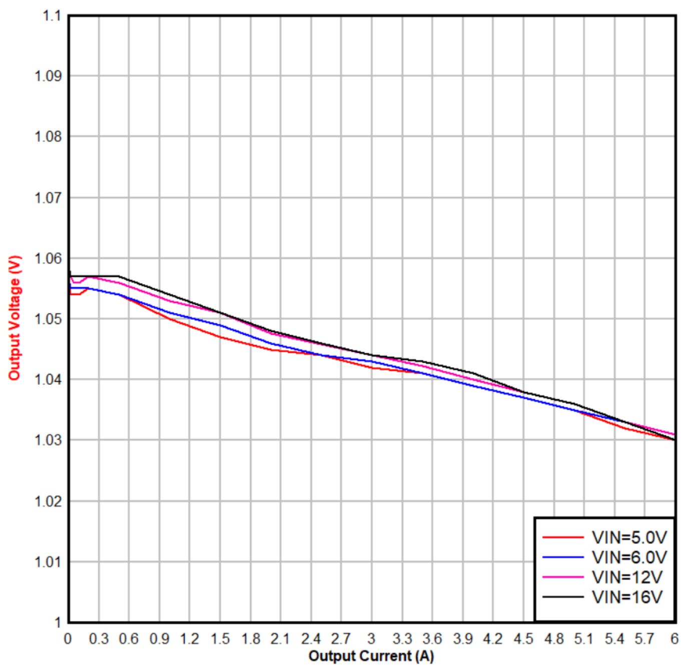


Figure 13. VOUT=1.05V, Regulation, L=1uH

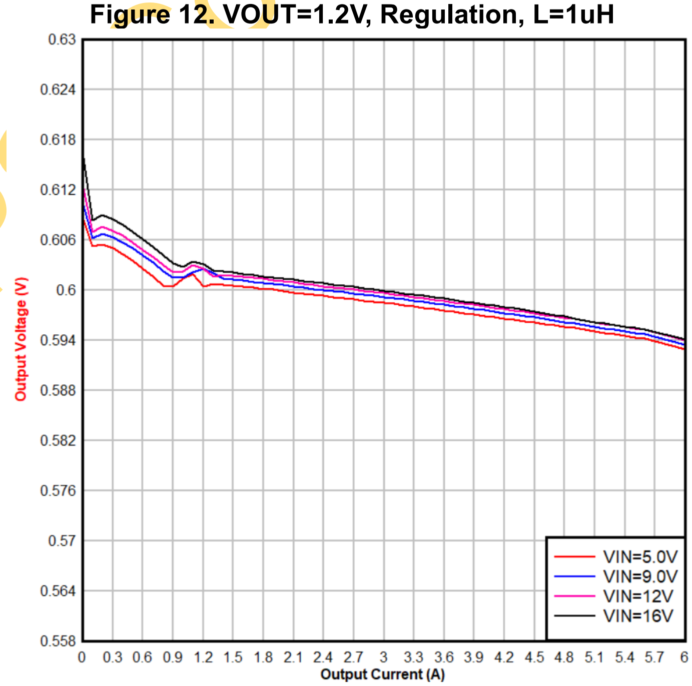


Figure 14. VOUT=0.6V, Regulation, L=1uH

Application Waveforms(VOUT=1.05V, L=1μH, COUT=22μF*3, 16V)

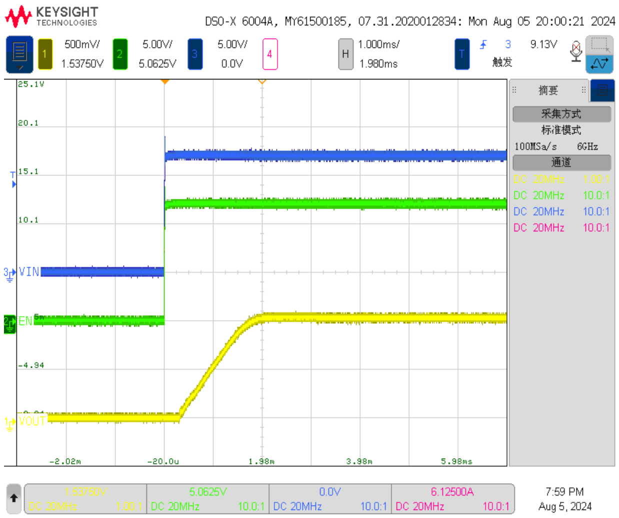


Figure 15. Startup by VIN, 0.2Ω load

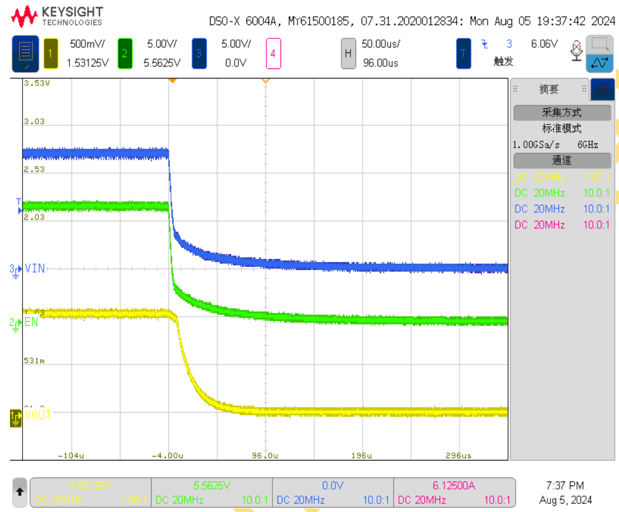


Figure 16. Shutdown by VIN, 0.2Ω load

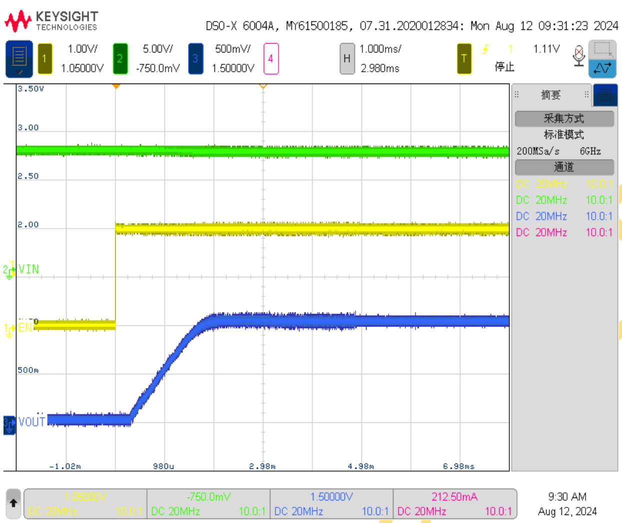


Figure 17. Startup by EN, 0.2Ω load

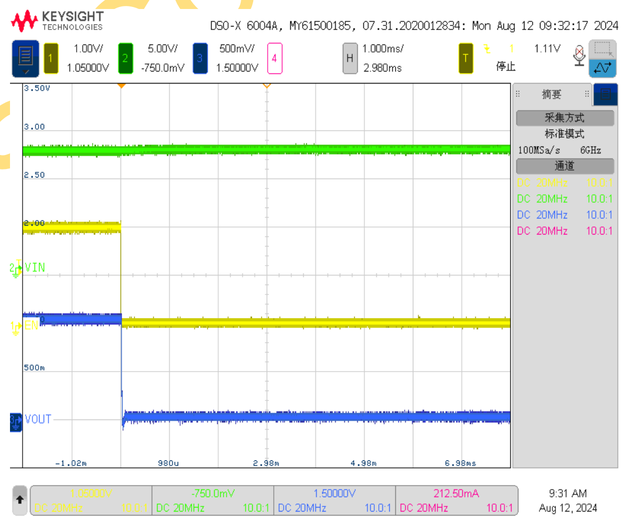
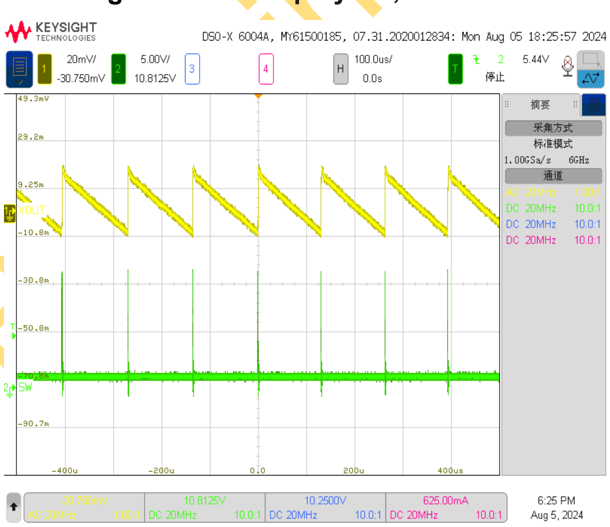


Figure 18. Shutdown by EN, 0.2Ω load



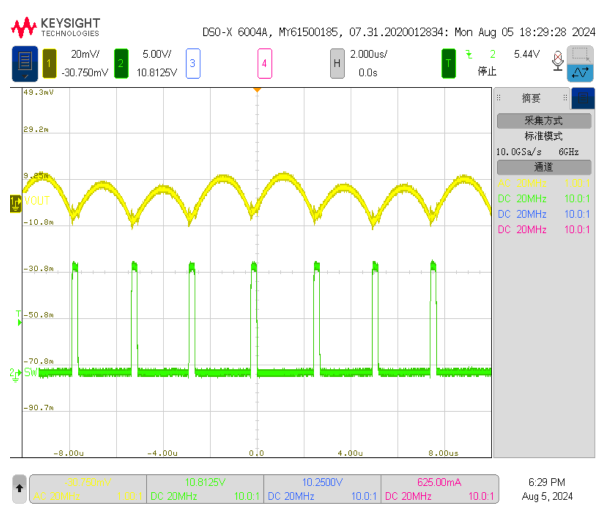
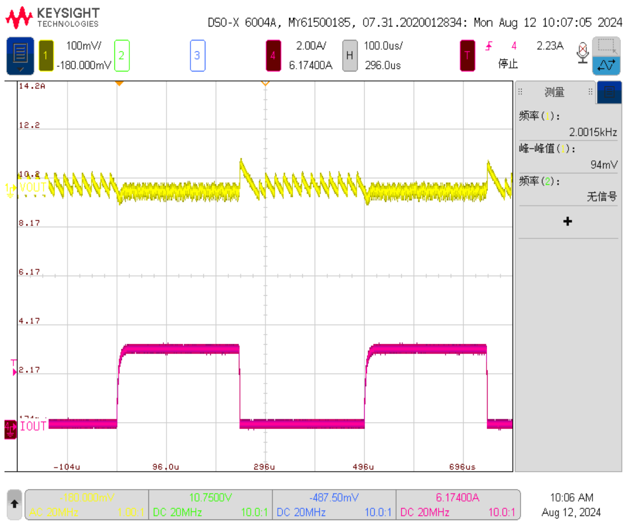


Figure 19. Switching Waveform, 10mA load

Figure 20. Switching Waveform, 6A load



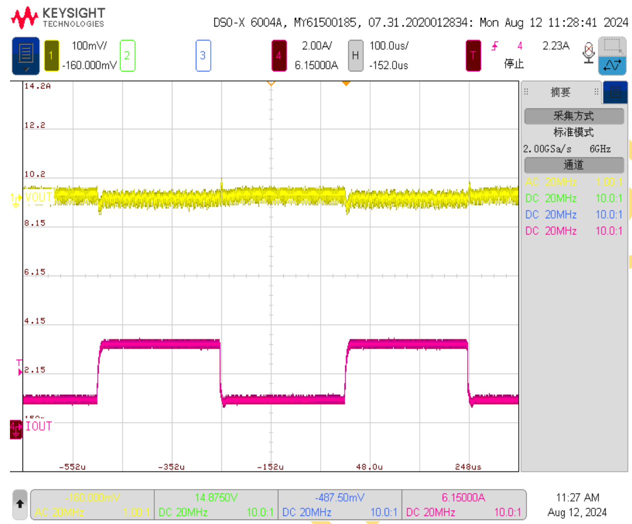
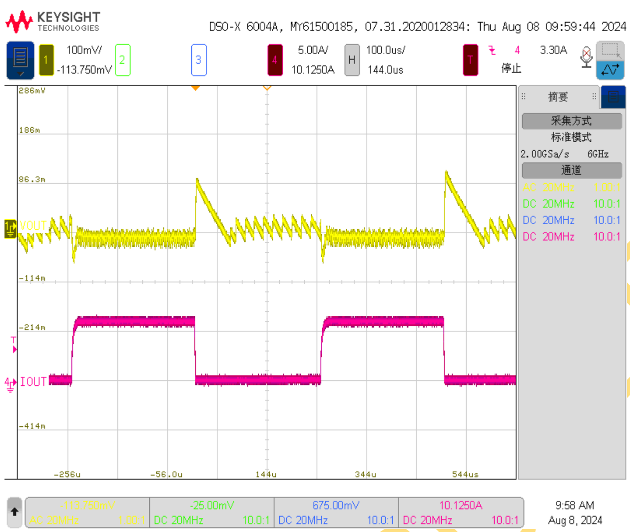


Figure 21. Load Transient, 0.1A-3A-0.1A

Figure 22. Load Transient, 1A-3A-1A



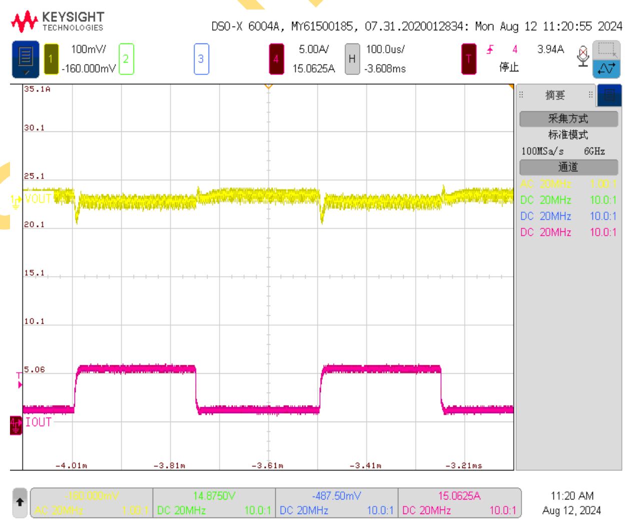
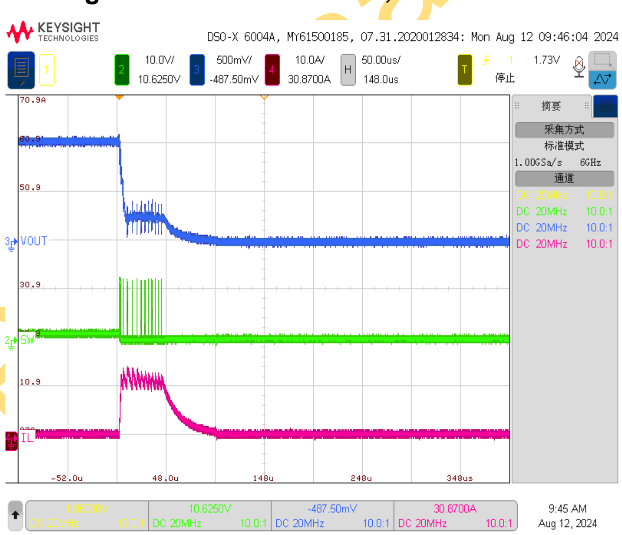


Figure 23. Load Transient, 0.1A-6A-0.1A

Figure 24. Load Transient, 1A-6A-1A



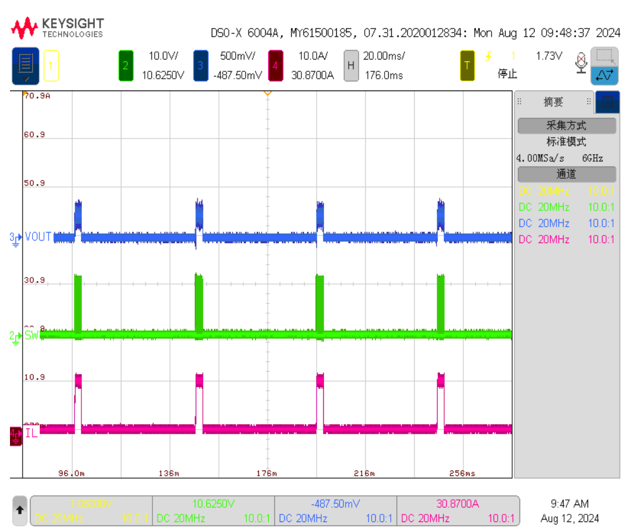
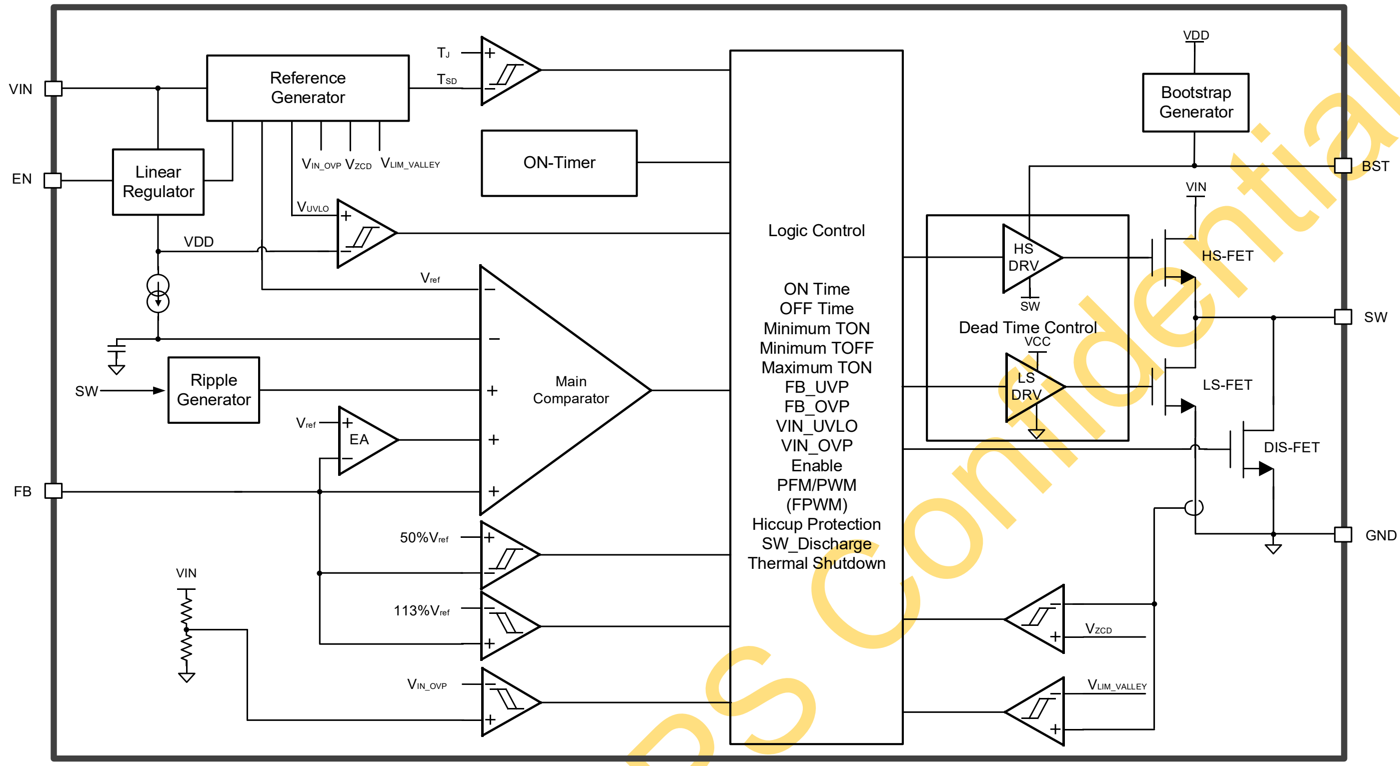


Figure 25. Output Hard Short

Figure 26. Hiccup Protection

Functional Block Diagram



Detailed Description

Overview

The LP6455 is a 5A synchronous buck converter, supporting 4.2-16V input voltage range. The adaptive COT control scheme enables fast transient respond and minimizes the output capacitance. The LP6455 supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP6455 automatically transfers between PFM and PWM according to the output current.

Under Voltage Lockout and Over Voltage Protection

When the input voltage VIN is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP6455 can be enabled by the EN pin.

When the input voltage VIN is higher than the VIN_OVP threshold, all functions are shut down as well. When the input voltage is lower than the UVLO rising threshold, the LP6455recovers to normal operation. The input voltage OVP is not active when EN is low and this protection is non-latch.

EN Control

The EN pin can be used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP6455 enables all the internal circuits, delays for 250us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1100kΩpull-down resistor to ground.

Soft-start

The LP6455 integrates soft-start function with a typical time of 1.25ms（t_{ss}）. After passing the UVLO threshold and enabled by the EN pin with the 250us delay(t_d), the internal reference voltage ramps from zero to the Vref in 1.25-ms and the output voltage ramps up accordingly.

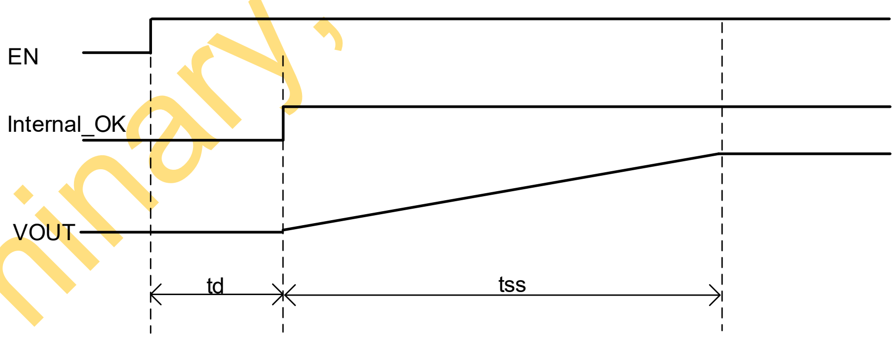


Figure 27.Soft Start Sequence

Constant-ON Time (COT) Control Scheme

The LP6455 integrates the COT control scheme for pseudo-fixed- frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal on-time (TON) generator block monitors the FB-pin voltage and turns on the high-side MOSFET to start a switching cycle, when the FB-pin voltage drops to an internal reference voltage Vref. Then the internal circuits start to calculate the on-time of the high-side MOSFET, which is proportional to the input voltage and inversely proportional to the output voltage. Once the on-time is finished, the TOFF generator turns off the high-side MOSFET and turns on the low-side MOSFET.

PFM Operation

The LP6455 is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

FPWM Operation (LP6455F)

The LP6455F is designed to work at FPWM to maintain the good regulation and transient performance. When the output decreases, the inductor is allowed to flow from the output to the ground plane. In this way, the switching frequency is kept the same even without load.

The negative current limit is -3A typically.

The FPWM operation mode reduced the output ripple under light load at the cost of lower light load efficiency.

Output Active discharge function

The LP6455 sinks current from the SW pin when the device is shutdown by EN, input UVLO/OVP or output OVP. An internal 150Ω on-resistance FET is turned on and the energy from the output capacitor is discharged to the ground under these states. The VIN power supply should remain present for the output discharge function to be active.

Table 1. Output Discharge Logic Table

Condition	Description	Output discharge
EN=Low	VIN>=1.5V	YES
EN=High	VIN<V_{IN_UVLO}	NO
EN=High	1.5<VIN<V_{IN_UVLO}	YES
EN=High	VIN>=V_{IN_UVLO}	NO
VIN OVP	EN=High and VIN> V_{IN_OVP}	NO
VIN low	VIN<1.5	NO
FB OVP	FB>=113%Vref	YES
FB Power Good	FB is in the range of 50%~113%Vref	NO
FB UVP	FB< 50%Vref	NO
Thermal Shutdown		YES

Bootstrap Capacitor

The LP6455 integrates two N-MOSFET to achieve high efficiency. The high-side MOSFET is powered by the bootstrap capacitor CBST, which is between the BST pin and SW pin.

Over Current Protection and Short Circuit Protection

The LP6455 protects an over current situation by limiting the inductor valley current. The current of low-side MOSFET is monitored all the time to sense the inductor valley current when the LP6455 is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit pluses a half of the inductor ripple current.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to FB UVP threshold for 1.5-ms, the LP6455 shuts down. The LP6455 will restart after a typical 40-ms hiccup waiting time. If the SCP condition still holds after soft-start, the LP6455 shutdown again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

Thermal Protection

The LP6455 has a thermal protection function. The device will shut down when the internal temperature is higher than 160°C and will restart after the temperature drops below 135°C.

Application Information

Design Requirements

The table 2 shows the design parameters for a typical 1.05V output voltage in the TV application.

Table 2 Design Parameters

Parameter	Target
Input voltage range	9~15V
Output voltage	1.05V
Transient ripple	±50mV
Operating frequency	400kHz

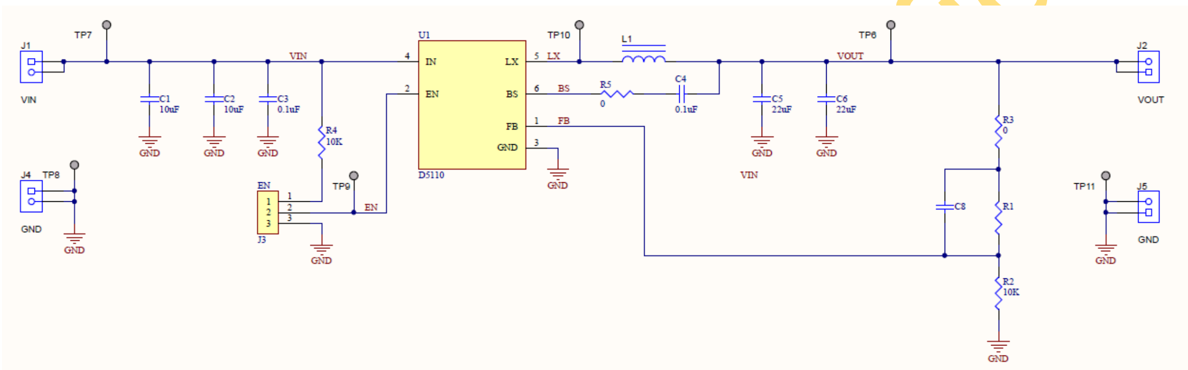


Figure 28. Typical schematic

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1\right) * V_{ref}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V for LP6455.
For better accuracy, the R_{DOWN} is recommended to be not higher than 10kΩto ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current.
For a 1.05V-output application, a 10kΩ$R_2$is selected and the R_1 is 7.5kΩ.

EN Design

The LP6455 allows the user to design a precise VIN voltage to enable the converter during power on. The startup sequence can be designed by adjusting the resistor divider of R_{UP_EN} and R_{DOWN_EN} with the equation below,

$$V_{EN} = \frac{1100k\Omega // R_{DOWN\_EN}}{R_{UP\_EN} + 1100k\Omega // R_{DOWN\_EN}} * VIN$$

where V_{EN} is the EN rising threshold voltage at which the converter is enabled, which is 1.2V typically.A 47pF-1nF capacitor is recommend to be soldered in parallel with the $R_{EN_DOWN}$to avoid the high-frequency noise influence from the switching node.

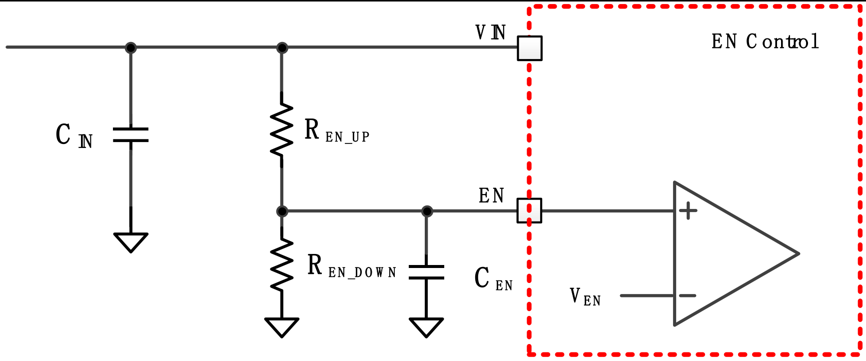


Figure 29. EN connection

Inductor and Output Capacitor Setting

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * Fsw} * \frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.
For a typical 12V input voltage and 1.05V output voltage, a low DCR value,1-μH inductor is recommended.
The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feed-forward capacitor C_8 can be selected to improve the transient behavior. The typical capacitance can be 10-100pF. For this design, 16V, X5R, 22μFcapacitors (GRM21BR61C226ME44) from Murata are soldered at the VOUT to GND.Multiple capacitors should be soldered to keep the system stable because of the voltage rating effect.

Table 1Recommend R/L/C values

Vout	Inductor-L	Minimum Cout	Typical Cout	R_1	R_2	Feedforward C_8
1.05V	1μH	22μF*2	22μF*3	7.5 kΩ	10 kΩ	10-100pF
3.3V	2.2μH	22μF*2	22μF*3	45 kΩ	10 kΩ	10-100pF
5.0V	4.7μH	22μF*2	22μF*3	73.3 kΩ	10 kΩ	10-100pF

Bootstrap capacitor

A 0.1-μF ceramic capacitor is needed to supply power for the high-side N-MOSFET driver. The capacitor should be at least 10V.

Input capacitor

A typical 22-μF ceramic capacitor is needed to serve as the bulk capacitor at the VIN pin. An additional 0.1μF is strongly recommended to provide additional high frequency filtering and should be placed to the VIN pin and GND as close as possible.

PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor (C_3)as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

- R_5 is reserved to slow down the switching speed for noise sensitive applications and R_3 with higher than 1kΩ resistor should be soldered if the feedforward capacitor is soldered at the same time.