LP78511

36V/1.2A Linear Charger& 2-Discharging Channel

Features

Easy-to-use standalone single-cell charger:

- High input voltage linear charger
  - Support up to 6.3V operating input voltage with 36V absolute maximum input rating
  - Programmable up to 1200mA fast charge current
  - ±0.5% regulated output voltage accuracy
  - Termination current 10% of fast charge current
- High integration
  - Integrated reverse blocking MOSFET
  - Built-in charge current sensing
  - Internal loop compensation
  - Integrated charge and power status indication
- Support full charge cycle of trickle current mode, constant current (CC) mode, constant voltage (CV) mode, charge termination and automatic recharge
- Protection features
  - Input under-voltage lockout (UVLO)
  - Input over-voltage protection (OVP)
  - Thermal regulation

2-Discharging Channel:

- Integrated 30mΩ R_{ON} NMOS of each channel
- Built-in charge pump without external capacitor
- OCP protection
- OTP protection and auto-recovery
- Load detection
- BAT leakage current <1μA typical
- RoHS Compliant and 100% Lead (Pb)-Free
- Package: DFN3x3-10

Applications

- Wireless Speaker
- Cordless Power Tools
- Gaming Devices
- Portable Media Players
- Handheld Battery-Powered Devices
- E-Cigarettes
- Power Bank

General Description

The LP78511 is an SoC with a highly advanced linear charger and 2-diacharging channel applied for single cell Li-Ion and Li-Polymer batteries. The device is ideally suited for portable applications due to DFN3x3-10 package and low number of external components required.

The device employs a full charge algorithm with trickle current, constant current (CC), constant voltage (CV) modes, charge termination and automatic recharge. The device supports charge current up to 1200mA, programmed by an external resistor. The device can withstand an input voltage up to 36V, which can protect the charger from the accidental insertion of a high voltage supply or a hot insertion.

The 2-discharging channel integrates ultra-low on-resistance (30mΩ typical) NMOS of each channel and built-in charge pump without external capacitor, which is suited for power battery applications. Without an input supply, the battery leakage current is less than 1μA typical.

The device provides various safety features for battery charging, including input under voltage lockout (UVLO), input over-voltage protection (OVP), charging thermal regulation protection that is implemented by reducing the charge current when the junction temperature reaches 140℃. The device provides OTP and OCP protection for discharging channel.

The LP78511 is available in a DFN3x3-10 package.

Order Information

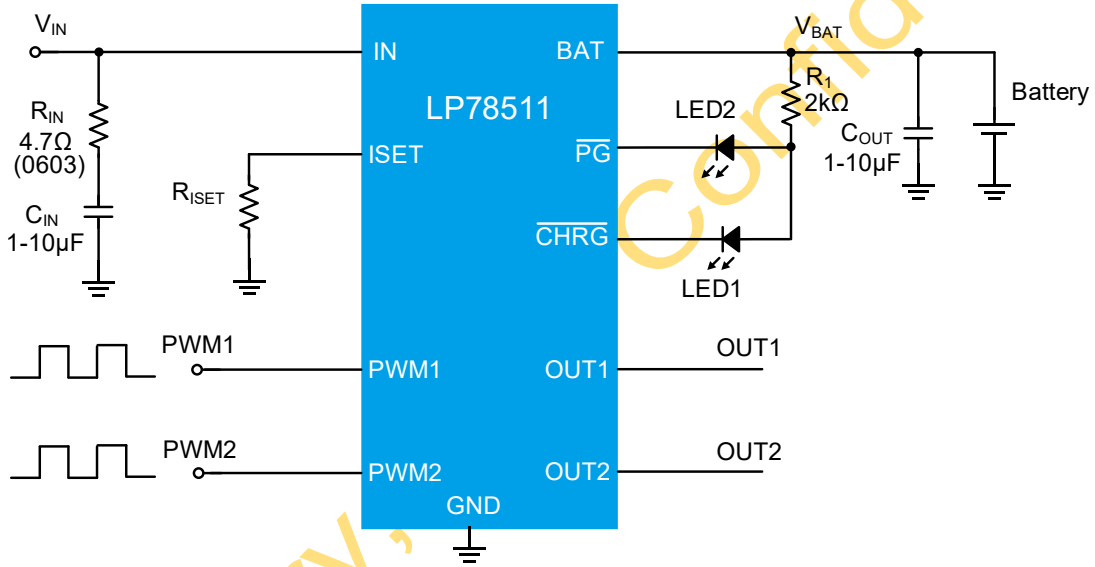
LP78511 □□ □-□□□

- Float Voltage
  Default:4.20V
  435:4.35V
  44:4.40V
- F: Pb-Free
- Package Type
  QV: DFN3x3-10

Device Information

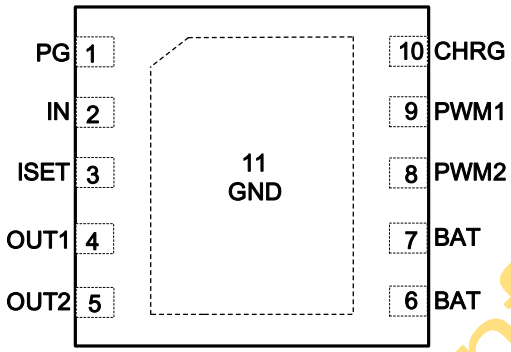
Part Number	Top Marking	Battery Voltage	Moisture Sensitivity Level	Package	Shipping
LP78511QVF	LPS LP78511 YWX	4.20V	MSL3	DFN3x3-10	5K/REEL
Marking indication: Y: Production year. W: Production week. X: Series number.					

Typical Application Circuit



Pin Diagram

DFN3x3-10 (Top View)



Pin Description

Pin DFN3x3-10	Name	Description
1	PG	Open Drain Input status output. when VIN is above UVLO thresholds and lower than OVP threshold, PG pin is pulled down by an internal NMOS. Otherwise PG pin is Hi-Z.
2	IN	Positive Supply Voltage Input. Place a 4.7Ω resistor and a 1-10μF ceramic capacitor in series from IN to GND and place the components as close as possible to the chip.
3	ISET	Fast Charge Current Program Pin. Connect this pin with an external resistor R_{ISET} to GND to program the fast charge current.
4	OUT1	Channel1 Output Pin.
5	OUT2	Channel2 Output Pin.
6,7	BAT	Battery Pin. Connect to the battery, A ceramic capacitor is needed typically.
8	PWM2	Channel2 PWM Input Pin.
9	PWM1	Channel1 PWM Input Pin.
10	CHRG	Open Drain Input status output. the device is in charging state, CHRG pin is pulled down by internal NMOS. when the charging cycle is completed, CHRG pin is Hi-Z.
11	GND	Ground reference for the device that is also the thermal pad used to conduct heat from the device.

Absolute Maximum Ratings (1)

IN to GND ---------- -0.3V to 36V
BAT, OUT1, OUT2 to GND ---------- -0.3V to 6.5V
ISET, CHRG, PG, PWM1, PWM2 to GND ---------- -0.3V to 6.5V
BAT Surge Voltage ---------- 20V
Maximum Junction Temperature (T_J) ---------- 150℃
Storage Temperature Range ---------- -65℃ to 125℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

HBM (Human Body Model) ---------- 2kV
MM (Machine Model) ---------- 200V

Recommended Operating Conditions

Input Voltage ---------- 4.5V to 6V
Maximum Charge Current ---------- 1200mA
PWMx frequency ---------- 100Hz~30kHz
Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = 5V, unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input voltage range		4.5	5	6	V
I_{SB}	Input standby current	Standby mode (Charge terminated)		115		μA
V_{IN_UVLO}	Input under voltage lockout	V_{IN} rising	3.75	3.9	4.05	V
$V_{IN\_UVLO\_HYS}$	V_{UVLO} hysteresis	V_{IN} falling		200		mV
V_{OVP}	Over-voltage protection threshold voltage	V_{IN} rising	6.15	6.3	6.45	V
V_{OVP_HYS}	OVP hysteresis	V_{IN} falling		150		mV
BATTERY CHARGE						
V_{FLOAT}	Regulated output voltage		4.179	4.2	4.221	V
I_{CC}	Fast charge current	R_{ISET}=3.4kΩ, constant current mode	450	500	550	mA
		R_{ISET}=17kΩ, constant current mode	90	100	110	mA
I_{TERM}	Termination current threshold	R_{ISET}=3.4kΩ, constant voltage mode		10%		I_{CC}
I_{TRIKL}	Trickle charge current	V_{BAT}<V_{TRIKL}		80		mA
V_{TRIKL}	Trickle charge threshold voltage	V_{BAT} rising	2.75	2.9	3.05	V
V_{TRIKL_HYS}	Trickle charge hysteresis voltage	V_{BAT} falling		200		mV
ΔV_{RECHRG}	Battery recharge voltage difference threshold	V_{BAT} falling	100	150	200	mV
V_{HR}	V_{IN}-V_{BAT} headroom threshold voltage	V_{BAT}=4.0V, V_{IN} rising	100	130	160	mV
V_{HR_HYS}	V_{HR} Hysteresis	V_{BAT}=4.0V, V_{IN} falling		80		mV
T_{J_LIMIT}	Junction temperature limit	Thermal foldback protection state		140		℃
R_{ON}	IN-BAT MOSFET on-resistance	Charge current=500mA		700		mΩ
V_{ISET_CC}	ISET pin voltage	Constant current mode		1		V
STAT (CHRG, PG) PIN						
V_{STAT_L}	CHRG/PG pin output low voltage	I_{SINK}=5mA			0.5	V
I_{STAT_SINK}	CHRG/PG pin sink current				5	mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
DISCHARGE CHANNEL						
R_{ON}	On resistance of each channel MOS	PWM_x=H, V_{BAT}=3.6V, R_{OUTx}=1Ω		30		mΩ
I_{OCP}	OCP threshold of each channel			12		A
t_{OCP}	OCP trigger deglitch time			10		μs
t_{OCPR}	OCP release time of PWM low			80		ms
t_{CHRGR}	The time from both PWMx low to charging recovery			80		ms
I_{OUT_PU}	OUTx pull-up current at PWMx is low	PWMx =L, V_{BAT}=3.6V		500		nA
t_{RISE_OUT}	OUTx rise time	V_{BAT}=3.6V, R_{LOAD}=1Ω		300		ns
t_{FALL_OUT}	OUTx fall time	V_{BAT}=3.6V, R_{LOAD}=1Ω		300		ns
t_{PD}	Propagation delay from PWMx to OUTx	V_{BAT}=3.6V, R_{LOAD}=1Ω			1	μs
V_{BAT_UVP}	BAT UVP rising threshold	V_{BAT} rising	2.5	2.6	2.7	V
	BAT UVP falling threshold	V_{BAT} falling	2.2	2.3	2.4	V
t_{BAT_UVP}	BAT UVP deglitch time			50		μs
T_{OTP}	OTP threshold			160		℃
T_{OTP_HYS}	OTP threshold hysteresis			30		℃
V_{PWM_H}	PWM logic-high voltage Threshold	PWM rising	1.4			V
V_{PWM_L}	PWM logic-low voltage threshold	PWM falling			0.4	V
BAT PIN						
I_{BAT_LKG}	Battery leakage current with OUT floating	V_{IN} floating, OUTx floating, V_{BAT}=4.2V, PWMx =low		0.5	1	μA
	Battery leakage current with OUT load	V_{IN} floating, OUTx 1Ω load, V_{BAT}=4.2V, PWMx =low		1.5		μA
V_{BAT_SG}	BAT surge	IEC61000-4-5		20		V
V_{BAT_CLP}	BAT Clamp	IEC61000-4-5, I_{BAT} = 7A		6.5		V

Typical Characteristics

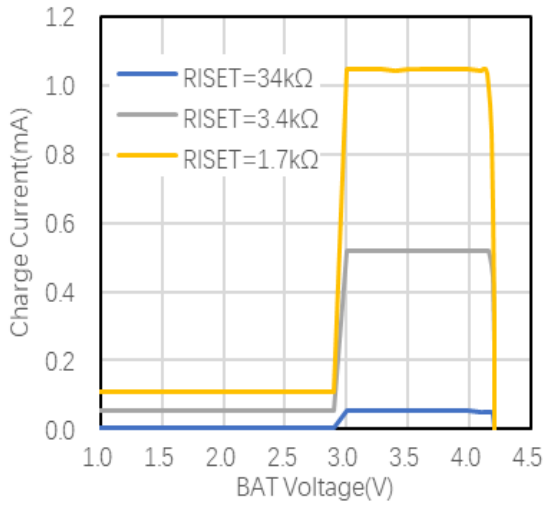


Figure 1. Charge Current vs BAT Voltage
V_{IN}=5V, 25℃

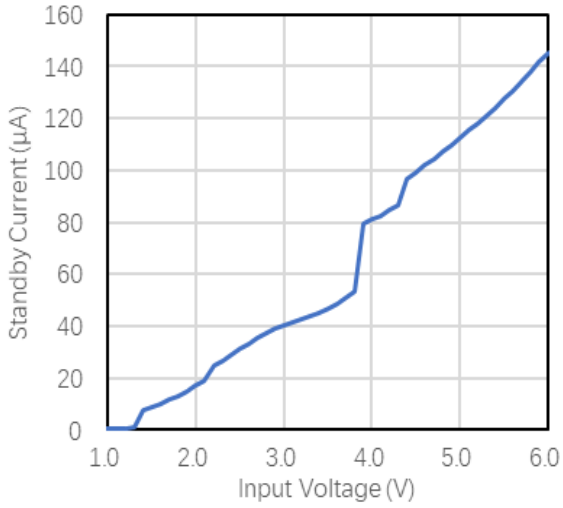
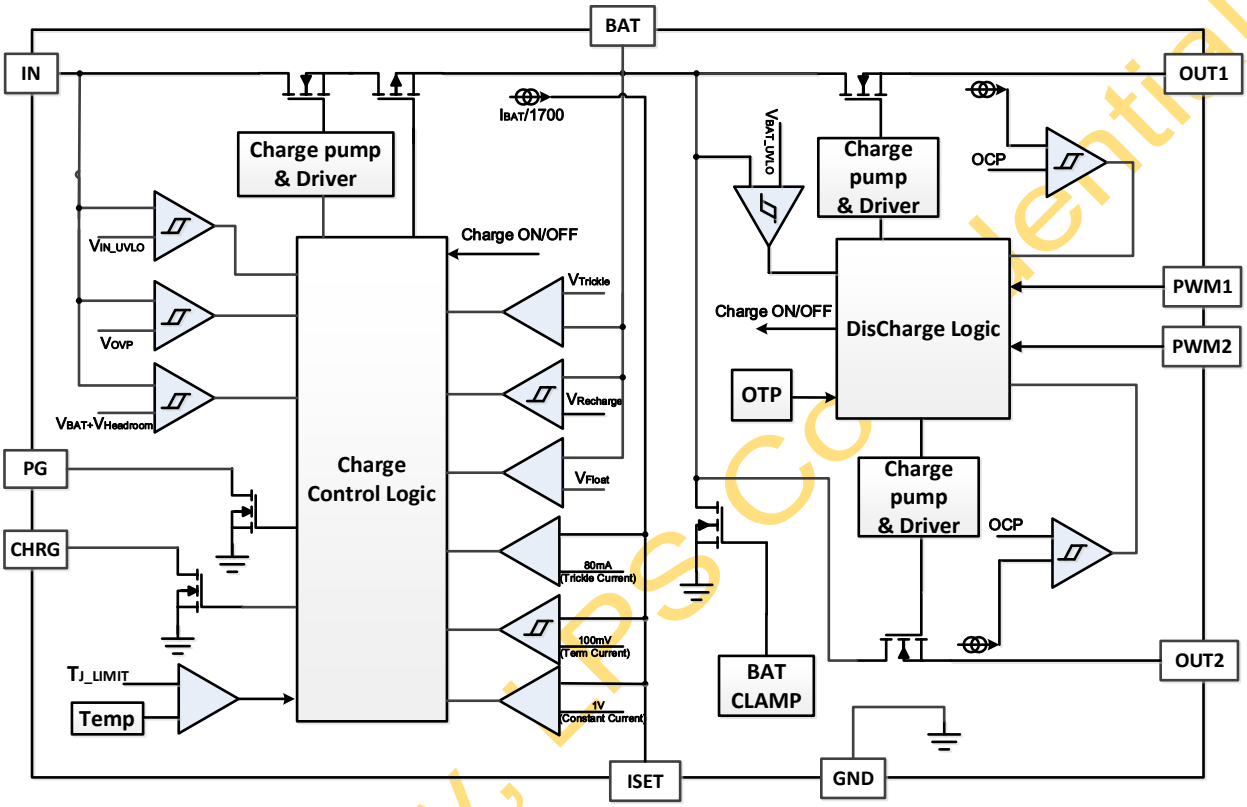


Figure 2. Input Standby current vs Input Voltage
Charge terminated, 25℃

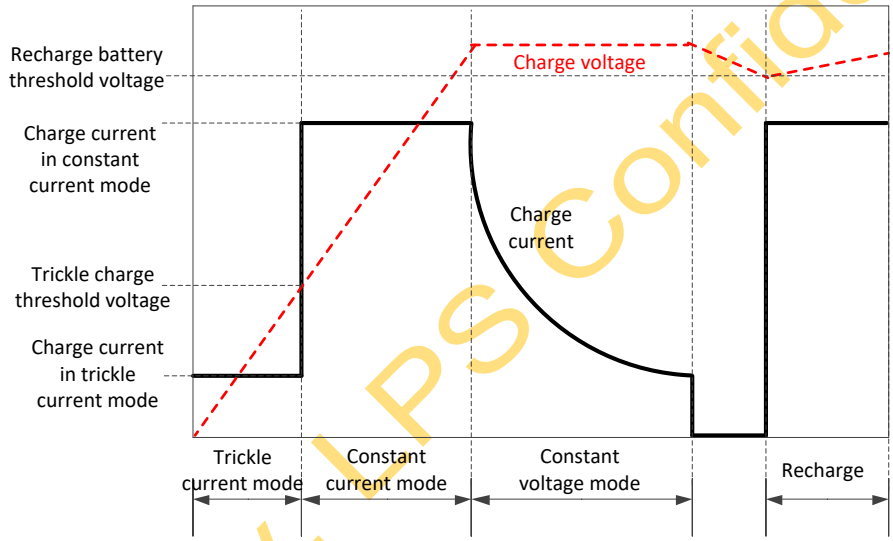
Functional Block Diagram



Detailed Description

Charging Section

The LP78511 is built-in highly advanced linear charger with up to 1200mA maximum charge current for single cell Li-Ion and Li-Polymer batteries. The device charges the battery with full charge cycle: trickle current mode, constant current mode (CC), constant voltage mode (CV), charge termination and recharge. The typical charge profile can be showed as the figure below.



When the battery voltage is lower than Trickle charge threshold voltage (V_{TRIKL}, 2.9V typical), the device charges in the trickle current mode, the charge current will be set to Trickle charge current (I_{TRIKL}), which is fixed 80mA(typical) to bring the battery voltage up to a safe level for full current charging. When the battery voltage rises to V_{TRIKL}, the device enters the constant current mode, where the charge current is Fast charge current(I_{CC}). When the battery voltage approaches the Regulated output voltage (V_{FLOAT}), the device goes to constant voltage mode, the charge current starts to decrease. When the charge current is lower than the Termination current threshold (I_{TERM}), which is 10%I_{CC}, the device will terminate the charging.

The device will automatically recharge the battery while the battery voltage drops ΔV_{RECHRG} (150mV, typical) from the Regulated output voltage (V_{FLOAT}).

ISET Programming Fast Charge Current

The Fast charge current (I_{CC}) is set by a resistor (R_{ISET}) connecting from the ISET pin to GND. The relationship between I_{CC} and the programming resistance is established by the following formula:

$$I_{CC} = \frac{V_{ISET} \times 1700}{R_{ISET}}$$

where V_{ISET}=1V typical.

Charge Termination and Automatic Recharge

A charge cycle will be terminated when the charge current falls to I_{TERM} (10%I_{CC}, typical), as the battery voltage reached V_{FLOAT}. The function is implemented by monitoring the ISET pin voltage and comparing to a 100mV threshold voltage. When the ISET pin voltage falls below 100mV for longer than 1ms typically, the charging will be

terminated.

Once the charge cycle is terminated, the LP78511 continuously monitors the voltage on the BAT pin by a comparator. A new charge cycle starts when the battery voltage drops by a voltage difference ΔV_{RECHRG} (150mV, typical) from V_{FLOAT}, which means the battery level drops to approximately 80% to 90% capacity. This ensures that the battery always keeps at or near a fully charged condition.

Undervoltage Lockout (UVLO) and Minimum Headroom Voltage

An internal UVLO circuit monitors the input voltage and keeps the device in Shutdown mode until the input supply rises above the UVLO threshold. The UVLO circuitry has a built-in hysteresis of 200 mV. The UVLO circuit always be active.

In addition, the input supply must be V_{HR} (130mV, typical) higher than the battery voltage before the LP78511 become operational. Whenever the input supply is below the UVLO threshold or lower than a voltage of V_{HR} above the VBAT pin, the LP78511 is in Shutdown mode.

Charge Status Indicator (CHRG&PG)

When the input voltage is above the V_{UVLO} and above the voltage of $V_{BAT}+V_{HR}$, but lower than V_{OVP} ($V_{IN}<V_{OVP}$), PG pin will be pulled down by an internal NMOS, otherwise, PG is on high impedance state. When the LP78511 is in a charge cycle, CHRG pin will be pulled down by an internal NMOS. After the charge current decreased to I_{TERM} in CV mode and then charging terminated, the CHRG pin will become high impedance.

Function	Function	PG	CHRG
$V_{UVLO}<V_{IN}<V_{OVP}$ &$V_{IN}>V_{BAT}+V_{HR}$	Charging	Low	Low
	Charge Terminated	Low	Hi-Z
Others		Hi-Z	Hi-Z

Thermal Regulation Foldback

An internal thermal regulation foldback loop reduces charge current if the junction temperature reaches a preset value of approximately 140℃ to prevent further temperature rise. This function protects the device from excessive temperature and allows the user to get the limits of the power handling capability of a given circuit board without the risk of damaging the device. The charge current can be set according to typical ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.

Charge termination function will not be active when thermal foldback regulation protection is happening.

Discharging Section

The LP78511 integrates two independent discharge channels, each of the channel is turned on and off by the internal ultra-low on-resistance (30mΩ typical) NMOSFET. And each of the MOSFET can be controlled by the logic of the corresponding PWM input signal. And an internal charge pump for each channel is integrated to drive the built-in NMOS without external capacitors.

Discharge Control Logic

When PWM1/2 is high, the corresponding channel NMOS is turned on; when PWM1/2 is low, the corresponding OUT channel is turned off.

When any one of the PWM is high and the corresponding channel is turned on, charging module will be disabled immediately. Charging can only be resumed when both PWM1 and PWM2 are low for 80ms continuously.

Discharging Over-Current Protection

Each channel's discharging current is sensed continuously and compared with the over-current protection threshold independently. When the discharging current of each channel reaches the threshold and lasts for 3us, the corresponding channel will be turned off, and the other channel is not affected. After being turned off, the subsequent PWM waveforms of this channel are ignored. When the PWM waveform of this channel remains low for 80ms, the next high-level PWM input can control this channel on/off normally. If OCP occurs again, the channel will be turned off again.

OTP Protection

When the chip temperature reaches 160℃, the chip turns off the output and no longer responds to PWM input. When the temperature drops to 130℃, the chip resumes normal logic. This OTP does not affect the charging part's logic.

BAT UVP

When the BAT voltage is lower than the UVP falling threshold voltage, the chip turns off the output and no longer responds to PWM input. When the BAT voltage is higher than the UVP rising threshold voltage, the chip resumes normal discharge logic.

Low Power Mode

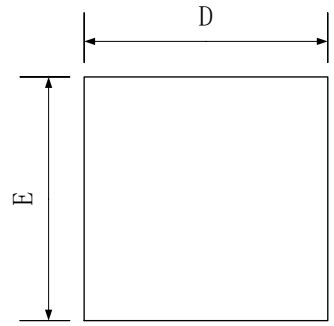
When both PWM1 and PWM2 are keep low for 80ms continuously, the chip enters low power mode, and the BAT current consumption is only 0.6μA typical.

Load Detection

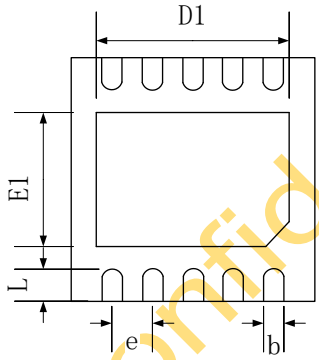
The chip integrates load detection function. Each channel's OUT terminal is integrated a 500nA pull-up current source. When the OUT terminal is not connected to a load, it will be pulled up to the BAT voltage. When a load is connected, the voltage at the OUT terminal will be pulled down.

Packaging Information

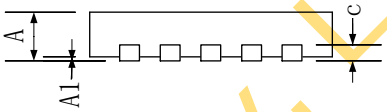
DFN3x3-10



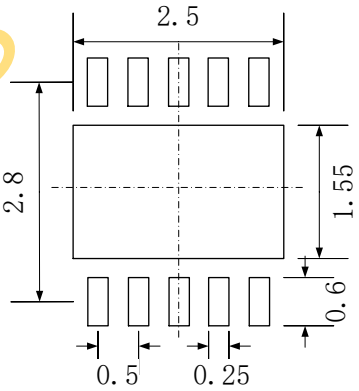
TOP VIEW



BOTTOM VIEW



SIDE VIEW



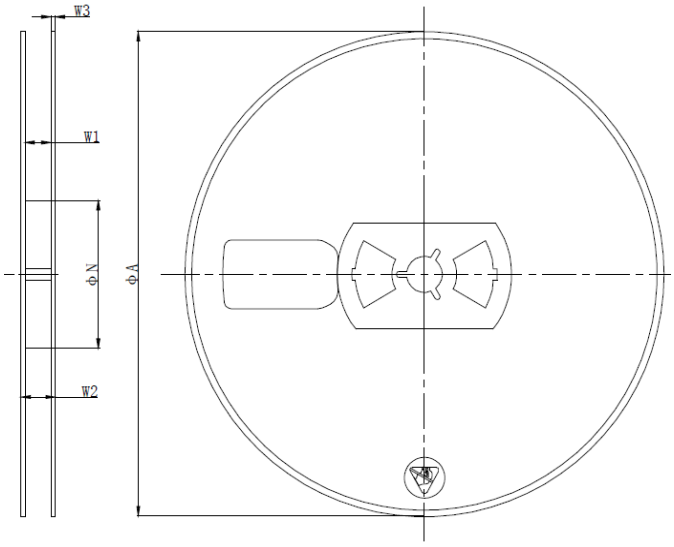
Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C		0.20 REF	
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
e		0.50 BSC	
L	0.30	0.40	0.50

Tape and Reel Information

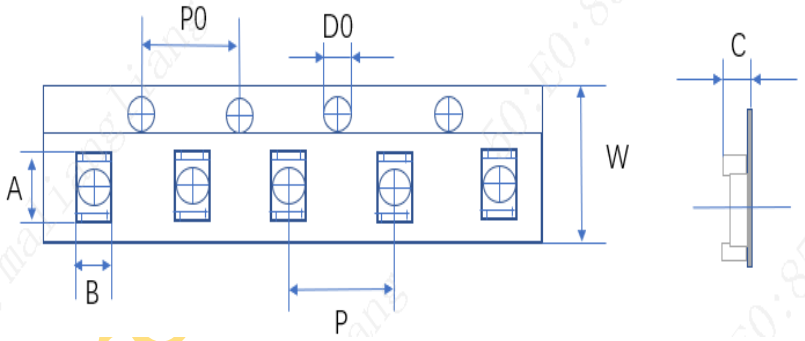
DFN3x3-10

REEL DIMENSIONS



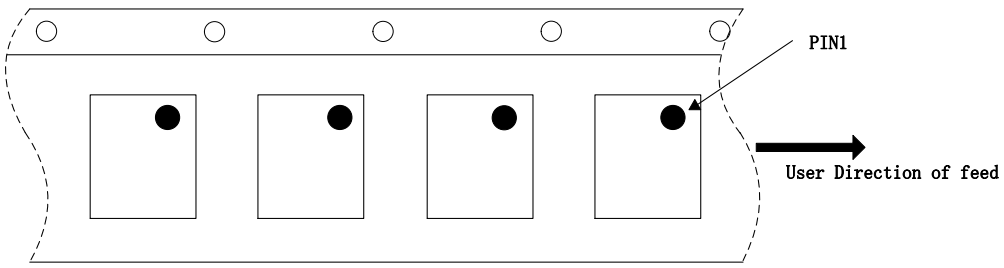
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	327.00	329.00	331.00
W2	14.40	16.40	18.40

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.10	3.40	3.70
B	3.10	3.40	3.70
P0	3.90	4.00	4.10
P	7.90	8.00	8.10
D0	1.45	1.55	1.65
W	11.70	12.00	12.30
C	0.95	1.10	1.25

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

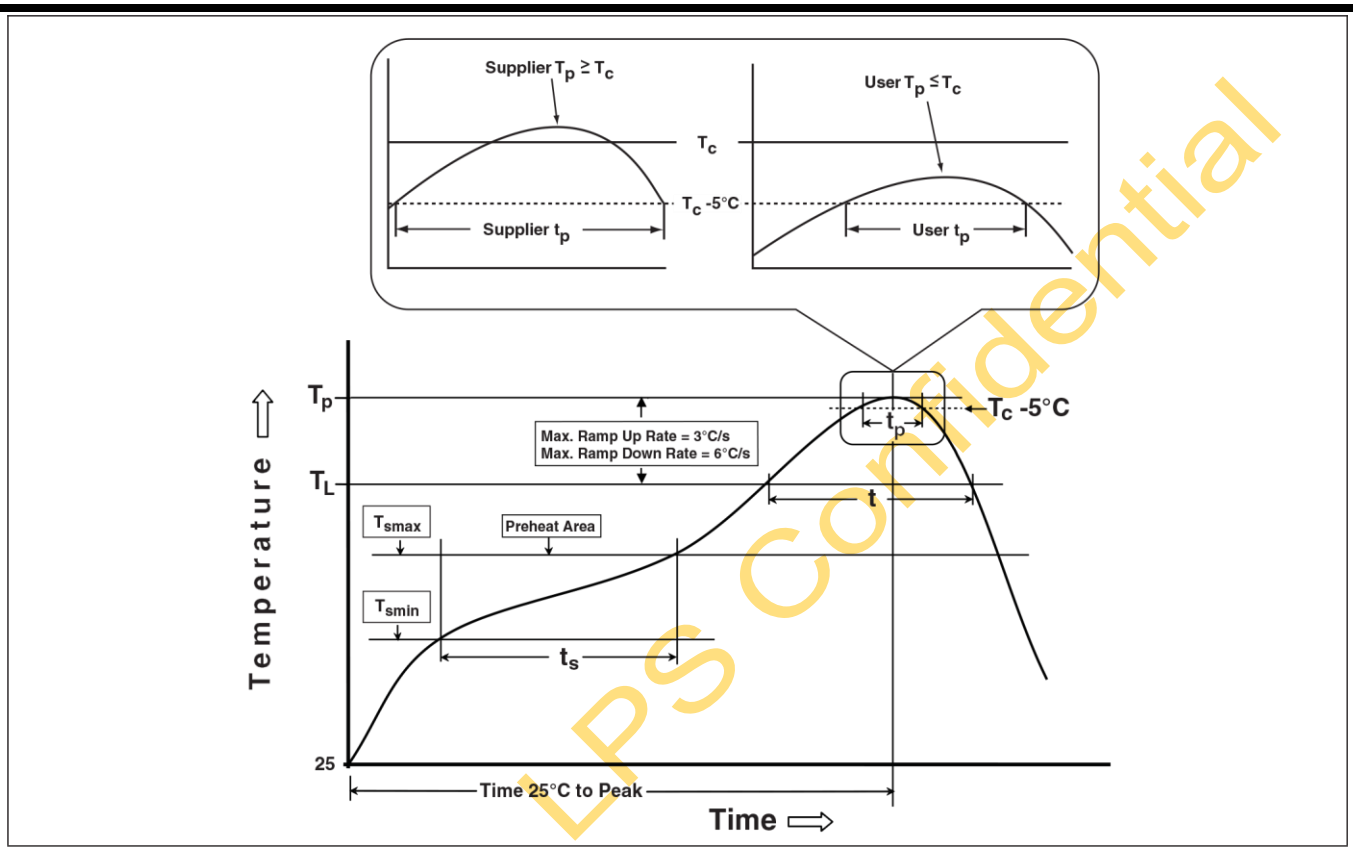


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;