LP3998

Dual Input Ultra Low Dropout LDO

Features

- Wide IN Voltage Range: 0.8V to 5.5V
- Bias Voltage Range: 2.4V to 5.5V
- Adjustable Output Voltage: 0.8V to 3.6V
- Fixed Output Voltage: 0.8, 0.9, 1.0, 1.05, 1.2, 1.25, 1.3, 1.5, 1.8, 2.5, 2.8, 3.0, 3.3V, 3.6V
- Maximum Load Current Up to 500mA
- High PSRR:
  - 76dB@1kHz, V_{IN} to V_{OUT}
  - 70dB@1kHz, V_{BIAS} to V_{OUT}
- Low Quiescent Current: 65μA typical
- Low Noise: 45μV_{RMS}@V_{OUT}=1.2V
- Low Dropout Voltage:
  - 85mV @ 500mA Load, V_{OUT}=1.2V, V_{IN} to V_{OUT}
  - 1050mV @ 500mA Load, V_{OUT}=1.2V, V_{BIAS} to V_{OUT}
- Output Voltage Accuracy: ±2% @ 1mA typical
- Thermal Shutdown Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.005%/V typical
- Load Regulation: 2mV typical
- Robust ESD capability:
  - Human Body Model: 4kV
  - Charged Device Model: 2kV
- Package: DFN1.2x1.2-6
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Digital cameras
- Audio devices
- Set-top Box
- Portable and battery-powered equipment
- Post regulation

Order Information

LP3998-□□ □□ □

- F: Pb Free
- Package Type
  - QV: DFN1.2x1.2-6
- OUT Voltage
  - A: Adjustable
  - 12: 1.2V
  - 15: 1.5V
  - 18: 1.8V
  - 25: 2.5V
  - 28: 2.8V
  - 30: 3.0V
  - 33: 3.3V

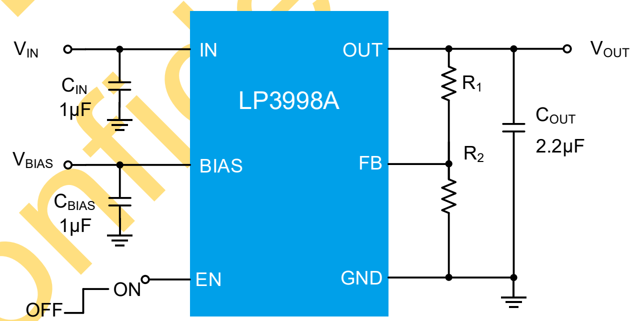
General Description

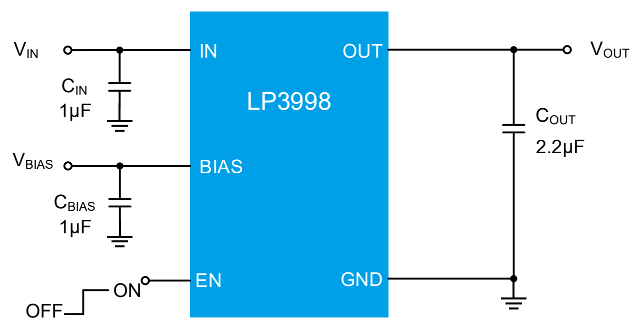
The LP3998 family are dual input high performance ultra-low dropout （LDO） voltage regulators with high PSRR, fast transient response, and high accuracy. The devices with advanced CMOS process are suitable for many applications that require regulated supplies of up to 500mA load current.

The LP3998 family include standard fixed voltage of 0.8V to 3.6V and adjustable output voltages of 0.8V to 5.0V with an external resister divider. The devices are stable with an effective 1.0μF capacitance ceramic output capacitor. The devices are protected from short circuit by a current limit function and from over-heating by a thermal overload protection.

The devices are available in a DFN1.2x1.2-6 package.

Typical Application Circuit

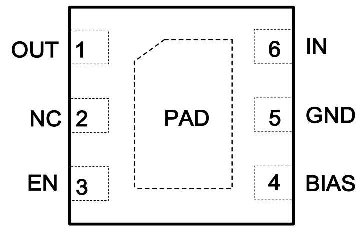




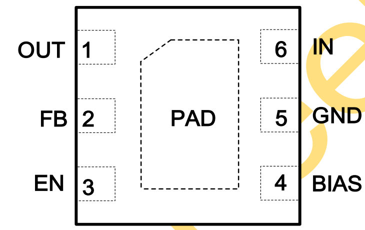
Device Information

Part Number	Top Marking	OUT Voltage	Moisture Sensitivity Level	Package	Shipping
LP3998AQVF	AWX	Adjustable	MSL3	DFN1.2x1.2-6	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

Pin Diagram



DFN1.2x1.2-6（top view）



DFN1.2x1.2-6（top view）

Pin Description

Pin	Name	Description
DFN1.2x1.2-6		
1	OUT	Output pin. Bypass with a minimum effective 1.0µF or greater capacitance ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.
2	NC/FB	No connection. / Feedback pin. Adjustable version only. This is used to set the output voltage. The reference voltage is 0.8V.
3	EN	Enable pin. Active high. Driving EN over 1V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode.
4	BIAS	Bias voltage supply for Internal control circuits. This pin is monitored by internal under-voltage lockout circuit.
5	GND	Ground.
6	IN	Supply input pin. Must be closely decoupled to GND with 1µF or greater ceramic capacitor. Place the capacitor as close as to the pin as possible.

Absolute Maximum Ratings (Note 1)

IN, BIAS Pin to GND -- -0.3~6.5V
OUT, EN, FB Pin to GND -- -0.3~V_{IN}
Maximum Junction Temperature (T_J) -- 150℃
Maximum Soldering Temperature (at leads, 10 sec) -- 260℃
Storage Temperature Range(T_{STG}) -- -65℃~125℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

HBM (Human Body Model) -- 4kV
CDM (Charged Device Model) -- 2kV

Recommended Operating Conditions

Input Voltage -- 0.8 V to 5.5V
BIAS Voltage -- 2.5 V to 5.5V
EN Voltage -- 0 V to 5.5V
Operating Junction Temperature Range (T_J) --40℃ to 125℃
Ambient Temperature Range -- -40℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃, V_{BIAS}=Max($V_{OUT(NOM)}$)+1.6V, 2.7V), V_{IN} = $V_{OUT(NOM)}$+0.3V, I_{OUT}=1mA, R_1=25.5kΩ, R_2=51kΩ, C_{IN}=1μF ,C_{OUT}=2.2μF, C_{BIAS}=0.1μF, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Operation Range		$V_{OUT(NOM)}+V_{DROP\_IN}$		5.5	V
V_{BIAS}	BIAS Operation Voltage Range		Max(($V_{OUT(NOM)}$+1.4), 2.5)		5.5	V
I_{Q_IN}	DC Supply Quiescent Current	V_{EN}=V_{IN}, I_{LOAD}=0mA		0.4		μA
I_{Q_BIAS}	BIAS Quiescent Current	V_{BIAS}=3.3V, V_{EN}=1.5V		65		μA
I_{SD_IN}	IN Shutdown Current	V_{EN}=0V		0.03	0.1	μA
I_{SD_BIAS}	BIAS Shutdown Current	V_{EN}=0V		0.3	1	μA
OUTPUT VOLTAGE AND CURRENT						
V_{OUT_ACC}	Output Voltage Accuracy		-2%		2%	
V_{FB}	FB Voltage		0.784	0.8	0.816	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	VIN Line Regulation	V_{IN}=$V_{OUT(NOM)}$+0.3V~5.5V		0.005		%/V
$\frac{\Delta V_{OUT}}{\Delta V_{BIAS} \times V_{OUT}}$	BIAS Line Regulation	V_{BIAS}=Max($V_{OUT(NOM)}$+1.6V, 2.7V)~5.5V		0.005		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{OUT} from 1mA to 500mA		2	20	mV
I_{OUT_MAX}	Max Load Current	V_{EN}=V_{IN}	500			mA
I_{LIMIT}	Load Current Limit	V_{OUT}=0.9*$V_{OUT(Nom)}$	500	650		mA
I_{SHORT}	Short Current Limit	V_{OUT} short to GND		280		mA
V_{DROP_IN}	VIN Dropout Voltage	I_{OUT}=100mA		17		mV
		I_{OUT}=500mA		85		mV
V_{DROP_BIAS}	BIAS Dropout Voltage	I_{OUT}=500mA		1050		mV
e_N	Output Noise	V_{IN}=$V_{OUT(NOM)}$+0.5V, V_{BIAS}=Max($V_{OUT(NOM)}$+1.6V 10Hz to 100kHz, V_{OUT}=1.2V,		45		$μV_{RMS}$
$PSRR_{IN}$	VIN Power Supply Rejection Ratio	V_{IN}=($V_{OUT(NOM)}$+1V)$_{DC}$+0.2V_{P-P}, V_{OUT}=1.2V, f=1kHz; I_{OUT}=20 mA,		76		dB
		I_{OUT}=150 mA		73		dB
$PSRR_{BIAS}$	BIAS Power Supply Rejection Ratio	V_{BIAS}=($V_{OUT(NOM)}$+1.6V)$_{DC}$+0.2V_{P-P}, V_{OUT}=1.2V, f=1kHz; I_{OUT}=20 mA		70		dB
		I_{OUT}=150 mA		70		dB
R_{DIS}	Auto-Discharge Resistance			120		Ω

THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			160		℃
T_{SD_HYS}	Thermal Shutdown Hysteresis			20		℃
EN LOGIC						
V_{ENH}	EN Logic High Voltage		1.0			V
V_{ENL}	EN Logic Low Voltage				0.4	V
I_{EN}	EN Input Current	VEN=0 to 5.5V		120		nA

Typical Characteristics

(T_J = 25℃, V_{IN} = V_{EN} =1.5V, R_1=25.5kΩ, R_2=51kΩ, V_{BIAS} = 2.7V, C_{IN} = C_{BIAS} = 1.0μF, C_{OUT}=2.2μF, unless otherwise noted.)

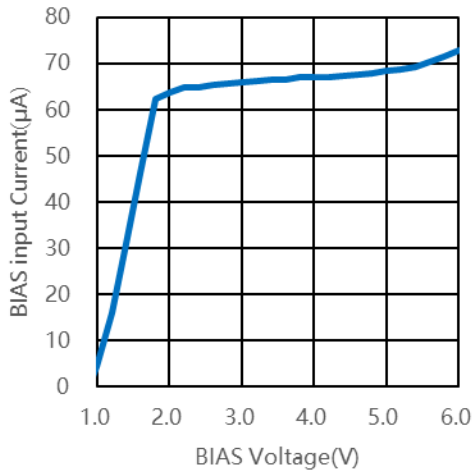


Figure 1 BIAS Quiescent Current vs Voltage,

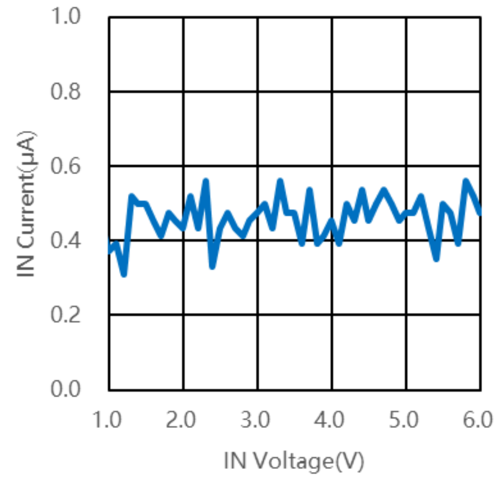


Figure 2. IN Quiescent current vs Voltage

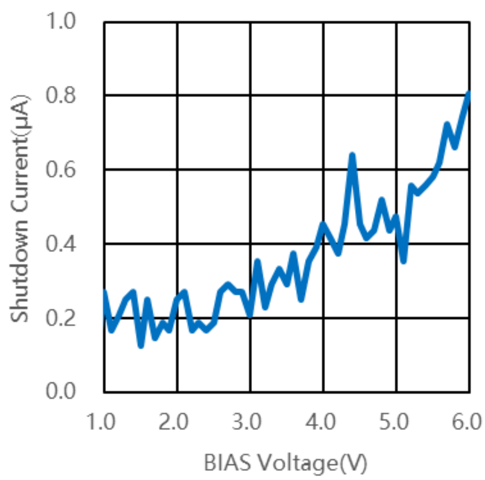


Figure 3 BIAS Shutdown Current vs Voltage

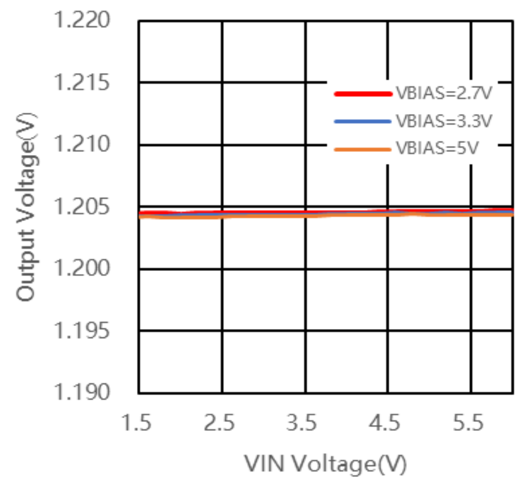


Figure 4 Line Regulation: Output Voltage vs Input voltage

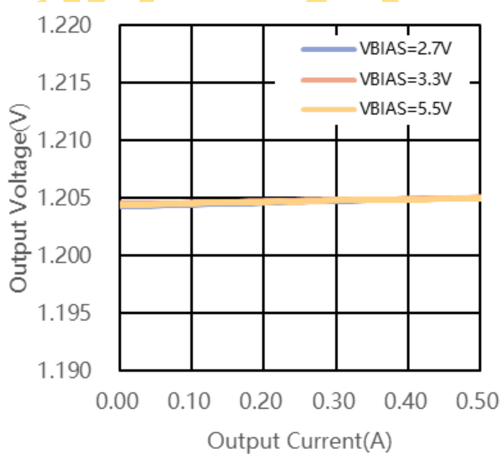


Figure 5 Load Regulation: Output Voltage vs Output Current

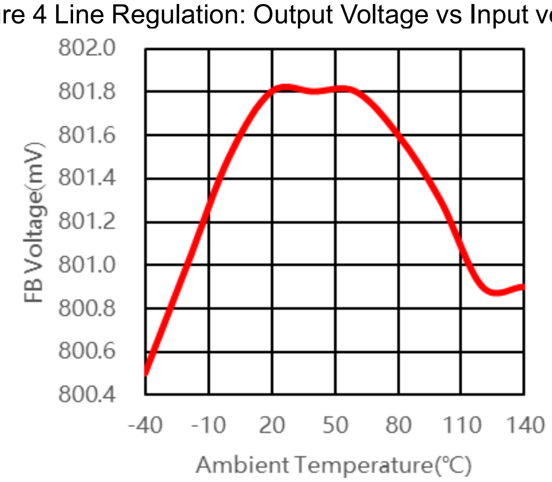


Figure 6 FB voltage vs Temperature

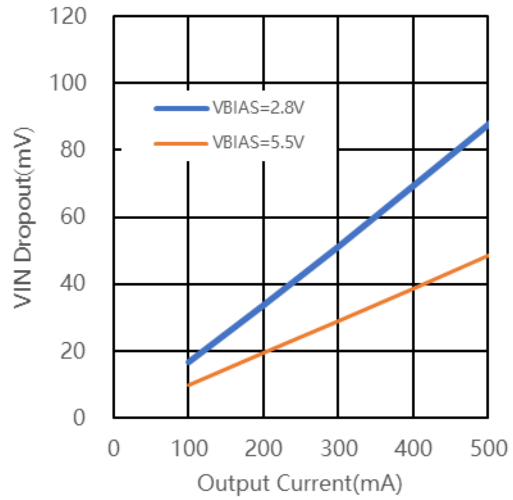


Figure 7 IN Dropout Voltage vs Output Current

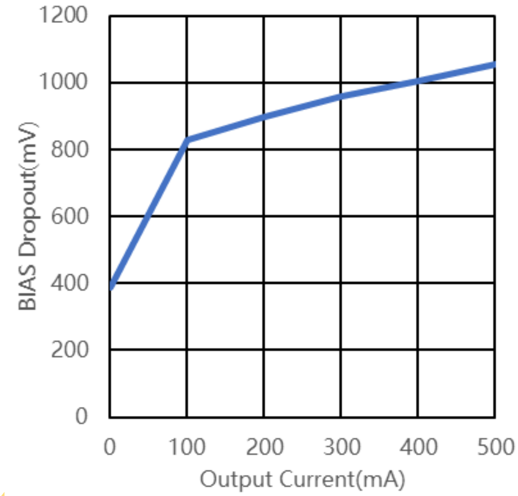


Figure 8 BIAS Dropout Voltage vs Output Current

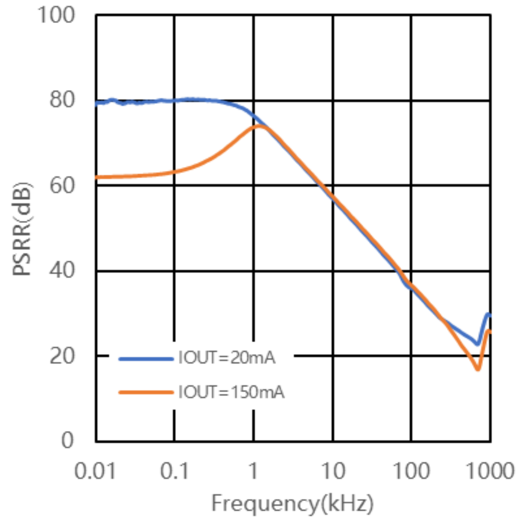


Figure9 IN to OUT PSRR vs Frequency

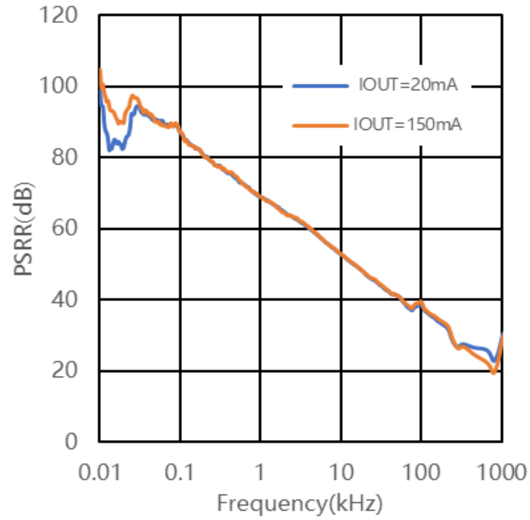


Figure 10 BIAS to OUT PSRR vs Frequency

Typical Characteristics(continued)

(T_J = 25℃, V_{IN} = V_{EN} =1.5V, R_1=25.5kΩ, R_2=51kΩ, V_{BIAS} = 2.7V, C_{IN} = C_{BIAS} = 1.0μF, C_{OUT}=2.2μF, unless otherwise noted.)

Start up and Turn off with EN:(I_{OUT}=1mA)

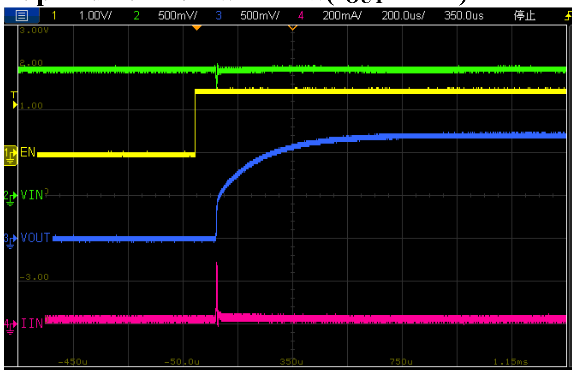


Figure 11 Start up with EN on

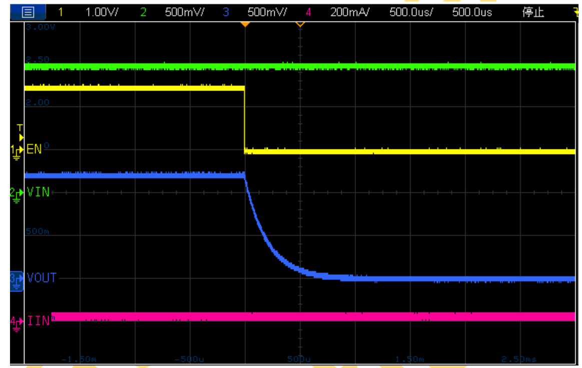


Figure 12 Turn off with EN off

Load Transient: I_{OUT}=1mA <->500mA

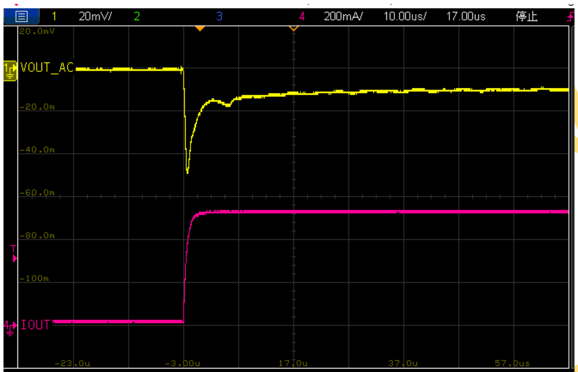


Figure 13. Load Transient 1mA->500mA,

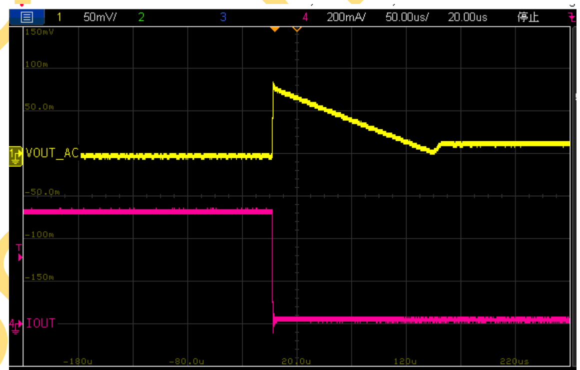


Figure 14. Load Transient 500mA->1mA,

VIN Line Transient: V_{IN}=1.5V <->2.5V

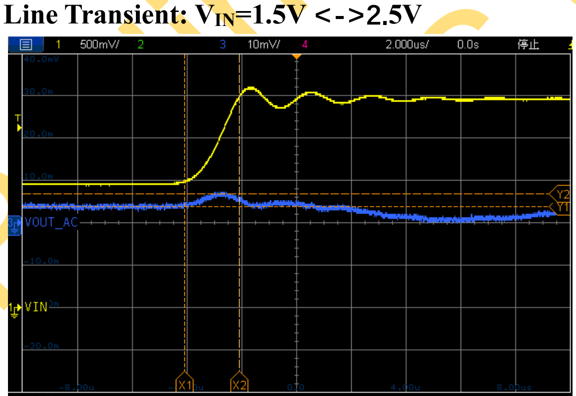


Figure 15. Line Transient V_{IN}=1.5V-> 2.5V with I_{OUT}=1mA

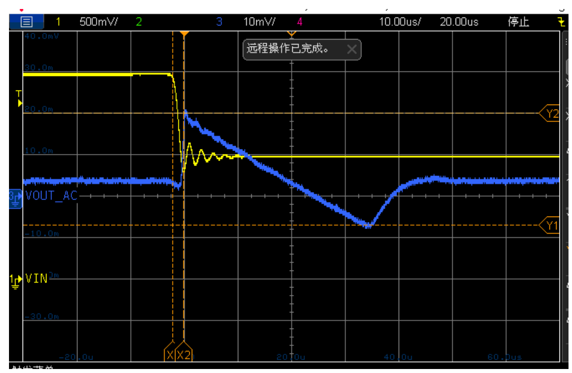


Figure 16. Line Transient V_{IN}=2.5V-> 1.5V with I_{OUT}=1mA

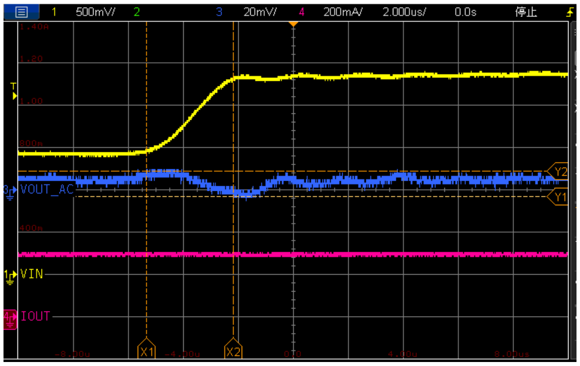


Figure 17. Line Transient V_{IN}=1.5V-> 2.5V with I_{OUT}=300mA

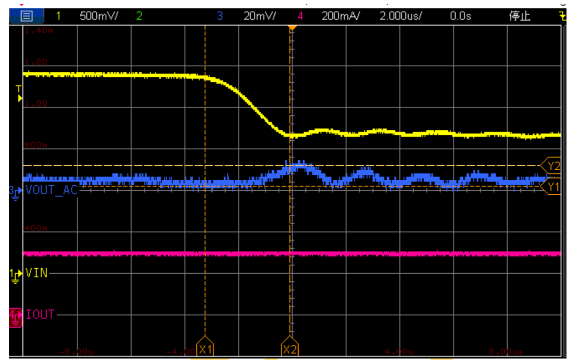


Figure 18. Line Transient V_{IN}=2.5V-> 1.5V with I_{OUT}=300mA

BIAS Line Transient: V_{BIAS}=2.7V <->3.7V

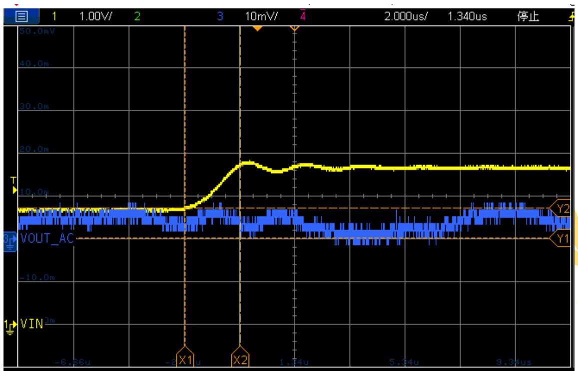


Figure 19. Line Transient V_{BIAS}=2.7V-> 3.7V with I_{OUT}=1mA

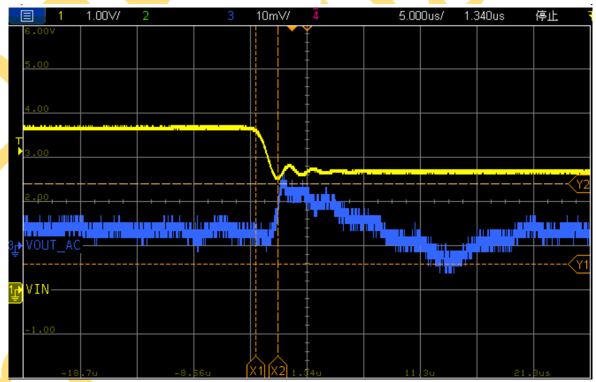


Figure 20. Line Transient V_{BIAS}=3.7V-> 2.7V with I_{OUT}=1mA

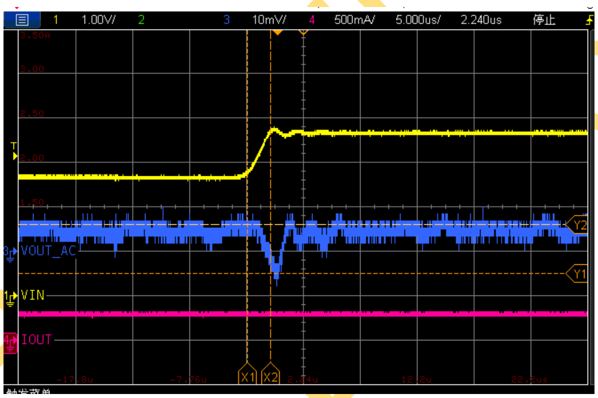


Figure 21. Line Transient V_{BIAS}=2.7V-> 3.7V with I_{OUT}=300mA

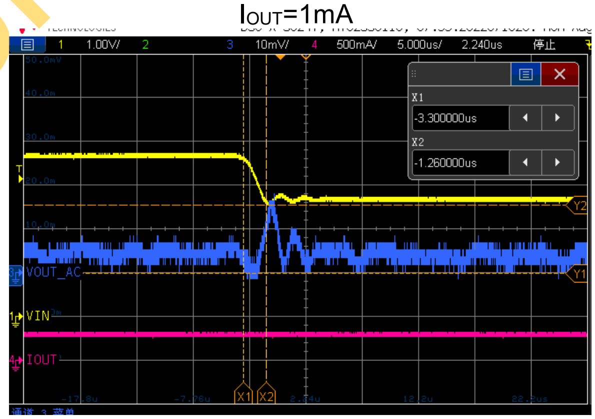


Figure 22. Line Transient V_{BIAS}=3.7V-> 2.7V with I_{OUT}=300mA

Functional Block Diagram

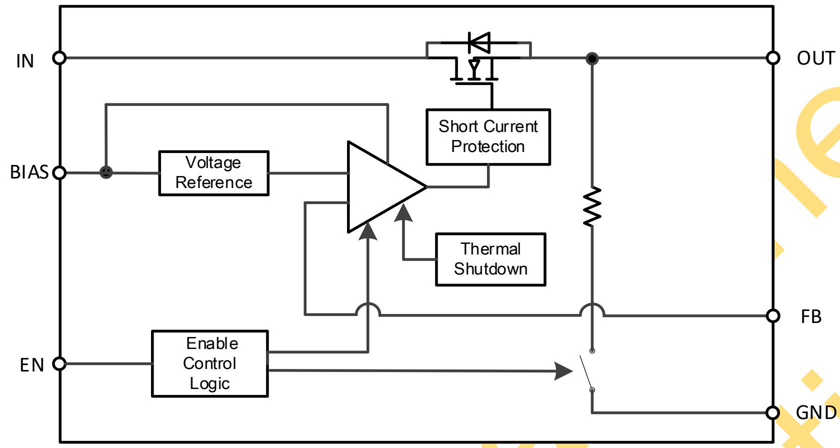


Figure 23. LP3998A functional block diagram

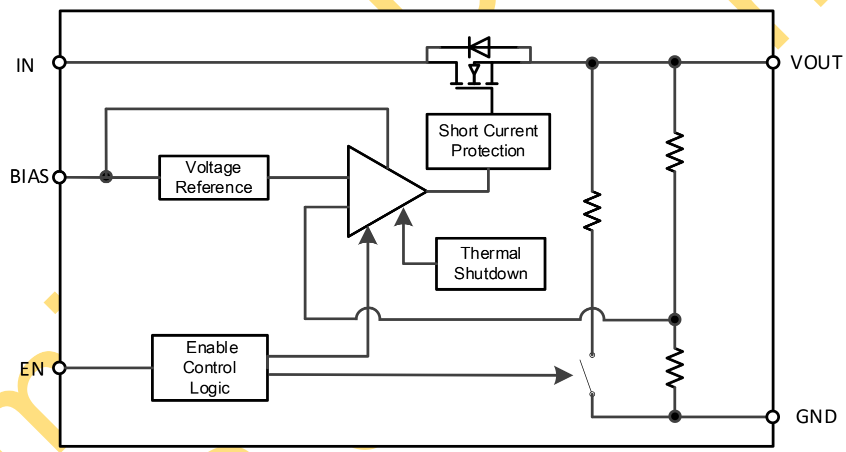


Figure 24. LP3998-XX functional block diagram

Detailed Description

Overview

The LP3998 family are high performance, low dropout linear regulators with fixed 0.9V to 3.6V output voltages or adjustable voltage of 0.8V to 5.0V and up to 500 mA output current capability. Optimized for using with ceramic capacitors, the device provides excellent transient performance and suitable for powering digital circuits.

Internally, the devices consist of a voltage reference, an enable control logic, an error amplifier, a feedback voltage divider, and an NMOS pass transistor. Output current is delivered via the NMOS pass device, which is controlled by the error amplifier. The error amplifier compares a reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the NMOS device is pulled higher, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the NMOS device is pulled lower, allowing less current to flow and decreasing the output voltage.

Adjustable Output Voltage

LP3998A output voltage is adjustable, which is programmed by an external resistor divider. The output can be calculated be by the following equation:

$$V_{OUT}= (1+ R_1/ R_2) \times V_{REF}$$

Where V_{REF} is the internal reference voltage, which is 0.8V in LP3998A. It recommends R2 resistance ranges from 10kΩ to 100kΩ.

Enable Function

The EN pin is a high active logic input pin. The internal power element is turned off when EN pin is tied low or left floating. When the EN pin is pulled high, the LP3998 will be activated and output voltage according to the setting.

Auto Discharge

The LP3998 has a quick discharge function. When the device is disabled by the pulled-down EN pin, a discharge resistor is connected between VOUT and GND. The resistance is 100Ω typically.

Short Current Limit Protection

When the output current at the VOUT pin is higher than current limit threshold or the VOUT pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 100mA to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

When the internal junction temperature of LP3998 family devices exceed the junction thermal shutdown threshold (160℃ typical), the devices will shut down the output, after the junction temperature falls below 140℃ , the VOUT voltage will resume.

Application Description

Thermal Consideration

The reason that causes thermal shutdown protection of an LP3998 device is the power dissipation. Nearly all of the power dissipation is generated by the internal NMOS pass device. The power dissipation can be calculated approximately as,

$$P_D = (V_{IN} - V_{OUT}) * I_{LOAD}$$

where P_D is the power dissipation. When the power dissipation of the LDO device is too much and the operating junction temperature exceeds 160℃，the device will trigger thermal shutdown protection.

The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction -to-ambient thermal resistance.

Input and BIAS Capacitors (C_{IN}, C_{BIAS})

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. An above 1μF ceramic capacitor for C_{IN} and an above 0.1μF ceramic capacitor for C_{BIAS} is recommended to connect between IN/BIAS and GND pins to decouple the power supply glitches and noise. This C_{IN} and C_{BIAS} must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

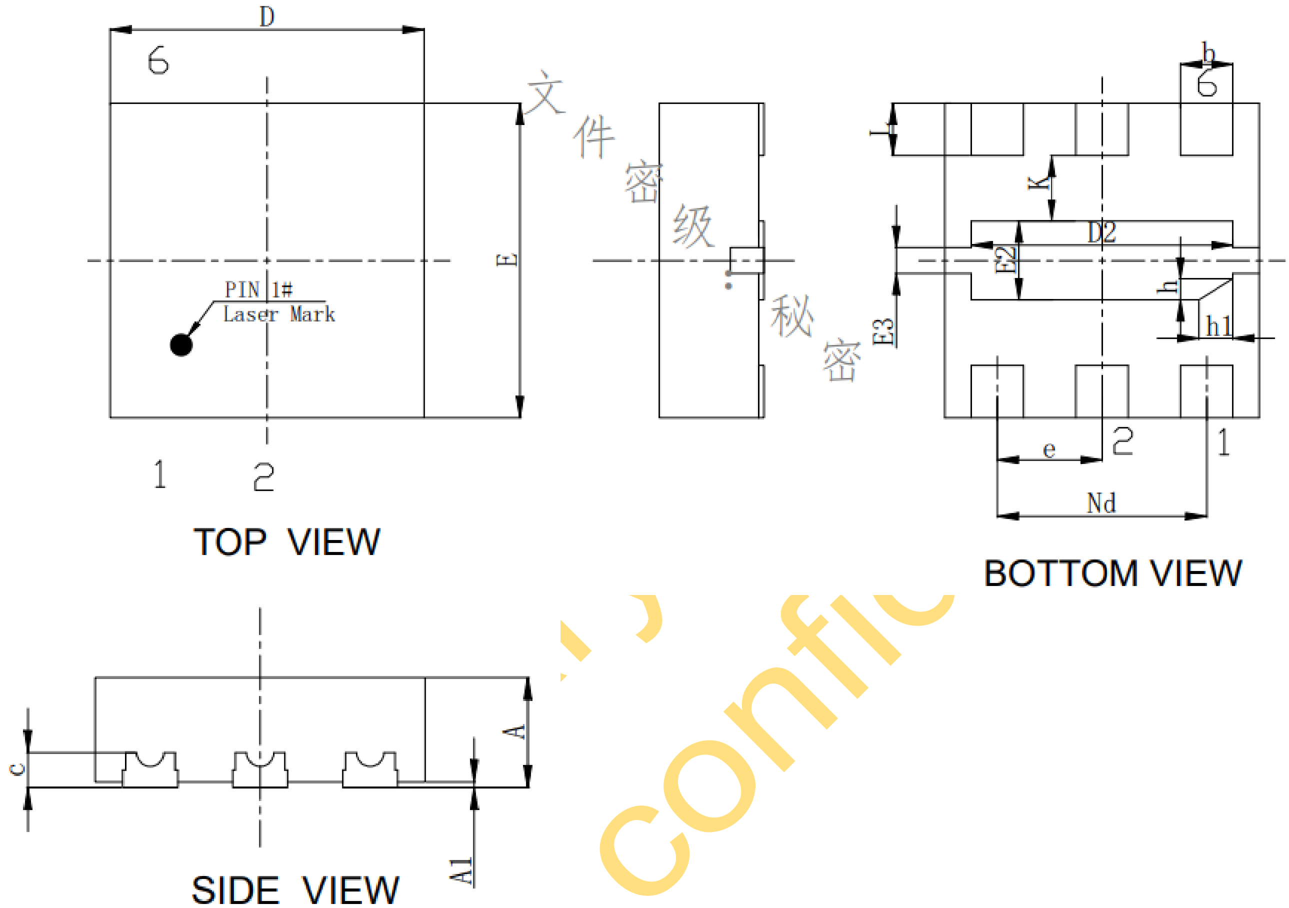
The LP3998 requires a minimum effective capacitance of 1 μF for output voltage stability. The recommended output capacitance is from 2.2μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as practically possible.

Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practically possible to the respective LDO pins. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible with a wide and component-side copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device.

Packaging Information

DFN1.2x1.2-6

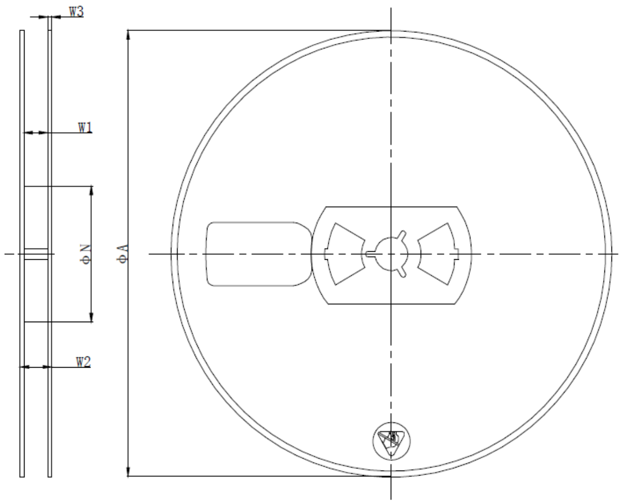


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.60
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.127 REF		
D	1.15	1.20	1.25
D2	0.90	1.00	1.10
e	0.40 BSC		
Nd	0.80 BSC		
E	1.15	1.20	1.25
E2	0.20	0.30	0.40
E3	0.10 REF		
L	0.15	0.20	0.25
h	0.03	0.08	0.13
h1	0.08	0.13	0.18
K	0.25 REF		

Tape and Reel Information

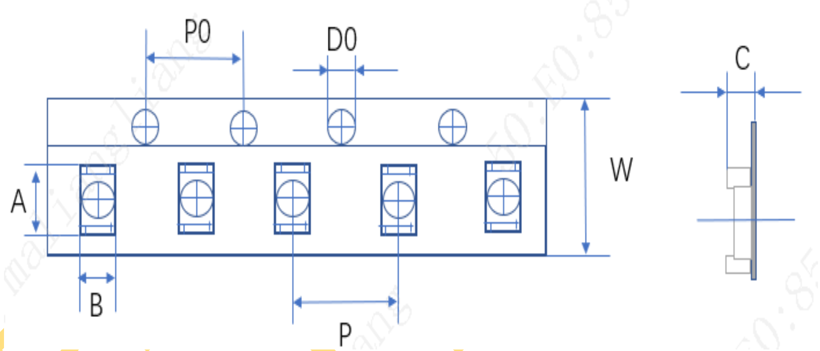
DFN1.2x1.2-6

REEL DIMENSIONS



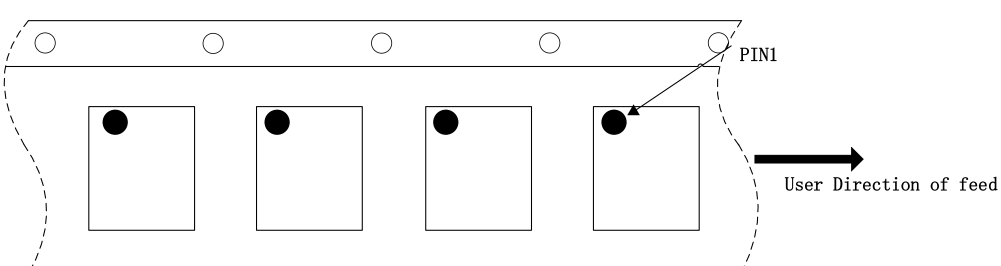
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	6.60	8.60	10.60

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.17	1.37	1.57
B	1.17	1.37	1.57
P0	3.80	4.00	4.20
P	3.80	4.00	4.20
D0	1.35	1.55	1.75
W	7.70	8.00	8.30
C	0.35	0.55	0.75

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min(T_{SMIN}) Temperature Max(T_{SMAX}) Time(T_S) from (T_{SMIN} to T_{SMAX})	 100℃ 150℃ 60~120 seconds	 150℃ 200℃ 60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L) Time(t_L) maintained above T_L	183℃ 60~150 seconds	217℃ 60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

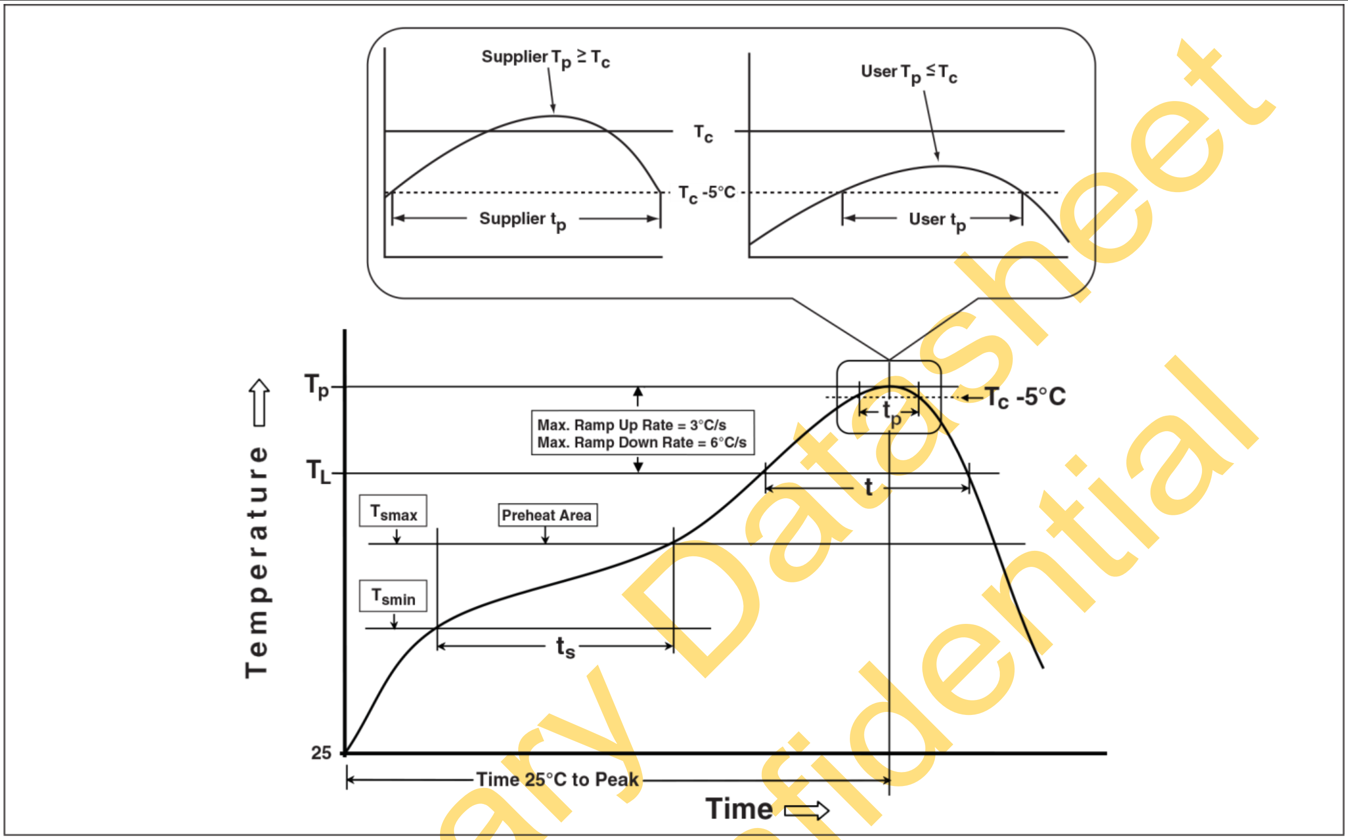


Figure1Classification Profile (Not to scale)

Products conform to “JEDEC J-STD-020C” standards;

Products shipped conform to “Rohs” standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;