LP7813

30V, I^2C Controlled, 1A Switch Mode TWS Solution

Features

- Input over-voltage protected up to 30V
- Charge management
  - Programmable charge current up to 1A
  - 93% charge efficiency at 0.5A from 5-V input
  - Programmable floating voltage with 0.35% accuracy
  - Programmable trickle charge and termination current with minimum 10mA termination current
- Automatic re-charge and thermal foldback
- I^2C bus to the MCU with an interrupt pin
- Power path management
- Boost converter with up to 0.6A output
- Two independent load switches with up to 250mA output for each channel
- Earphone insertion and removal detection
- Ultra-low quiescent current linear regulator for peripheral devices
- NTC management (JIETA Compliance)
- HALL detection
- Watchdog reset
- Ship Mode with 0.7-µA current
- Rich protections: UVLO, OVP, SCP
- 3mm X 3mm QFN-16 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- TWS
- Wireless Microphone
- Smart Glasses
- Electrical Tool
- Solar-cell charger

General Description

The LP7813 is a fully integrated switch mode charger solution with power path management targeting TWS charging case applications. A low on-resistance BUS-FET is integrated to manage the input power from the VIN pin. A bidirectional buck or boost converter is integrated to manage charging and discharging of the battery. The buck charger supports up to 1A charging current with up to 95% efficiency. The ultra-low quiescent current boost converter consumes less than 2µA quiescent current and supports up to 0.6A output current. Two independent load switches feature earphone insert detection, removal detection and provide power from the PMID pin to the VOL pin and VOR pin with ultra-low voltage drop. An NTC circuit is offered to manage the temperature range that charging or discharging is allowed. A VCC pin delivers power to the system that contains an MCU typically. The LP7813 offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the VIN input and the battery to meet the system loading needs. An I^2C interface enables programming various parameters of charging, discharging, and multiple protection functions. An interrupt output (IRQb) sends a signal to the MCU when an interrupt event happens so the MCU can take actions accordingly. The LP7813 support ship mode by setting the SHIP bit and support three methods to exit ship mode.

Multiple features are offered for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), etc. When powered by a battery, LP7813 can operate with only 5-µA current and this current is reduced to 0.7-µA when in ship mode.

The whole System is in a 16-pin 3 X 3 QFN package.

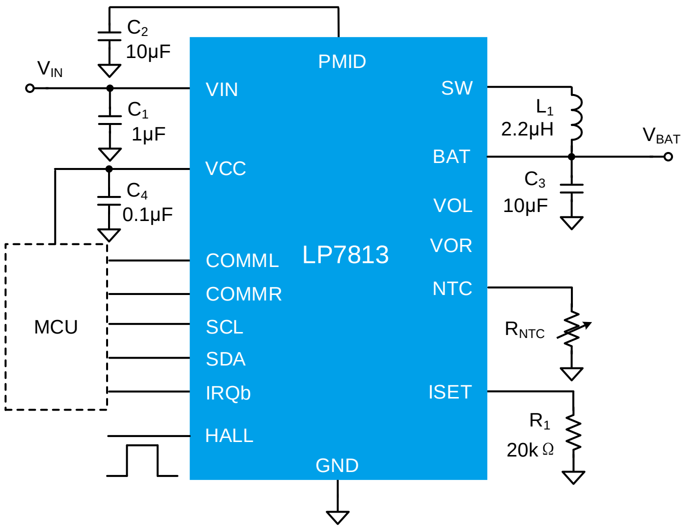
Order Information

LP7813 □□ □

F：Green/Pb-Free

Package Type
QV : QFN

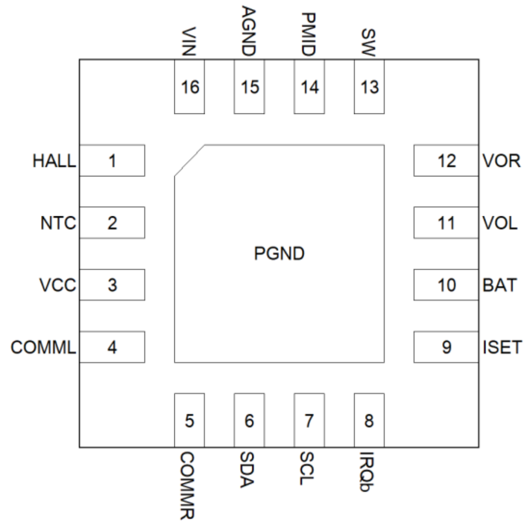
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	MSL
LP7813QVF	LPS LP7813 YWX	16-pin 3 X 3 QFN	3K/REEL	LEVEL 3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. **MSL: Moisture Sensitivity Level according to JEDEC Standard.**				

Pin Diagram



LP7813 Pinout

Pin Description

Pin #	Name	Description
1	HALL	HALL detection. A rising edge at hall will force LP7813 exiting ship mode.
2	NTC	A bias current output at this pin. The internal detection circuit sense this pin for NTC detection.
3	VCC	LDO output pin.
4	COMML	Left earphone communication pin. This pin is bi-directional.
5	COMMR	Right earphone communication pin. This pin is bi-directional.
6	SDA	Data line of the I2C bus. This pin is open-drain output.
7	SCL	Clock line of the I2C bus. This pin is open-drain output.
8	IRQb	Interrupt output to the external MCU. Pull this pin low force LP7813 can exit ship mode.
9	ISET	This pin set the charging current. Don't leave this pin open.
10	BAT	Battery voltage sense pin of the buck charger.
11	VOL	Left earphone power output pin.
12	VOR	Right earphone power output pin.
13	SW	Switch node of the boost converter/ buck charger.
14	PMID	Power input for the buck charger and power output for the load switches. A 10uF or higher ceramic capacitor is required between this pin and the GND pins.
15	AGND	Analog Ground pin. Connect to PGND by PCB layout.
16	VIN	Input voltage that is connected to the positive input of the USB port. 30V maximum voltage rating. A 1uF or higher value input decoupling capacitor must be connected to this pin and the GND pins.
Thermal PAD	PGND	Power Ground pin. This is also the thermal dissipation PAD. Connect to ground plane.

Absolute Maximum Ratings (Note 1)

VIN to GND -- -0.3V to 31V
All other pins to GND -- -0.3V to 6.5V
SW to GND (5ns transient) --- -1V to 8V
Junction Temperature (T_J) -- -40°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec)--- 260℃

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---2kV
CDM (Charge Discharge Model) -- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) --- 55℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.1		5.7	V
I_{IN}	Input current			2	A
T_A	Ambient temperature range	-40		85	°C
C_{IN}	Input decoupling capacitor, 25V rating or higher		1		μF
C_{pmid}	System capacitor, 10V rating or higher		10		μF
C_{bat}	Battery capacitor, 10V rating or higher		10		μF

Electrical Characteristics

(The specifications are at V_{UVLO_IN} < V_{IN} < V_{OVP_IN}, V_{BAT} =3.6V, T_A = -40°C to +85°C and T_A = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{UVLO_IN}	VIN UVLO	V_{IN} falling	3.55	3.7	3.85	V
	Hysteresis			150		mV
V_{OVP_IN}	VIN OVP threshold	V_{IN} rising, 5.85V option	5.7	5.85	6.0	V
	Hysteresis			150		mV
I_{q_IN}	Input quiescent current	V_{IN} =5.0V , V_{BAT} =4.3V ENCHG=1		200		µA
R_{DSON_IN}	BUS-FET on- resistance	V_{IN} =5.0V		0.3		Ω
T_{SS}	Soft-start time of BUS-FET			150		µs
BATTERY SECTION						
V_{BAT_POR}	BAT Power-on-reset	V_{BAT} rising			2.6	V
	Hysteresis			180		mV
I_{BAT}	Quiescent current from BAT	Discharge mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=01, EN_BST=1,STD=0, not include NTC bias current		25		µA
		Standby mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=01, EN_BST=1, STD=1		8		µA
		Standby mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=00, EN_BST=0, STD=1		5		µA
		Standby mode, V_{IN} =5V, V_{BAT} =4.5V, EN_CHG=0		0.3		µA
		Charge mode, V_{IN} =5V, V_{BAT} =4.5V, EN_CHG=1		3		µA
		Ship mode, V_{IN} =0V, V_{BAT} =3.6V		0.7		µA
CHARGE MANAGEMENT						
V_{TRI}	Trickle charge voltage threshold	V_{BAT} rising, V_{TRI}=3.0V option	2.95	3.0	3.05	V
	Hysteresis			100		mV
I_{TRI}	Trickle charge current	R_{ISET}=10K, I_{CC} =1000mA, 10%I_{CC}	90	100	110	mA
		R_{ISET}=10K, I_{CC} =1000mA, 2%I_{CC}	18	20	22	mA
I_{CC}	CC current	25°C, 1000mA R_{ISET}=10K, ICCR[2:0]=000	-5		+5	%
		From -10°C to 85°C, 1000mA R_{ISET}=10K, ICCR[2:0]=000	-10		+10	%
		25°C, 500mA R_{ISET}=10K, ICCR[2:0]=100	-5		+5	%
		25°C, 125mA R_{ISET}=10K, ICCR[2:0]=111	-10		+10	%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CV}	CV voltage	25ºC, V_{CV}=4.2V	-0.35		0.35	%
		From -10ºC to 85ºC, V_{CV}=4.2V	-0.6		0.6	%
		25ºC, V_{CV}=4.35V	-0.35		0.35	%
		25ºC, V_{CV}=4.4V	-0.35		0.35	%
V_{RECHG}	Re-charge threshold	V_{BAT} falling, Reference to CV voltage		-150		mV
t_{drechg}	Recharge deglitch time[Note 2]			30		ms
I_{TERM}	Charge termination current	I_{CC} =1000mA, 12%I_{CC}	110	120	130	mA
		I_{CC} =1000mA, 3%I_{CC}	27	30	33	mA
t_{dterm}	termination deglitch time[Note 2]			30		ms
V_{PMID_DPM}	PMID dynamic power management threshold	V_{PMID} falling, 4.4V option		4.4		V
T_{therm}	Thermal foldback threshold[Note 2]		100	120	140	ºC
f_{SW1}	Buck switching frequency	V_{IN} =5.0V , V_{BAT} =3.6V, ICC=800mA		1.1		MHz
R_{DSON_HS}	HS-FET on resistance	V_{BAT} =3.6V, V_{PMID}=5.1V		0.24		Ω
R_{DSON_LS}	LS-FET on resistance	V_{BAT} =3.6V, V_{PMID}=5.1V		0.12		Ω
I_{BUCK_LIM}	Buck HS-FET peak current limit			1.8		A
BOOST CONVERTER						
V_{PMID}	Boost output voltage accuracy	5.1V option	5.03	5.1	5.15	V
I_{BST_LIM}	Boost LS-FET peak current limit			2.2		A
I_{BYP_LIM}	Boost HS-FET bypass mode current limit	V_{BAT} =4.2V, V_{PMID}=3.5V	0.6	0.8		A
f_{SW2}	Boost switching frequency	V_{BAT} =3.6V, V_{PMID}=5.1V, 500mA		1.3		MHz
V_{BAT_UV}	Battery UVLO	V_{BAT} falling, 3.3V option	3.25	3.3	3.35	V
	Hysteresis	V_{BAT} rising		0.2		V
t_{d_BATUV}	BAT_UV deglitch time[Note 2]			30		us
NTC MANAGEMENT						
I_{NTC}	NTC bias current	-10C/0C/10C/15C,(R_{NTC}=10K)	19.2	20	20.8	uA
		45C/60C,(R_{NTC}=10K)	96	100	104	uA
T_{-10}	-10ºC threshold	V_{NTC} rising	1.07	1.1	1.13	V
	Hysteresis			1		V
T_0	0ºC threshold	V_{NTC} rising	0.63	0.65	0.67	V
	Hysteresis			0.6		V
T_{10}	10ºC threshold	V_{NTC} rising	0.385	0.4	0.42	V
	Hysteresis			0.37		V
T_{15}	15ºC threshold	V_{NTC} rising	0.3	0.31	0.32	V
	Hysteresis			0.28		V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{45}	45°C threshold	V_{NTC} falling	0.43	0.44	0.45	V
	Hysteresis			0.47		V
T_{60}	60°C threshold	V_{NTC} falling	0.24	0.25	0.26	V
	Hysteresis			0.28		V
ULTRA-LOW QUIESCNET CURRENT LDO						
V_{CC}	LDO output voltage accuracy	V_{BAT} =3.6V, VCC[1:0]=00, 5mA load	2.69	2.72	2.75	V
I_{VCC}	LDO output current capability	V_{BAT} =3.6V, VCC[1:0]=00, 5% VCC drop		100		mA
LOAD SWITCH (VOL, VOR)						
I_{PUP}	Load insert detection current	PUP[1:0]=10, 7-μA pull up current, V_{BAT} =3.6V	6	6.5	7	uA
V_{INSERT}	Load insert detection threshold	V_{BAT} =3.6V, V_{PMID} =5.1V, reference to PMID voltage		-0.7		V
t_{dins}	Load insert deglitch time[Note 2]			30		ms
R_{on_EAR}	$R_{ds,on}$ of VOL/R	V_{PMID}=5.1V		650		mΩ
I_{LS_LIM}	Load switch current limit	25℃, EICC=200mA	190	200	210	mA
		25℃, EICC=20mA	18	20	22	mA
I_{LS_LL}	Load switch light load current threshold	EEOC=4mA	3.5	4	5	mA
		EEOC=16mA	14	16	18	mA
t_{dLL}	Load switch light load deglitch time[Note 2]			30		ms
V_{clamp}	VOL/R output clamp	4.6V option	4.55	4.6	4.65	V
HALL, SCL, SDA and IRQb						
V_H	Logic High		1.2			V
V_L	Logic Low				0.4	V
I_{sink}	Sink current capability	V_{BAT} =3.6V, V_{PIN}=0.4V	10			mA
I_{leak}	Pin leakage	V_{PIN}=2.7V		0.01		μA

Note 2: Not production tested. Guaranteed by design.

Typical Characteristics

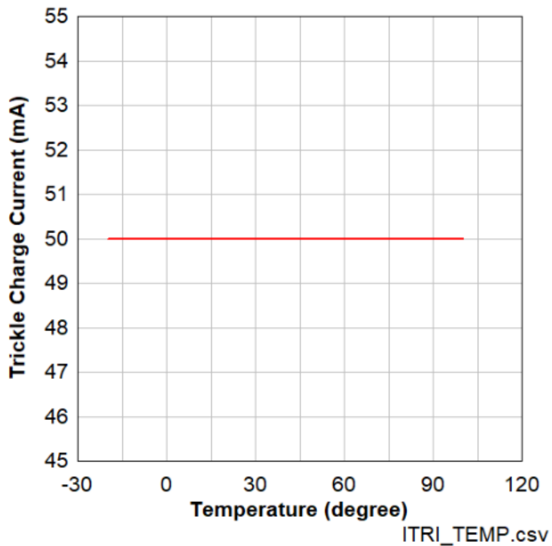


Figure 1. I_{TRI} vs. Ambient Temperature. V_{BAT}=2.5V, 50mA

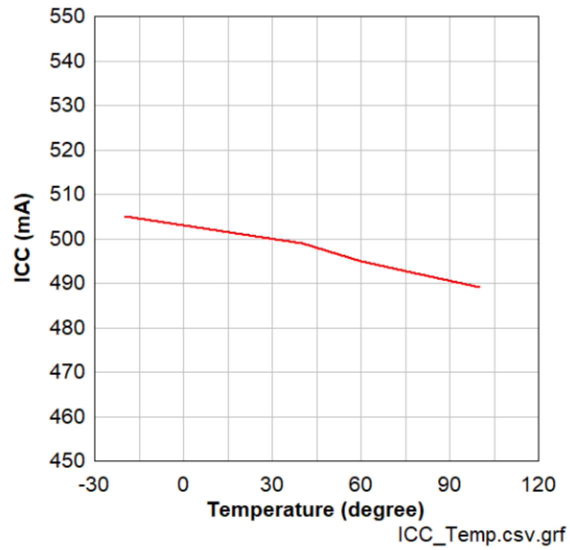


Figure 2. I_{CC} vs. Ambient Temperature. V_{BAT}=3.6V

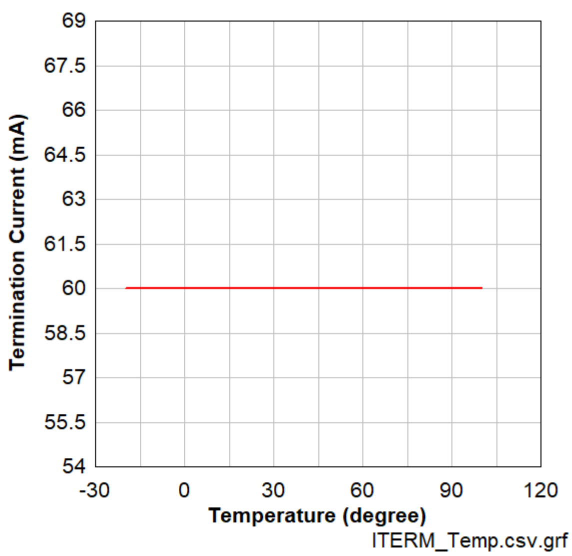


Figure 3. I_{TERM} vs. Ambient Temperature. 60mA

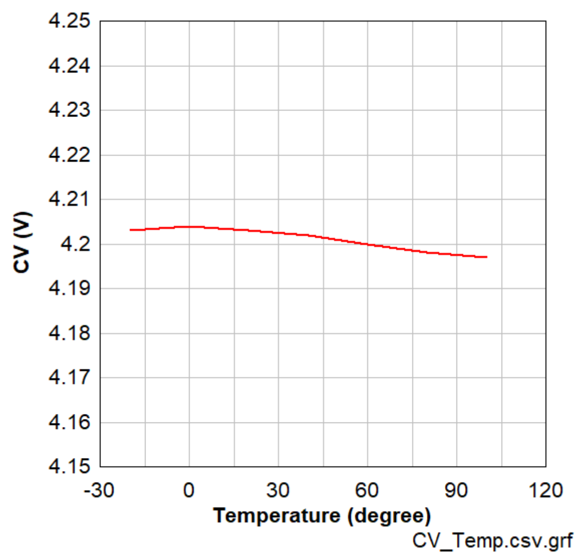


Figure 4. V_{CV} vs. Ambient Temperature. CV=4.2V

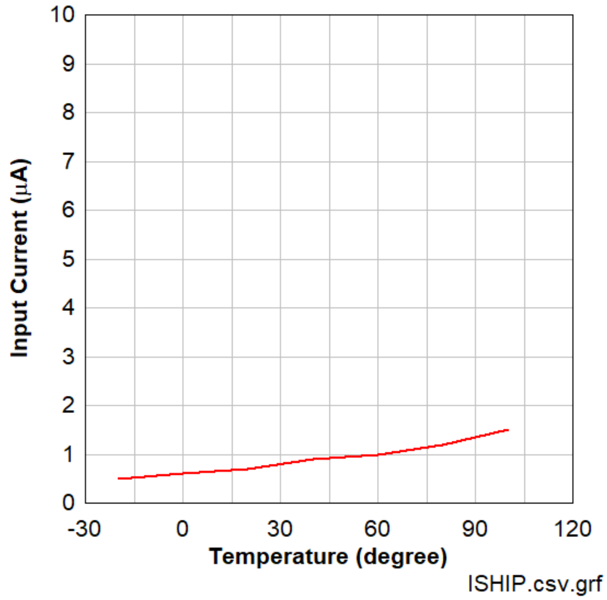


Figure 5. I_{SHIP} vs. Ambient Temperature. V_{BAT}=4.2V

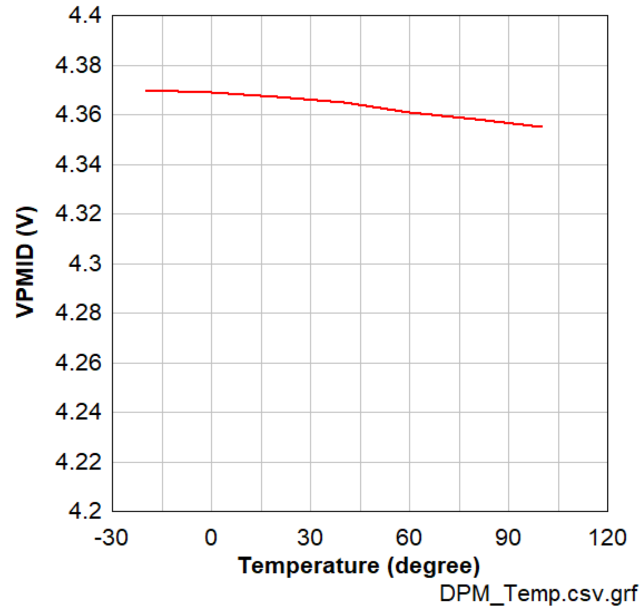


Figure 6. V_{DPM} vs. Ambient Temperature.

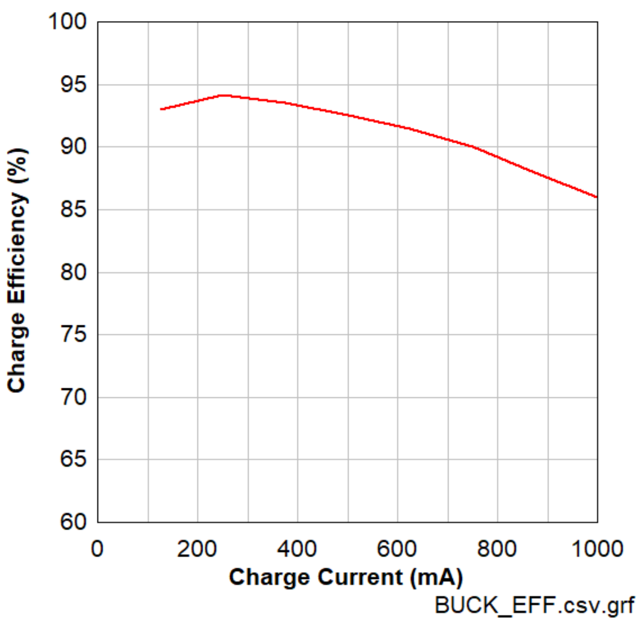


Figure 7. Charger Efficiency. V_{BAT}=3.8V, 2.2µH

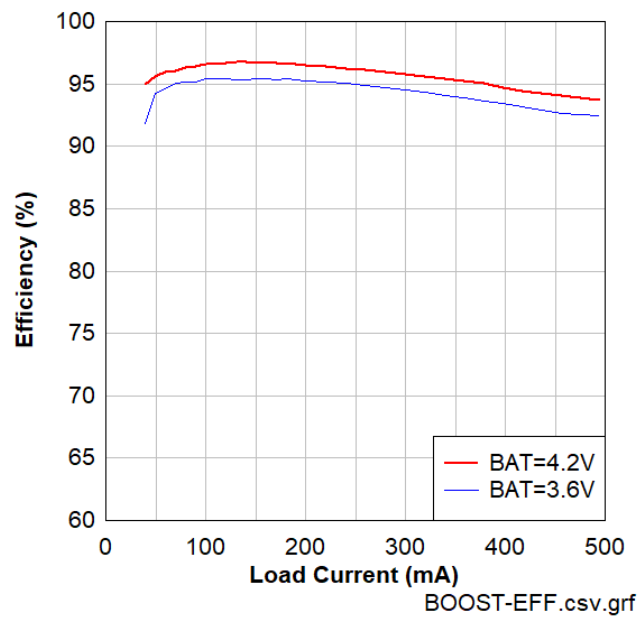


Figure 8. Boost Efficiency. V_{PMID}=4.5V, 2.2µH

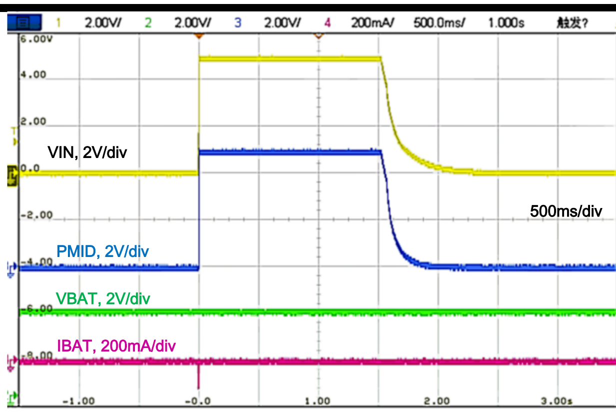


Figure 9. VIN plugged in and unplugged with V_{BAT}=3.6V (EN_BST=EN_CHG=0)

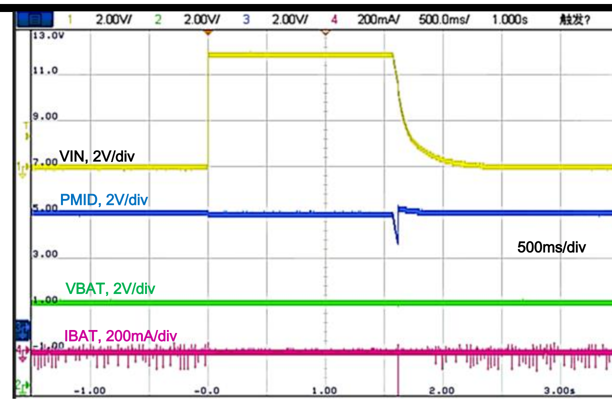


Figure 10. VIN plugged in and unplugged with V_{BAT}=3.6V (EN_BST=1, EN_CHG=0)

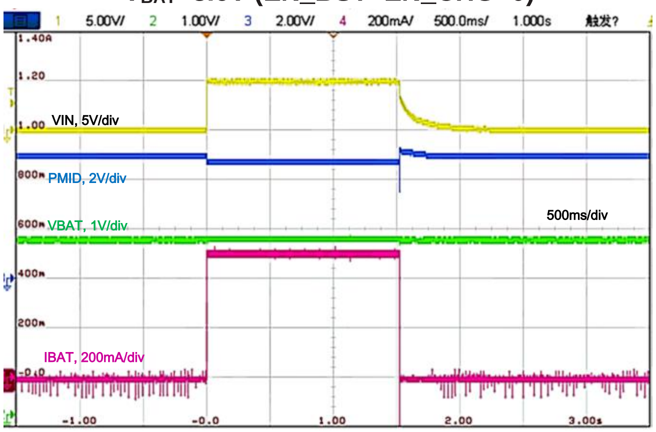


Figure 11. VIN plugged in and unplugged with ICC=500mA, V_{BAT}=3.6V(EN_BST=EN_CHG=1)

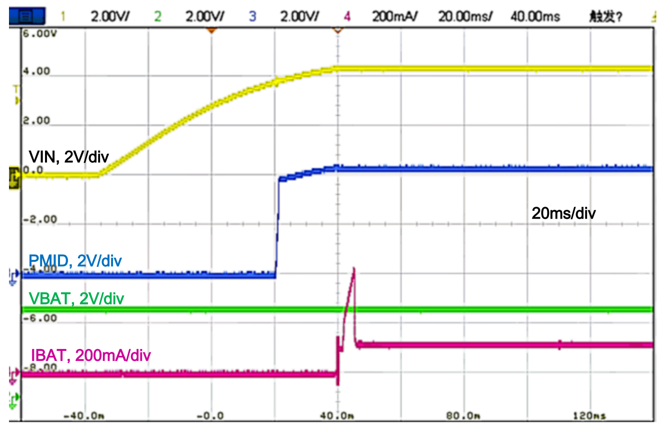


Figure 12. VIN plugged in and unplugged with VIN DPM, ICC=500mA, V_{BAT}=3.6V

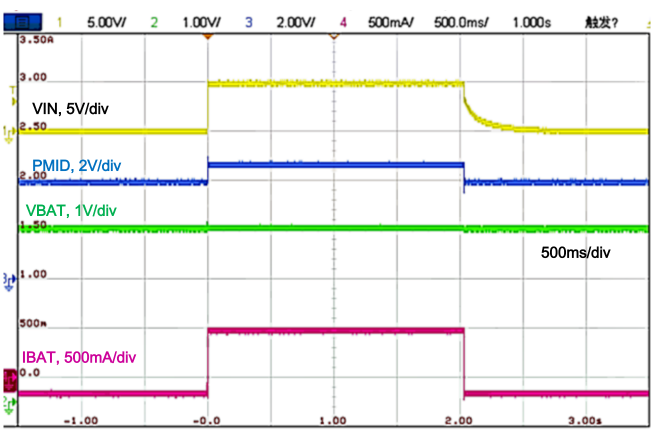


Figure 13. VIN powerup with ICC=500mA, VOL sinks 150mA, V_{BAT}=3.6V

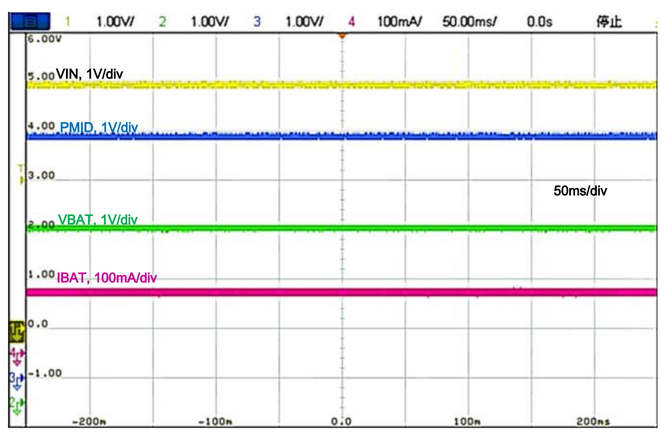


Figure 14. Switch charge, ICC=125mA, V_{BAT}=3.6V

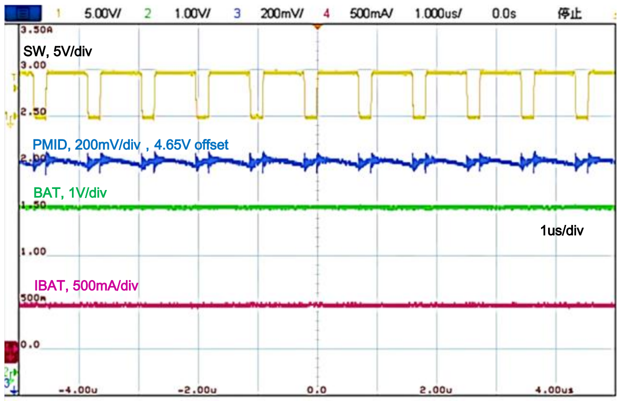


Figure 15. Switch charge, ICC=500mA, V_{BAT}=3.8V

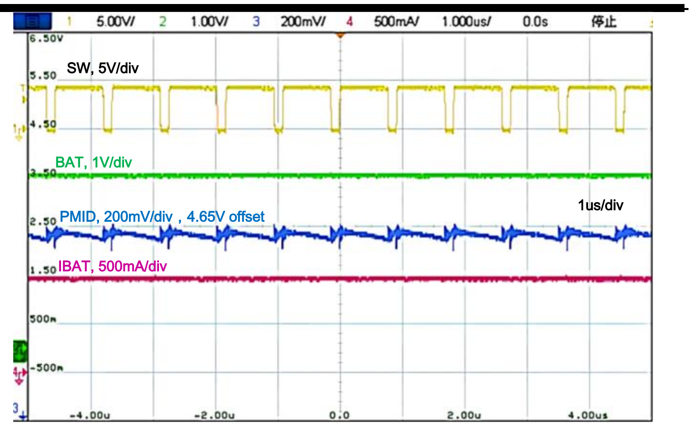


Figure 16. Switch charge, ICC=1A, V_{BAT}=3.8V

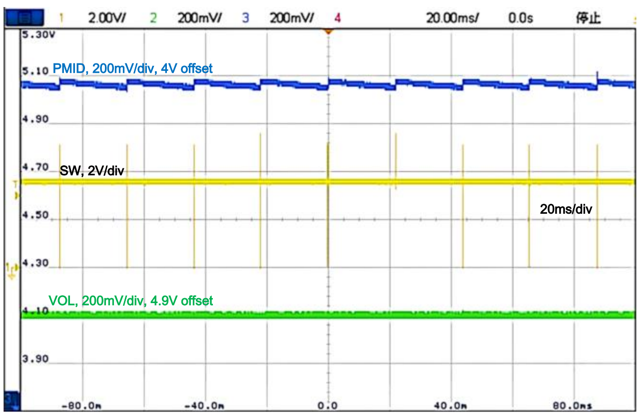


Figure 17. BOOST operation, 10mA, V_{BAT}=3.6V, V_{PMID}=4.6V

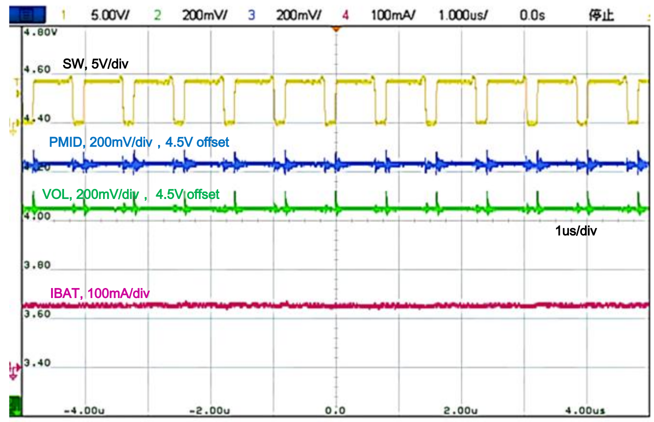


Figure 18. BOOST operation, EICC=100mA load, V_{BAT}=3.6V, V_{PMID}=4.6V

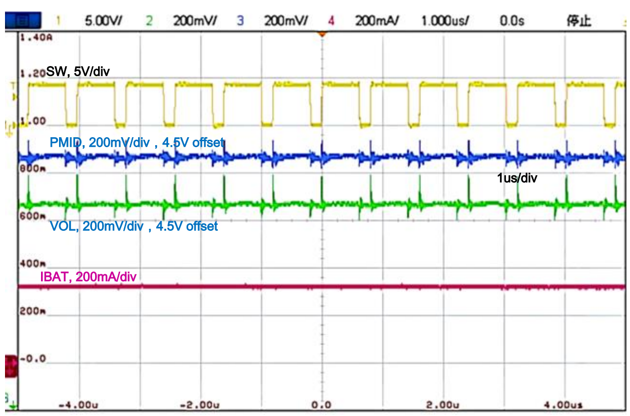


Figure 19. BOOST operation, EICC=250mA load, V_{BAT}=3.6V, V_{PMID}=4.6V

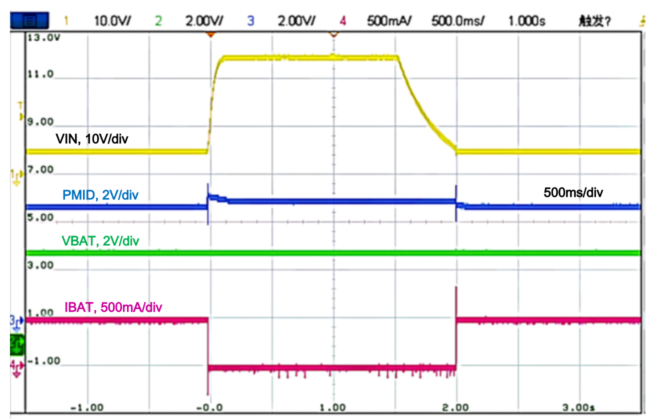
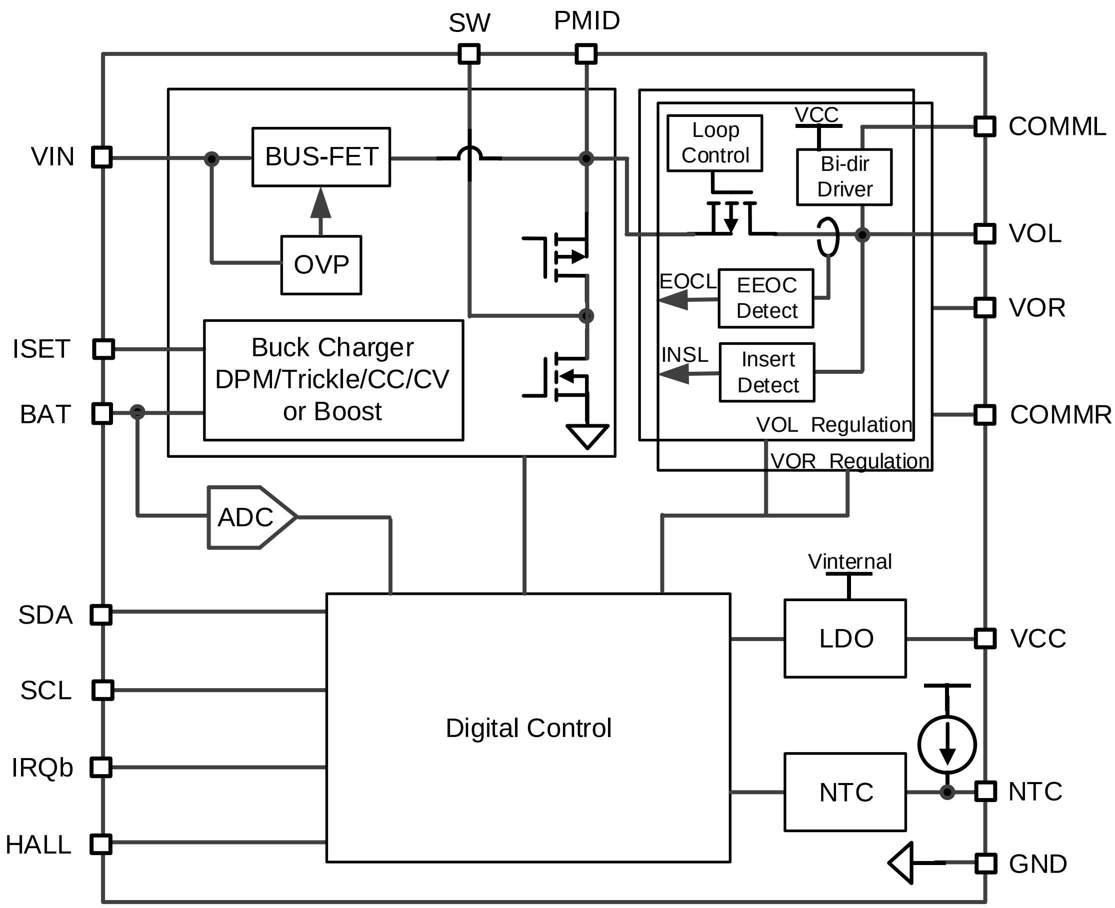


Figure 20. Input OVP and Release

Functional Block Diagram



Detailed Description

Overview

The LP7813 is a fully integrated switch mode charger solution with power path management targeting single-cell Li-ion battery powered portable applications. A low on-resistance BUS-FET is integrated to manage the input power from the VIN pin. A bidirectional buck or boost converter is integrated to manage charging and discharging of the battery. The buck charger supports up to 1A charging current with up to 93% efficiency. The ultra-low quiescent current boost converter consumes less than 2-μA quiescent current and supports up to 0.6A output current. Two independent load switches feature earphone insert detection, removal detection and provide power from the PMID pin to the VOL pin and VOR pin with high accuracy current limit. An NTC circuit is offered to manage the temperature range that charging or discharging is allowed. A VCC pin delivers power to the system that contains an MCU typically. The LP7813 offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the VIN input and the battery to meet the system loading needs. An I^2C interface enables programming various parameters of charging, discharging, and multiple protection functions. An interrupt output (IRQb) sends a signal to the MCU when an interrupt event happens so the MCU can take actions accordingly. The LP7813 support ship mode by setting the SHIP bit, the current consumption is 0.7-μA. The LP7813 supports three methods to exit ship mode, the HALL(opne-lid), the IRQb (press button) and the USB insert.

Multiple features are offered for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), etc.

Power-on Reset (POR)

The LP7813 performs a POR when either the VIN input voltage or the BAT pin voltage is higher than the $V_{BAT\ POR}$ rising threshold. All registers will be set to default values when performing the POR. Refer to the Register Map section for more register information. The MCU can access all registers after POR.

Input Section

The input section contains the BUS-FET and its control circuitry to realize UVLO, OVP and RCP (Reverse current protection).

UVLO and OVP

The input section control circuit monitors the VIN-pin voltage to determine when to turn on or off the BUS-FET. The LP7813 detects an over-voltage event when the input voltage is higher than OVP threshold and turns off the BUS-FET immediately. The LP7813 detects an under voltage (UV) event when the input voltage is lower than V_{UVLO_IN} falling threshold. The LP7813 turns off the BUS-FET immediately as well.

VIN Power Good (PGD)

When it is between the UVLO and the OVP threshold, the input voltage is in a power-good (PGD) range. The BUS-FET is turned on slowly and the PGD bit of the Status Register 0 is set after a 30-ms deglitch time. If the VIN voltage falls off the PGD range, the BUS-FET is turned off.

Reverser Current Protection

If the BUS-FET is reversely biased, i.e. the VIN-pin voltage is only 200mV higher than the BAT-pin voltage, the BUS-FET is turned off immediately and the reverse current is fully blocked. The RCP comparator has a typical 50-mV hysteresis.

Charge Management

The LP7813 will charge the battery through the BUCK charger when the PMID-pin voltage is 150mV higher than the battery voltage. The charger operates with three charging modes, i.e., trickle, CC, and CV modes. During trickle charge mode, the LP7813 is a linear charger to achieve high low-current accuracy. The LP7813 automatically enters switch mode when LP7813 exits the trickle charge mode and enters the CC mode. The LP7813 enters linear mode again when the battery is close to be fully charged. A typical charging cycle is shown in Figure 21. The charging currents and CV are programmable by I^2C. The EN_CHG bit of Control Register 3 can enable the charger. The following describes the details of the charging operation.

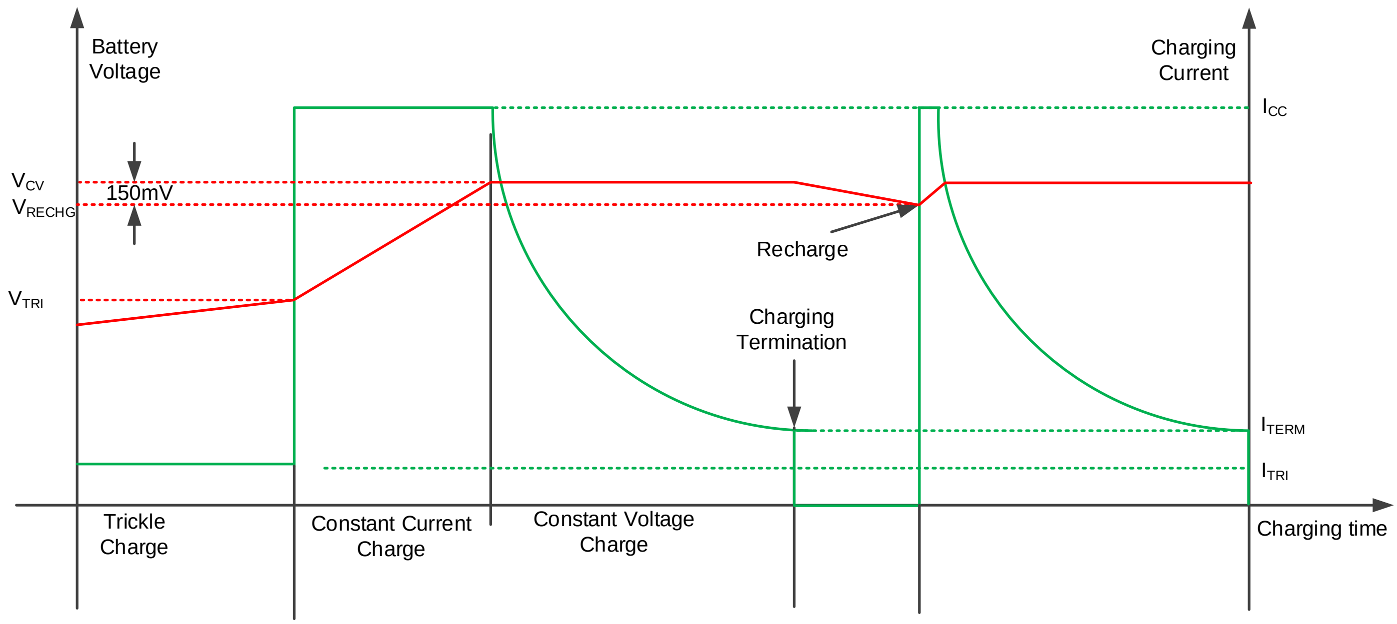


Figure 21. 5V normal charging profile

Start of a Charge Cycle

The charger can be in a charge cycle when all the conditions below are valid,

- PGD = 1
- EN_CHG = 1
- The NTC-pin voltage is in the range of T_0 and T_{45} given in the Electrical Characteristics table.

A new charge cycle will start when the last of the above conditions change from invalid to valid. For example, when the NTC-pin voltage and the PGD are valid when the EN-CHG bit is set.

The CHG[1:0] bits of the Status Register0 is set to 00 before a charge cycle.

Trickle Mode

The charger enters the trickle mode at the beginning of a charge cycle if the battery voltage is below the trickle-charge voltage threshold (V_{TRI}) that is programmable via the VTRI bit of the Control Register 0. The default value is 3.0V. The trickle-charge current is programmable with the R_{ISET} resistance and the ITRI[1:0] bits of the Control Register 0. The LP7813 is a linear mode charger when the battery voltage is below the V_{TRI}.

The CHG[1:0] bits of the Status Register0 is set to 01 in trickle mode.

CC Mode

The LP7813 starts the CC mode when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The charging current is determined by the resistor connected at ISET pin and the ICCR[2:0] bits of the Control Register 1. The CC current is calculated with the equation below:

$$ICC = ICCR[2:0] * \frac{10000}{R_{ISET}} \, (A)$$

For example, the CC current is 400mA if the R_{ISET} is 25kΩ and ICCR[2:0]=000. The CC current is programmable from 10~1000mA and the LP7813 works in switch mode all the time when in CC mode. The default charging current is 100% the current set by the R_{ISET}.

The CHG[1:0] bits of the Status Register0 is set to 01 in CC and CV mode.

Please be noted: The CC current should always 2.5 times higher than the termination current. Please follow the **table 1** to configure the ICCR[1:0] and ITER[1:0] registers.

Table 1 ICCR and ITERM Combination

ITERM Ratio / ICC Ratio	ITERM[1:0]=00, 3%	ITERM[1:0]=01, 6%	ITERM[1:0]=10, 8%	ITERM[1:0]=11, 12%
ICCR[2:0]=000, 12.5%	YES	NO	NO	NO
ICCR[2:0]=001, 25%	YES	YES	YES	NO
ICCR[2:0]=010, 37.5%	YES	YES	YES	YES
ICCR[2:0]=011, 50%	YES	YES	YES	YES
ICCR[2:0]=100, 62.5%	YES	YES	YES	YES
ICCR[2:0]=101, 75%	YES	YES	YES	YES
ICCR[2:0]=110, 87.5%	YES	YES	YES	YES
ICCR[2:0]=111, 100%	YES	YES	YES	YES

CV Mode

The LP7813 starts the CV mode when the battery voltage reaches the CV threshold. The charging current decreases gradually until the charging termination is triggered in this mode. The CV voltage is programmable via the CV[2:0] bits of the Control Register 0. The default value is 4.2V.

Charge Cycle Termination

When the BAT voltage is higher than the recharge voltage and the charging current drops to the termination current threshold, which is programmable with the R_{ISET} resistance and the ITERM[1:0] bits of the Control Register 0. the charging termination is triggered. The charging is terminated immediately and the CHG[1:0] bits of the Status Register0 is set to 11.

Please be noted the termination current should be adjusted according to table 1.

Recharge

A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage while the VIN voltage is still present after a typical 30-ms deglitch time. The LP7813 works in switch mode again at the beginning of recharge cycle.

Charge Current Thermal Foldback

When the die temperature reaches 120 ^{o}C, the charging current decreases to prevent further temperature rise.

NTC Management

An NTC resistor with typical 10kΩ resistance, 1% accuracy and a beta of 3950 is recommended for LP7813. The NTC resistor is enabled by the DISNTC bit with its default value of 0. The internal NTC detection circuitry are disabled when DISNTC bit is set to 1 to reduce the quiescent current.

Four temperature detecting thresholds are provided when charging, i.e., T_0, T_{10}, T_{15}, and T_{45}. An NTC interrupt pulse will be sent when the temperature is crossing these thresholds. The charging is terminated when the temperature range is out of T_0 - T_{45}.

The NTC [2:0] bits are used to indicate the temperature range in the Status Register 0. The MCU can change the charging parameters or disable the charging operation by using the control registers.

The NTC[2:0] will be set to 100 when DISNTC is set to 1.

Battery Voltage Monitor

A 5-bit ADC with minimum 25mV/step to monitor the battery voltage is offered in the LP7813. The ADC samples the battery voltage and the battery voltage range is shown in the VBATM[4:0] bits of the Status Register 2. The VBATM[4:0] can be used in a software gauge. The ADC is always-on until both the VIN and BAT falls below the POR thresholds.

ENCHG Bit

ENCHG bit can enable the charger. When ENCHG is set to 0, the charging cycle is terminated immediately. When ENCHG is set to 1 from 0, a new charging cycle starts again. The default value of ENCHG bit is 0.

ISET Abnormal Detection

The LP7813 performs a ISET detection if a valid power source is present at VIN pin and the ENCHG is set to 1 at the same time. The charging function will not be enabled and the ISET_Abn bit is set to 1 when the ISET pin is short to ground or floating.

If the ISET short or floating when charging, the ISET_Abn bit will not be set at the register table and the charge function will not be forced off.

Power Path Management

The LP7813 integrates the power path management function. The PMID pin can be powered from the input voltage, the battery under different scenarios.

Dynamic Power Management

The voltage at the PMID pin and currents through the BUS-FET is monitored continuously when the LP7813 is powered. The minimum PMID-pin voltage is set by the DPM[1:0] bits of the Control Register 6. When the PMID-pin voltage drops (due to load switches' loading) to the voltage set by the DPM[1:0] bits , the charging current is reduced to prevent the PMID-pin voltage from dropping further. The battery will start providing current if the VIN drops to the V_{UVLO_IN} falling threshold, in which case the HS-FET and LS-FET are controlled as a boost converter.

Boost converter

When the input power is removed, the HS-FET and LS-FET are controlled as a boost converter with up to 0.6A output current capability. The quiescent current of the boost converter is only 2-µA from the battery when there is no load sink by the load switches.

The boost is always-on once ENBST is set to 1 until the BAT pin voltage falls below BSTUV threshold.

Boost Converter Operation

The boost regulator has two operation modes. It operates in the voltage step-up mode when the PMID voltage is required to be higher than the battery voltage. It operates in a by-pass mode when the PMID voltage is required to be lower or equal to the battery voltage. The maximum output voltage of the boost converter is programmable by the VBST[2:0] bits of the Control Register 2. The range is between 3.6V- 5.1V with minimum 50mV/STEP.

PFM and FPWM Operation

The boost regulator improves the efficiency by reducing the switching frequency when the load decreases, this is called the PFM mode.

The LP7813 supports another operation mode, which is FPWM by setting the FPWM register at Control Register 6. In FPWM mode, the switching frequency is kept at 1.3MHz even with no load. In this way, the output ripple is greatly reduced. The quiescent current increase 3~4mA in FPWM and the MCU can disable the FPWM when no earphone is in charge mode (both the ENVOL and ENVOL are set to 0).

Boost Under-voltage Protection

The boost converter is turned off after a typical 200-ms deglitch time when the BAT pin voltage falls below the boost under-voltage protection threshold, which is programmable by the BSTUV[1:0] bits of the Control Register 2. The range is between 3.0V- 3.5V with minimum 100mV/STEP.

The boost converter recovers to operation when the BAT pin rises 200mV above the battery under-voltage protection threshold.

Current Limit

The current flow the HS-FET of the boost regulator is limited to 2.2A when the PMID is overloaded. The current is even reduced to 0.8A when the PMID is short to ground.

ENBST Bit

The boost converter can be enabled by the ENBST bit of the Control Register 3. When ENBST is set to 0, the earphone charge is terminated immediately. The default value of ENBST bit is 0.

Earphone Control

The LP7813 offers two independent control circuits to detect the earphone insert, earphone charge, and earphone light load detection. The earphone charge circuit is achieved by two 600mΩ on-resistance power FETs to provide power for the earphones. Both the load switches are powered by the PMID and the current limit is programmable from 20mA to 250mA with minimum 5mA/step by the EICC[4:0] bits of the Control Register 1.

Earphone insert and removal

The LP7813 supports earphone insert and removal detection. Both the VOL and VOR are pulled to the PMID or BAT with a weak current source, which is programmable by the PUP[1:0] bits of the Control Register 2. The VOL and VOR are pulled at the same voltage level of PMID or BAT when there is nothing connected to the VOL and VOR. When the VOL/R pin is pulled 0.7-V lower than the maximum voltage of PMID and BAT pin because of the earphone insert, the INSL or the INSR bit is set to 1 and an interrupt is sent and the MCU can enable the load switches, i.e., the ENVOL and ENVOR bits to power the earphones.

Earphone charge

The load switches support constant current source function by configuring the EICC[4:0] bits of the Control Register 1.

When work with LP4080H or LP4081, the voltage drop between the PMID and VOL is only 200mV and the system efficiency is improved compared with the traditional 5.1V constant output at the PMID pin. This is the low-voltage dropout mode. The maximum current for the each peripheral device connected at VOL and VOR is 250mA in this mode.

Earphone voltage clamp

The LP7813 integrates two independent clamp control circuits to clamp the maximum output voltage of VOL and VOR by setting the VEAR[1:0] register at Control Register 6 to protect the bluetooth SoC.

The clamp circuit is disabled when the VEAR[1:0] is set to 00, which is the default value.

Earphone light load current detection

When the charge current at each load switch is reduced to less than the earphone light load current threshold which is set by the register EEOC[1:0] bits of the Control Register 4, the EOCL bit or EOCR bit is set to 1 and the interrupt is sent to MCU and the MCU can decide whether to cutoff the power to the earphones. When the earphone is removed from the VOL or the VOR pin, the VOL or the VOR voltage recovers to the level same as the PMID voltage, the INSL bit or the INSR is set to 0 and no interrupt is sent to the MCU this time.

Bi-directional Communication (Bi-dir Driver)

The LP7813 supports bi-directional communication with the COMML and COMMR pins. The MCU can send to or receive the signals from the earphones independently as shown in the Figure 26. The TXL bit enables the signal transfer from the COMML to the VOL while the RXL bit enables the signal transfer reversely. The S_1 and S_2 are closed and the pull-up resistors are enabled once the TXL or RXL is enabled. Both these 2 bits should be set to 0 to save quiescent current when no communication is on-going.

The capacitance at the VOL/R nodes is critical for communication speed. For a typical 115200bps UART communication, less than 1-nF capacitor is allowed.

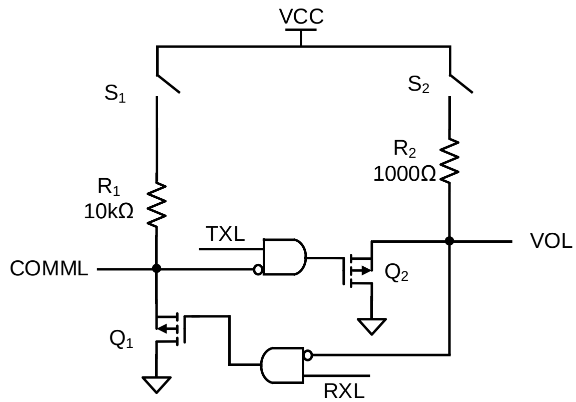


Figure 22. Communication Diagram (VOL channel)

Transmission Gate

The LP7813 integrates a transmission gate for the earphone to exchange bluetooth address. When the TG bit is set to 1, the VOL and VOR are connected together, the signals can transfer between the earphones directly and TXL and TXR are forced to 0, but RXL and RXR are not influenced.

Load switch SCP

The LP7813 integrates short circuit protection as well. The SCPL bit and the SCPR bit of the Status Register 1 is set to 1 and the interrupt is sent to the MCU when any one pin voltage falls below 0.7V. The MCU can take actions accordingly. The current limit is fixed at 150mA when VOL or VOR is below 0.7V.

NTC Management

Two temperature detecting thresholds are provided when the battery is discharging, i.e., T_{-10} and T_{60}. An NTC interrupt pulse will be sent when the temperature is crossing these thresholds. The load switches are terminated when the temperature range is out of T_{-10} - T_{60} by default.

The VOL and VOR are terminated when the temperature range is out of T_0 – T_{45}. If the JEITA bit from Control Register 4 is set to 1.

Ultra-low quiescent current LDO (VCC)

The LP7813 integrates an ultra-low quiescent current linear regulator that is powered by either the VIN or the BAT pin. This output is to power the external MCU, the NTC circuit, the internal logic circuit, and the communication circuit. A 0.1~0.47-μF external ceramic capacitor is required. The LDO output voltage is programmable by the VCC[1:0] bits of the Control Register 5 from 1.8V to 3.3V.

The LDO is always-on once the VIN or the BAT is higher than POR threshold.

HALL Detection

The LP7813 supports hall sensor detection, when the HALL pin is pulled to 1 from 0(close-lid) or pulled to 1 from 0 (open-lid), after 30ms deglitch time, the IRQb is pulled low for 500us and HALL status changes accordingly.

The HALL pin can be used to exit ship mode as well. Please see the Ship Mode Section for more details.

Ship Mode

The LP7813 supports ship mode by setting the SHIP bit to 1 by I^2C when LP7813 is powered by the battery and the input is removed. Before entering ship mode, please set the 0x08 to 00, in this way, all the power blocks and the watchdog are disabled. The LP7813 turns off all the active circuits after the TSHIP deglitch time, which is programmable by the Control Register 5. The LP7813 only consumes 0.7-μA in ship mode.

There are three methods force the LP7813 exiting the ship mode.

1. Pull the HALL pin high (open-lid) for at least 1-s
2. Place a 5V power at the VIN pin for at least 30ms
3. Pull IRQb low for at least 2-s

The I2C interface is turned off and all the registers are set to the default values after LP7813 enters ship mode.

Watchdog

A 32-s typical wait time watchdog is integrated. The SoC should write the WTD bit to 1 before time expires.

When the watchdog timer expires, all the registers recover to the default values after watchdog expires (exclude the EN_WTD bit). The SoC can read the WTD_TIMEOUT bit in Register 03H [7] to check whether a watchdog time expiration event happens. The LDO is disabled for 2-s, in this way, the MCU will be shutdown and can reset itself.

The watchdog is disabled to save quiescent current default and the SoC can enable the watchdog function by setting EN_WTD bit to 1.

Thermal Shutdown

When the internal junction temperature of LP7813 exceeds the thermal shutdown threshold of 150 ºC, the LP7813 disables all the power paths. The LP7813 will not reset the registers and recovers to the default setting after the junction temperature falls to the 130 ºC.

I²C Bus and Interrupt

The LP7813 has an I²C bus and the interrupt IRQb pin. The LP7813 operates as a slave device with an address of 6AH (7bit, 1101010). A 1 or 0 should be placed at the end of the address that represents read or write operation. The SDA, SCL and IRQb are open-drain output.

Interrupt

The interrupt pin IRQb is pulled low for 500-us when an interrupt event happens in the chip. Those events include,

- Input power attaching or removal
- LP7813 starting to charge the battery
- The charging status changes
- Battery voltage falling below the UVLO threshold
- Temperature sensed by the NTC circuit crossing thresholds
- Earphone insertion
- Earphone charge current is less than EEOC
- Any one channel of the VOL/VOR is short circuit.
- HALL pin status change
- Thermal shutdown

The interrupt events can be masked by the control bits in the Interrupt Mask Register 0.

I²C DATA Validity

The data on the SDA line must be stable during the high-level period of the clock, The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low-level.

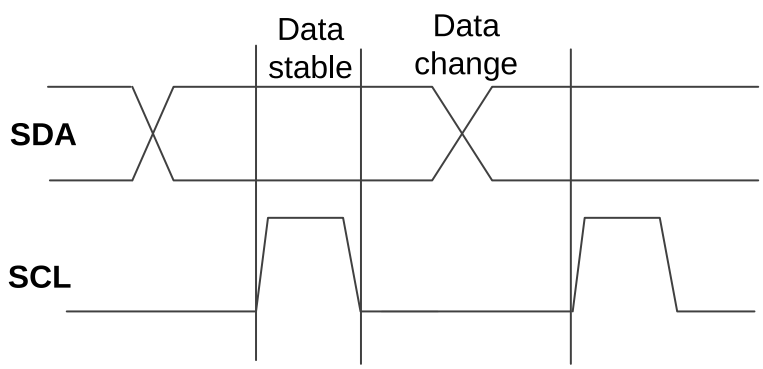


Figure 23. I2C Data validity

I²C Start and Stop Conditions

The data transfer on the SDA line starts with a Start condition and terminated by a Stop condition. A falling edge on the SDA line while the SCL is high means a Start condition. A rising edge on the SDA line while the SCL is at high means a Stop condition.

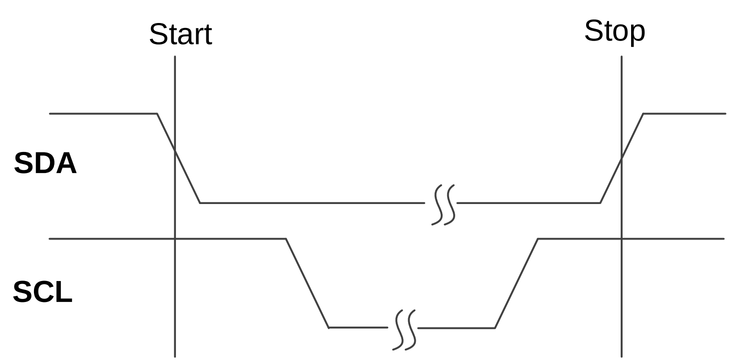


Figure 24. I2C Start and Stop Conditions

I²C Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted, Each byte starts with a MSB(most significant bit) and ends with an ACK bit. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state. Data transfer continues when the slave is ready for another byte of data and release the clock line.

Single Byte Read and Write

1bit	7bit	1bit	1bit	8 bit	1 bit	8 bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	Data to Address	ACK	stop

Figure 25. Single-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1	ACK

8 bit	1bit	1bit
Data from Address	NACK	STOP

Figure 26. Single-byte Read

Multi-Read and Multi-Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit
START	Slave address	0	ACK	Register address	ACK	START

8 bit	1bit	8 bit	1bit	......	8 bit	1bit	1bit
Data to Address	ACK	Data to Address	ACK	......	Data to Address	ACK	stop

Figure 27. Multi-byte Write

1bit	7bit	1bit	1bit	8 bit	1 bit	1bit	7bit	1bit
START	Slave address	0	ACK	Register address	ACK	START	Slave address	1

8 bit	1bit	8 bit	1bit	......	8 bit	1bit	1bit
Data from Address	ACK	Data from Address	ACK	......	Data from Address	NACK	stop

Figure 28. Multi-byte Read

Register Map

Table 2. Device Registers

Register Name	Address	Read/ Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status rgister 0	00H	RO	NTC	NTC	NTC	EOCR	EOCL	INSR	INSL	Reserve
Status register 1	01H	RO	Reserve	Reserve	BSTUV	ISETABN	HALL	SCPR	SCPL	POL
Status register 2	02H	RO	CHG	CHG	PGD	VBATM	VBATM	VBATM	VBATM	VBATM
Interrupt register 0	03H	RC	WTD_TIMEOUT	iHALL	iINS	iEOC	iABN	iNTC	iCHG	iPGD
Mask register 0	04H	RW	Reserve	mHALL	mINS	mEOC	mABN	mNTC	mCHG	mPGD
Control register 0	05H	RW	CV	CV	CV	ITERM	ITERM	ITRI	ITRI	VTRI
Control register 1	06H	RW	EICC	EICC	EICC	EICC	EICC	ICCR	ICCR	ICCR
Control register 2	07H	RW	PUP	PUP	BSTUV	BSTUV	VBST	VBST	VBST	VBST
Control register 3	08H	RW	WTD	SHIP	EN_WTD	DISNTC	ENVOR	ENVOL	ENBST	ENCHG
Control register 4	09H	RW	JEITA	EEOC	EEOC	TG	RXR	RXL	TXR	TXL
Control register 5	0AH	RW	VEAR	VEAR	VCC	VCC	TEEOC	TEEOC	TSHIP	TSHIP
Control register 6	0BH	RW	Reserve	FPWM	VOVP	DPM	DPM	DPM	Reserve	DIS_BUS

Note: **RO**: read only; **RC**: read and clear; **RW**: read and write

Status Register 0 /Address: 00H (default: 0x98)

Table 2. Status Register 0

Bit	Symbol	Description	Read/Write	Default
7	NTC[2]	000: <-10 °C , 001: -10~0 °C	RO	1
6	NTC[1]	010:0-10 °C, 011: 10~15 °C	RO	0
5	NTC[0]	100: 15~45 °C, 101: 45~60 °C ,110:>60 °C ,111: not valid	RO	0
4	EOCR	=1 VOR current is less than EEOC current threshold	RO	1
3	EOCL	=1 VOL current is less than EEOC current threshold	RO	1
2	INSR	=1 VOR is in-case (only invalid when EN_VOR=0)	RO	0
1	INSL	=1 VOL is in-case (only invalid when EN_VOL=0)	RO	0
0	RESERVE		RO	0

Status Register 1 /Address: 01H (default: 0x00)

Table 3. Status Register 1

Bit	Symbol	Description	Read/Write	Default
7	RESERVE		RO	0
6	RESERVE		RO	0
5	BSTUV	=1 Battery is under-voltage	RO	0
4	ISETABN	=1 ISET pin is short or open (Only valid before a charge cycle starts)	RO	0
3	HALL	=1 HALL pin is high-level	RO	0
2	SCPR	=1 VOR is short circuit	RO	0
1	SCPL	=1 VOL is short circuit	RO	0
0	POL	=1 PMID is short circuit	RO	0

Status Register 2/Address: 02H (default: 0x00)

Table 4. Status Register 2

Bit	Symbol	Description	Read/Write	Default
7	CHG[1]	00: Not in charge mode, 01: Trickle mode	RO	0
6	CHG[0]	10:CC/CV mode, 11: Charge termination	RO	0
5	PGD	=1 VIN pin is under V_{OVP_IN} but above V_{UVLO_IN}	RO	0
4	VBATM[4]	Battery voltage: 00000:<3.3V,00001:3.3~3.4V, 00010:3.4~3.5V,00011:3.5~3.6V	RO	0
3	VBATM[3]	00100:3.6~3.65V,00101:3.65~3.7V,00110:3.7~3.75V,00111:3.75~3.8V,01000:3.8~3.85V,01001:3.85~3.875V,01010:3.875~3.9V,01011:3.9~3.925V	RO	0
2	VBATM[2]	01100:3.925~3.95V,01101:3.95~3.975V,01110:3.975~4.0V, 01111:4.0~4.025V,10000:4.025~4.05V,10001:4.05~4.075V,	RO	0
1	VBATM[1]	10010:4.075~4.1V,10011:4.1~4.125V,10100:4.125~4.15V, 10101:4.15~4.175V,10110:4.175~4.2V,10111:4.2~4.225V, 11000:4.225~4.25V,11001:4.25~4.275V,	RO	0
0	VBATM[0]	11010:4.275~4.3V, 11011:4.3~4.35V, 11100:4.35~4.4V, 11101:4.4~4.45V,11110:4.45~4.5V, 11111:>4.5V	RO	0

Interrupt Register 0/Address: 03H (default: 0x00)

Table 5. Interrupt Register 0

Bit	Symbol	Description	Read/Write	Default
7	WTD_TIMEOUT	WATCHDOG timer expiration	RC	0
6	iHALL	HALL pin rise or fall edge (open-lid or close lid)	RC	0
5	iINS	At least one earphone is inserted	RC	0
4	iEOC	At least one earphone is light load	RC	0
3	iABN	Abnormal happens: ISET open, ISET short, PMID SCP, earphone SCP, battery under-voltage or thermal shutdown	RC	0
2	iNTC	NTC cross range or thermal shutdown	RC	0
1	iCHG	Charging status change	RC	0
0	iPGD	Input voltage status change	RC	0

Interrupt Mask Register 0/Address: 04H (default: 0x00)

Table 6. Interrupt Mask Register 0

Bit	Symbol	Description	Read/Write	Default
7	RESERVE			
6	mHALL	Mask Interrupt	RW	0
5	mINS		RW	0
4	mEOC		RW	0
3	mABN		RW	0
2	mNTC		RW	0
1	mCHG		RW	0
0	mPGD		RW	0

Control Register 0/Address: 05H (default: 0x00)

Table 8. Control Register0

Bit	Symbol	Description	Read/Write	Default
7	BAT_CV[2]	Constant voltage set:	RW	0
6	BAT_CV[1]	000: 4.2V 001:4.25V 010:4.3V 011:4.35V	RW	0
5	BAT_CV[0]	100: 4.4V 101:4.45V 110:4.48V 111:4.0V	RW	0
4	ITERM[1]	Termination current set:	RW	0
3	ITERM[0]	00:12%ICC, 01:8%ICC, 10:6%, 11:3% Please be noted, when configuring the ICCR[2:0] the ITERM[1:0] should also be adjusted at the same time. Please refer to Table 1 for details.	RW	0
2	ITRI[1]	Trickle charge current set:	RW	0
1	ITRI[0]	00:10%ICC, 001:6%ICC, 010:4%, 011:2%	RW	0
0	VTRI	Trickle charge voltage set: 0: 3.0V, 1:2.8V	RW	0

Control Register 1/Address: 06H (default: 0X00)

Table 9. Control Register1

Bit	Symbol	Description	R/W	Default
7	EICC[4]	Earphone charge current set: 00000:20mA, 00001:25mA, 00010:30mA,	RW	0
6	EICC[3]	00011:35mA, 00100:40mA, 00101:45mA, 00110:50mA, 00111:55mA,01000:60mA,01001:65mA, 01010:70mA,	RW	0
5	EICC[2]	01011:75mA, 01100:80mA, 01101:85mA, 01110:90mA 01111:95mA,10000:100mA, 10001:110mA, 10010:120mA,	RW	0
4	EICC[1]	10011:130mA,10100:140mA,10101:150mA, 10110:160mA, 10111:170mA, 11000:180mA, 11001:190mA, 11010:200mA,	RW	0
3	EICC[0]	11011:210mA,11100:220mA, 11101:230mA, 11110:250mA, 11111: not valid	RW	0
2	ICCR[2]	CC charge current ratio set	RW	0
1	ICCR[1]	000:100%ICC, 001:87.5%ICC, 010:75%ICC, 011:62.5%ICC	RW	0
0	ICCR[0]	100:50%ICC, 101:37.5%ICC, 110:25%ICC, 111:12.5%ICC Please be noted, when configuring the ICCR[2:0] the ITERM[1:0] should also be adjusted at the same time. Please refer to Table 1 for details.	RW	0

Control Register 2/Address: 07H (default: 0X2D)

Table 10. Control Register2

Bit	Symbol	Description	R/W	Default
7	PUP[1]	Pull up current for earphone insert detection:	RW	0
6	PUP[0]	00: off, 01: 1uA, 10: 7uA, 11: 20uA	RW	0
5	BSTUV[1]	Boost under-voltage set:	RW	1
4	BSTUV[0]	00:3.3V,01:3.4V, 10:3.5V, 11:3.0V	RW	0
3	V_BST[3]	Boost output voltage set:	RW	1
2	V_BST[2]	0000:3.6V, 0001:3.7V, 0010:3.8V, 0011:3.9V,0100:4.0V	RW	1
1	V_BST[1]	0101:4.1V, 0110:4.15V, 0111:4.2V, 1000:4.25V,1001:4.3V	RW	0
0	V_BST[0]	1010:4.35V, 1011:4.4V, 1100:4.5V, 1101:4.6V,1110:4.8V,1111:5.1V	RW	1

Control Register 3/Address: 08H (default: 0X00)

Table 11. Control Register3

Bit	Symbol	Description	R/W	Default
7	WTD	Watchdog bit, write this bit to 1 every 32-s, otherwise all registers are cleared and VCC is disabled for 2-s	RW	0
6	SHIP	=1 Enter ship mode after TSHIP time	RW	0
5	EN_WTD	=1 Watchdog is enabled	RW	0
4	DISNTC	=1 NTC function is disabled	RW	0
3	ENVOR	=1 Right earphone power is enabled	RW	0
2	ENVOL	=1 Left earphone power is enabled	RW	0
1	ENBST	=1 Boost regulator is enabled	RW	0
0	ENCHG	=1 Charge is enabled	RW	0

Control Register 4/Address: 09H (default: 0X00)

Table 12. Control Register4

Bit	Symbol	Description	R/W	Default
7	JEITA	Discharge temperature range set: 0:-10~60C, 1:0~45C	RW	0
6	EEOC[1]	Earphone light load current detection:	RW	0
5	EEOC[0]	00:2 mA, 01:4 mA, 10:8 mA, 11:16 mA	RW	0
4	TG	=1 Transmission Gate is enabled (VOL is short to VOR)	RW	0
3	RXR	1: Right earphone receive data is enabled	RW	0
2	RXL	1: Left earphone receive data is enabled	RW	0
1	TXR	1: Right earphone transmit data is enabled	RW	0
0	TXL	1: Left earphone transmit data is enabled	RW	0

Control Register 5/Address: 0AH (default: 0X00)

Table 13. Control Register5

Bit	Symbol	Description	R/W	Default
7	VEAR[1]	Earphone maximum voltage set:	RW	0
6	VEAR[0]	00: no limit, 01: 4.4V, 10: 4.5V, 11: 4.6V	RW	0
5	VCC[1]	LDO output voltage set:	RW	0
4	VCC[0]	00:2.7V, 01:3.0V, 10:3.3V, 11:1.8V	RW	0
3	TEEOC[1]	Earphone light load current detection deglitch time set:	RW	0
2	TEEOC[0]	00: 30ms, 01:480ms, 10:960ms, 11:3.8s	RW	0
1	TSHIP[1]	Enter ship mode delay time set:	RW	0
0	TSHIP[0]	00:1s, 01:2s, 10:4s, 11:8s	RW	0

Control Register 6/Address: 0BH (default: 0X00)

Table 14. Control Register6

Bit	Symbol	Description	R/W	Default
7	Reserve		RW	0
6	FPWM	=1 Boost if forced PWM mode	RW	0
5	VOVP	VIN OVP threshold set: 0:5.85V, 1:6.4V	RW	0
4	DPM[2]	PMID dynamic power management voltage set:	RW	0
3	DPM[1]	000:4.4V, 001:4.5V, 010:4.6V, 011:4.7V	RW	0
2	DPM[0]	100:4.8V, 101:4.9V, 110:5.0V, 111:5.1V	RW	0
1	Reserve		RW	0
0	DIS_BUS	=1, BUS-FET is turned off	RW	0

Application Information

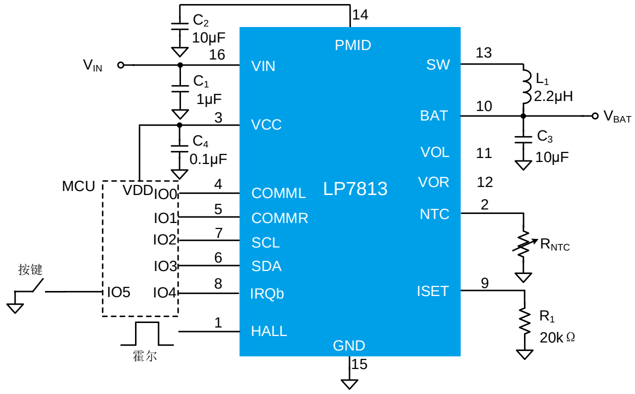


Figure 29. Typical Application Schematic

A typical application consists of the multi-function-in-one power management IC of LP7813 and a host MCU. When powering up in default mode, the battery CV voltage of LP7813 is 4.2V, the termination current is 12% ICC and the trickle charge current is 10%ICC. The maximum output voltage of boost converter is 4.6V and the battery discharge undervoltage protection threshold is 3.3V. The MCU can change all the default values by the I^2C interface.

Inductor and Capacitor Selection

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the VIN, BAT and PMID pin to the GND pin. The VIN capacitor C_1 should be 25V rating with minimum 1-μF capacitance. The BAT capacitor C_3 should be at least 6.3V rating with minimum 10-μF capacitance. The PMID capacitor C_2 should be at least 6.3V rating with minimum 10-μF capacitance. The LDO capacitor C_4 should be at least 6.3V rating with typical 0.1-μF capacitance.

The LP7813 is optimized to work between 1-μH and 2.2-μH inductance.

NTC Circuit Design

As all the trigger point thresholds of the internal NTC comparators are well design with a certain type of NTC resistor, an 10-kΩ NTC resistor with 1% accuracy and with a beta of 3950 is recommended. All the trigger point thresholds can be found in the electrical characteristics table. The default NTC threshold indicates the temperature of -10 ˚C, 0 ˚C, 10 ˚C, 15 ˚C, 45 ˚C, 60 ˚C. The NTC pin can't be left float, setting the R_{NTC} to 10kΩ if NTC is not used.

PCB Layout Guidelines

Please follow the rules when designing the PCB layout.

1. The high frequency filtering capacitor C_2 should be placed with the highest priority and as close to the PMID pin and the PGND pins (the PGND is also the thermal PAD). 0603 size capacitors are recommended. The critical path loop circumference formed by the capacitor and the pins should less than 200 mils to minimize the parasitic inductance. (For example, the enclosed circumference via the C_2, the PMID pin and the thermal PAD should be controlled to less than 200 mils. This the most critical path, marked with yellow line, this path should not use vias.)
2. The C_1 is recommended to serve as the bulk capacitor and an 1Ω resistor is recommended to be in series with C_1 to absorb the input spike when the USB is plugged in. The C_1 should be placed to the VIN pin and the ground plane with less than 300mil loop circumference.
3. The IN, VBAT, VOL, VOR and the GND power paths should be wide and short to improve the system efficiency. As a recommendation, the trace path should be at least 40 mils to deliver 1A current with 1oz copper thickness.
4. The thermal pad which is also the power ground of the device, should be connected to the ground plane to help dissipating the power from the silicon.

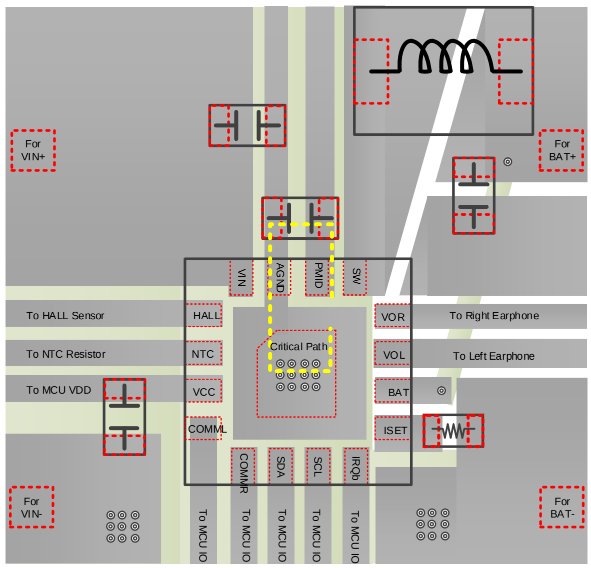
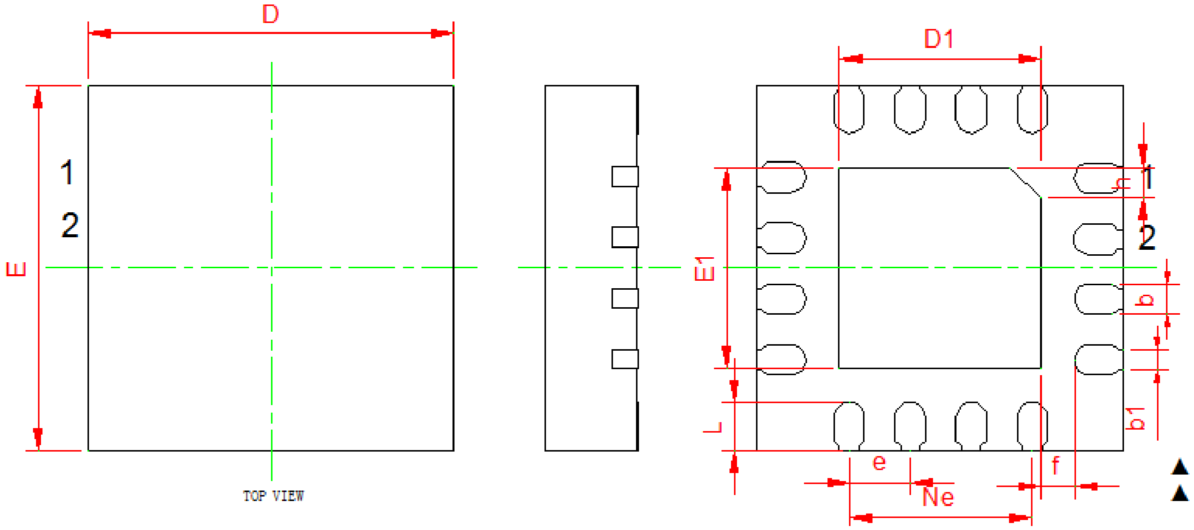
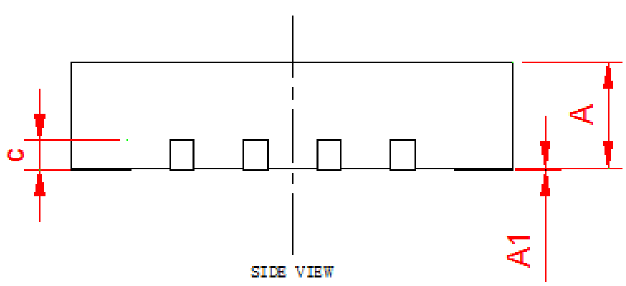


Figure 30. PCB Example (TOP View)

Packaging Information

3x3 QFN package

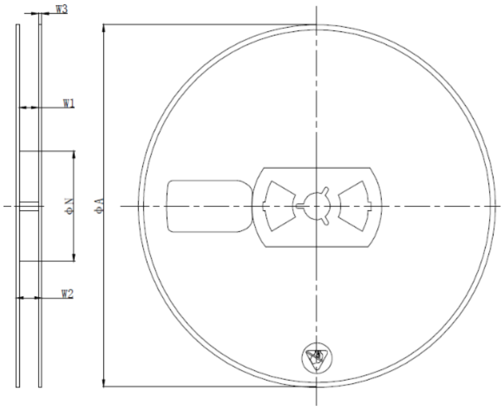




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.200	0.250	0.300
b1	0.160REF		
c	0.180	0.210	0.240
D	2.900	3.000	3.100
E	2.900	3.000	3.100
D1	1.600	1.650	1.700
E1	1.600	1.650	1.700
e	0.500BSC		
Ne	1.500BSC		
f	0.225	0.275	0.325
h	0.200	0.250	0.300
L	0.350	0.400	0.450

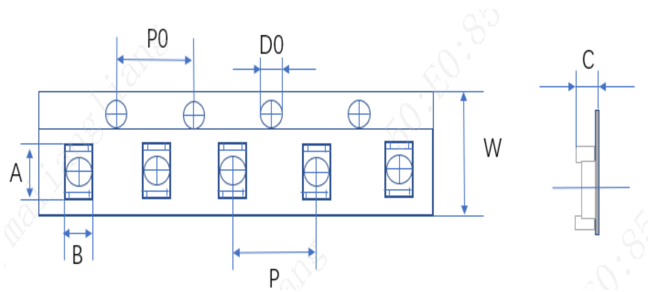
Carrier Information

REEL DIMENSIONS（Unit:mm）



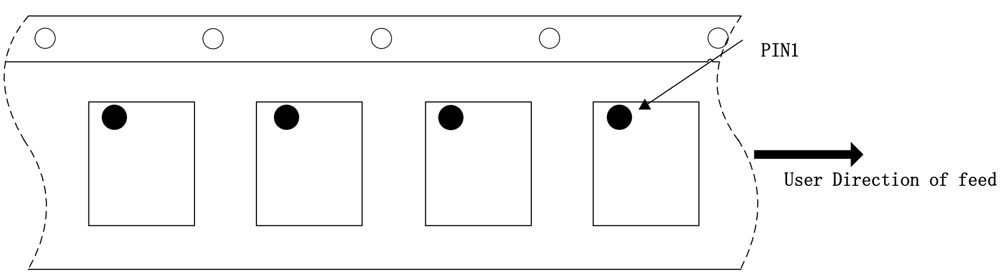
ΦA	W2
329±2	16.4±2

TAPE DIMENSIONS（Unit:mm）



口袋宽度A		口袋长度B		编带孔中心间距P0		IC中心间距P		孔径D0		编带宽度W		编带厚度C	
尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差
3.40	±0.3	3.40	±0.3	4.00	±0.10	8.00	±0.10	1.55	±0.1	12.00	±0.30	1.10	±0.15

PIN1 AND TAPE FEEDING DIRECTION



Revision History

Revision	Date	Change Description
Rev 1p0	2/5/2024	Release Version 0.0