Features

- Input Supply Range
  TV MODE: 8.6V to 14.7V; MNT MODE: 4.3V to 6.0V
- AVDD Async-Boost Converter:
  TV MODE: 13.0V to 19.8V
  MNT MODE: 11.0V to 17.3V
  500/750KHz/1250KHz Switching Frequency
  5A Switching Current limit
  Controller by 0.3V Over-current Protection
- Programmable Internal/External V_{AVDD} Isolation PMOS
- VBK Sync Buck Converter: 1.8V to 3.35V
  500/750KHz/1250KHz Switching Frequency
  2.0A Switching Current Limit
- HAVDD OP
  1 Channel Programmable HAVDD OP
  ±500mA Peak Current
  ±200mA Output Current
  7-bits DAC resolution
- VGH Async-Boost Converter/Charge pump Regulator: 20V to 42V
  500/750KHz/1250KHz Switching Frequency
  1.5A Switching Current Limit
  Temperature Compensation: 20V to 42V
- VGL Async-Inverting Converter/Charge pump Regulator: -3V to -18V
  500/750KHz/1250KHz Switching Frequency
  1.5A Async Inverting Switching Current Limit
  Temperature Compensation: -3V to -18V
- VSS1 Negative Regulators: -3V to -16V
- 14-CH Gamma Buffers
  14 Channels Rail-to-Rail Programmable Gamma Buffers
  10 Bits Resolution for reach channel
- 1-CH VCOM1 Buffer
  1 Channel Programmable VCOM Buffer
  7-Bits Resolution for reach Channel
- 1-CH VCOM2 DAC
  1 Channel Programmable VCOM DAC
  7-Bits Resolution for reach Channel
- Invtegrated MTP Non-Volatile Memory
- Programmable Sequence Timing
- Over-Temperature Protection
- IIC Compatible Interface for Register Control
- Available in 6.5mmX4.5mm 46-pin QFN Package

General Description

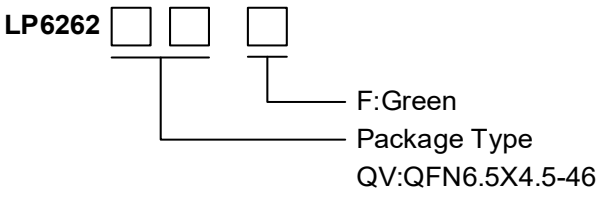
The LP6262 is a programmable multi-functional power solution with integrated gamma buffers, VCOM1 buffer for TFT-LCD. It contains one boost converter controller (AVDD), one ISO MOSFET controller for AVDD power on sequence, one buck converter (VBK), one boost converter/ positive charge pump regulator (VGH) with the temperature compensation, one inverting converter/ negative charge pump regulator (VGL) with the temperature compensation, one negative regulators (VSS1), 14-CH gamma buffers, 1-CH VCOM1 buffer, 1-CH VCOM2 DAC. All channel output level and sequence can be programmable by I2C interface and integrated Multiple-Time Programmable (MTP) non-volatile memory.

With its high current capabilities, the LP6262 is ideal for large screen LCD TV/MNT panel application with widely supply voltage range and also integrated complete protection functions including, OVP, UVP, OCP and OTP The LP6262 available in a QFN6.5x4.5-46 pin package.

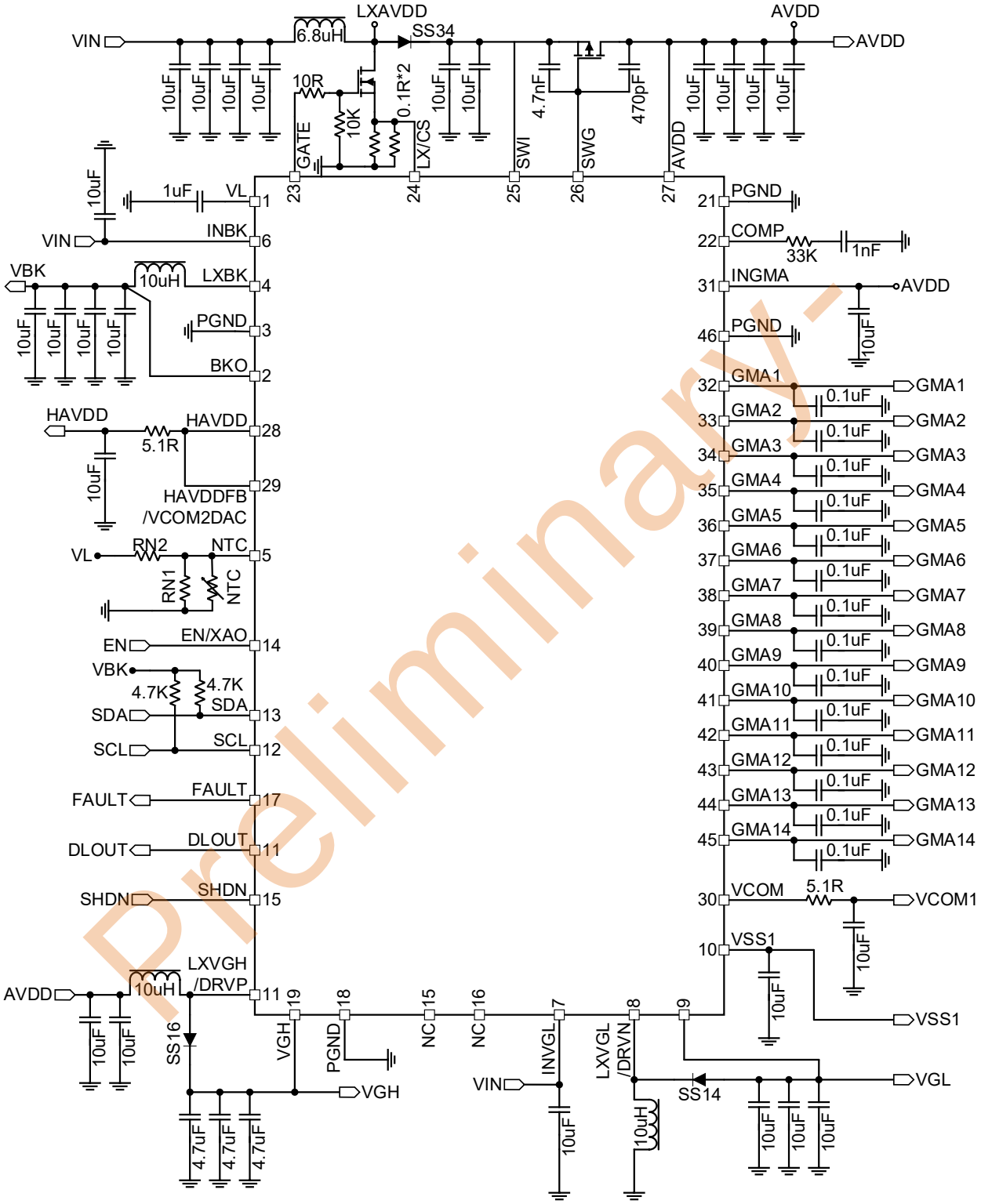
Applications

- TFT LCD Monitor Panel
- TFT LCD TV Panel

Order Information



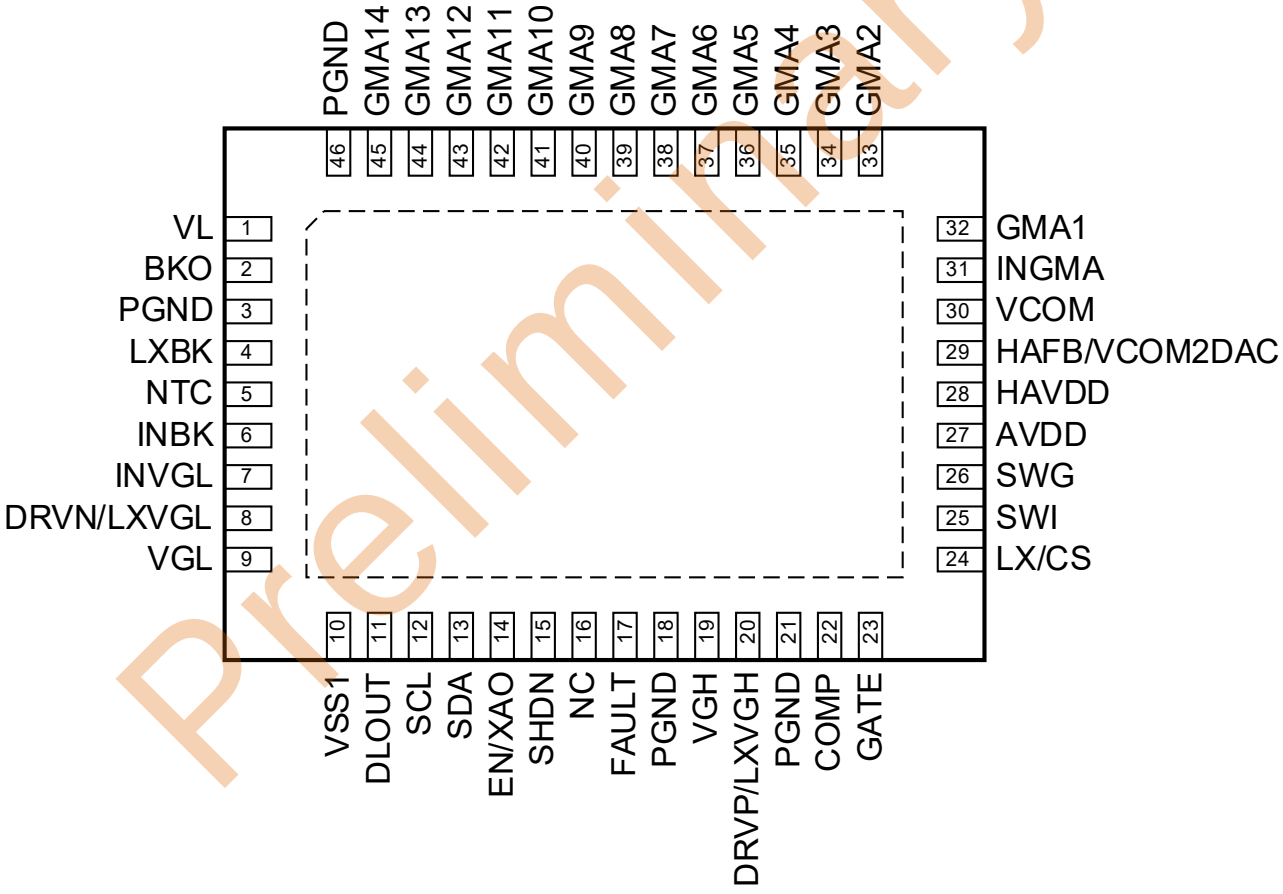
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6262QVF	LPS LP6262 YWX	MSL3	QFN6.5X4.5-46	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



LP6262QVF QFN6.5X4.5-46

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Pin Description

Pin#	Name	Description
1	VL	5V internal linear regulator output
2	BKO	Feedback voltage input for VBK buck converter
3	PGND	Power Ground
4	LXBK	Switch node of the VBK Buck converter
5	NTC	Temperature compensation node, Connect NTC thermistor and resistors to this pin to control the slope of VGH/VGL/VCOM1 voltage for temperature compensation
6	INBK	Supply voltage input of VBK Buck converter
7	INVGL	Supply voltage input of the Inverting converter
8	DRVN/LXVGL	DRVN: VGL charge pump mode, for negative linear regulator base drive LXVGL: VGL Inverting mode, for switch node of the inverting converter
9	VGL	VGL charge pump mode, for feedback voltage input for VGL charge pump regulator VGL inverting mode, for feedback voltage input for VGL inverting converter
10	VSS1	Negative supply voltage output
11	DLOUT	Delay output signal of the Vcore enable.
12	SCL	Clock input pin of the IIC serial interface
13	SDA	Data input pin of the IIC serial interface
14	EN/XAO	@31h,bit7=0, Enable pin of the AVDD,VGH,HAVDD,VCOM1,VCOM2DAC and Gamma. Enable pin must be connect high signal. 400Kohm pull down resistor connect from this pin to ground @31h,bit7=1, XON pin for the shutdown reset function output and open drain voltage detector output.
15	SHDN	Sleep MODE Control, When SHDN is high Level, the chip goes into sleep mode
16	NC	Floating this pin, Do not connect to any other pin or circuit
17	FAULT	FAULT signal input/output pin. The FAULT pin is open drain output with internal pull up resistor. The output High/Low depended on protection functions. It also can be connected the open drain circuit to control IC operations. (1) Ouput channel UVP/SCP except VBK channel FAULT_O pin is Low active and all output channel shutdown except VBK (2) VBK UVP/SCP FAULT_O pin is Low active and all output channel shutdown (3) External signal FAULT_I pin is Low active and all output channel shutdown except VBK
18	PGND	Power ground
19	VGH	VGH charge pump mode, for feedback voltage input for VGH charge pump regulator VGH boost mode, for feedback voltage input for VGH boost converter
20	DRVP/LXVGH	DRVP: VGH charge pump mode, for positive linear regulator base drive LXVGH: VGH boost mode, for switch node of the boost converter
21	PGND	Power ground
22	COMP	Compensation pin for AVDD Boost converter
23	GATE	External N MOSFET gate driver for AVDD external mode
24	LX/CS	LX: Switch node of the AVDD boost converter for AVDD internal mode CS: External current sense for AVDD external mode
25	SWI	Source input of the AVDD Boost converter isolation P MOSFET
26	SWG	Gate driver of the AVDD Boost converter External isolation P MOSFET
27	AVDD	Drain output of the AVDD Boost converter isolation P MOSFET and Feedback voltage input of the AVDD Boost converter

Pin Description(continued)

Pin#	Name	Description
28	HAVDD	Output of the AVDD OPAMP
29	HAFB/DAC	HAFB: Negative input of the HAVDD OPAMP VCOM2DAC: VCOM2 DAC output
30	VCOM1	VCOM1 operational amplifier output
31	INGMA	Supply voltage input of Gamma buffer and VCOM OP
32	GMA1	Gamma DAC analog output 1.
33	GMA2	Gamma DAC analog output 2.
34	GMA3	Gamma DAC analog output 3.
35	GMA4	Gamma DAC analog output 4.
36	GMA5	Gamma DAC analog output 5.
37	GMA6	Gamma DAC analog output 6.
38	GMA7	Gamma DAC analog output 7.
39	GMA8	Gamma DAC analog output 8.
40	GMA9	Gamma DAC analog output 9.
41	GMA10	Gamma DAC analog output 10.
42	GMA11	Gamma DAC analog output 11.
43	GMA12	Gamma DAC analog output 12.
44	GMA13	Gamma DAC analog output 13.
45	GMA14	Gamma DAC analog output 14.
46	PGND	Power ground
47	EPAD	Exposed pad. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation

Absolute Maximum Ratings (Note1)

VL,BKO to PGND ---------- -0.3V to +6V
LXBK to PGND ---------- -0.3V to INBK1+0.3V
INBK,INVGL to PGND ---------- -0.3V to +16.5V
DRVN/LXVGL to PGND ----------20V to INVGL+0.3V
DRVN/LXVGL to INVGL----------40V to +0.3V
VGL to PGND----------20V to +0.3V
VSS1 to PGND ----------20V to +0.3V
VGL to VSS1----------20V to +0.3V
DLOUT,SCL,SDA,EN/XAO,SHDN,FAULT to PGND ---------- -0.3V to +6V
VGH to PGND ----------0.3V to +50V
DRVP/LXVGH to PGND----------0.3V to +50V
COMP to PGND---------- -0.3V to +6V
GATE to PGND---------- -0.3V to +6V
LX/CS to GND ----------0.3V to +24V
LX/CS to SWI ----------0.3V to +24V
SWI to AVDD ----------0.3V to +24V
SWI,SWG,AVDD to PGND ----------0.3V to +24V
HAVDD, HAFB/VCOM2DAC to PGND ----------0.3V to +24V
INGMA to PGND ----------0.3V to +24V
VCOM1 to PGND ---------- -0.3V to INGMA+0.3V
GMA1-14 to PGND ---------- -0.3V to INGMA+0.3V
VGH to VGL,VSS1 ----------0.3V to +60V
AGND to PGND ----------0.3V to +0.3V

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2KV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ----------150℃
Operating Junction Temperature Range (TJ)---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec)----------260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- TBD℃/W
θ_{JC} (Junction-to-Case Thermal Resistance) ---------- TBD℃/W

Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	Def.	MAX	UNIT
V_{IN}	VIN Supply Range		8.6	12	14.7	V
	VIN Supply Range		4.3	5	6.0	V
V_{AVDD}	AVDD Output Range1	Step:100mV$_{REG\ 0x46[7]=0}$	13.0	17.6	19.8	V
	AVDD Output Range2	Step:100mV$_{REG\ 0x46[7]=1}$	11	15.1	17.3	V
V_{BK}	VBK Output Range	Step:50mV	1.8	3.3	3.35	V
V_{VGL}	VGL Output Range	Step:250mV	-18	-12	-3.0	V
V_{VSS}	VSS Output Range	Step:250mV	-16	-8	-3.0	V
V_{VGH}	VGH Output Range	Step:1.0V	20	30	42	V
V_{HAVDD}	HAVDD Output Range	Resolution:AVDD/512	192*Res4		319*Res4	V
V_{VCOM1}	VCOM1 Output Range	Resolution: (Vcom.max-vcom.min)/127	$V_{VCOM.MIN}$		Res1*127+ $V_{VCOM.MIN}$	V
$V_{VCOM2DAC}$	VCOM2DAC Output Range	Resolution: (Vcom.max-vcom.min)/127	$V_{VCOM.MIN}$		Res1*127+ $V_{VCOM.MIN}$	V
GMA1-14	GMA1-14 AVDD Range	AVDD/1024	0		V_{AVDD}/1024 *1023	V
VGH_{VTC2}	VGH&VGL VTC2	Step:0.2V	0.4	3.0	3.4	V
VGH_{VTC1}	VGH&VGL VTC1	Step:0.2V	0.4	2.0	3.4	V
$VCOM_{VTC2}$	VCOM VTC2	Step:0.2V	0.4	1.2	3.4	V
$VCOM_{VTC1}$	VCOM VTC1	Step:0.2V	0.4	0.6	3.4	V
V_{XAO}	XAO Discharge Threshold	Step:0.25V$_{REG\ 0x46h[7]=0}$	6.5	7.00	10.25	V
	XAO Discharge Threshold	Step:0.14V $_{REG\ 0x46h[7]=1}$	3.63	3.91	5.58	V

Power off discharge resistor

SYMBOL	PARAMETER	CONDITIONS	MIN	Def.	MAX	UNIT
R_{DIS_VBK}	VBK power off discharge resistor	0x2Ch[6]=0	0.4	0.5	0.6	KΩ
R_{DIS_VBK}	VBK power off discharge resistor	0x2Ch[6]=1	0.8	1.0	1.2	KΩ
R_{DIS_AVDD}	AVDD power off discharge resistor	0x2Ch[5]=0	1.1	1.4	1.7	KΩ
R_{DIS_AVDD}	AVDD power off discharge resistor	0x2Ch[5]=1	3.8	4.7	5.6	KΩ
R_{DIS_VGH}	VGH power off discharge resistor	0x2Ch[4]=0	1.2	1.5	1.8	KΩ
R_{DIS_VGH}	VGH power off discharge resistor	0x2Ch[4]=1	3.8	4.7	5.6	KΩ
R_{DIS_VGL}	VGL power off discharge resistor	0x2Ch[3]=1	8	10	12	KΩ
R_{DIS_HAVDD}	HAVDD power off discharge resistor	0x2Ch[2]=1	8	10	12	KΩ
R_{DIS_VCOM1}	VCOM1 power off discharge resistor	0x2Ch[1:0]=01	16	20	24	Ω
R_{DIS_VCOM1}	VCOM1 power off discharge resistor	0x2Ch[1:0]=10	0.8	1.0	1.2	KΩ
R_{DIS_VCOM1}	VCOM1 power off discharge resistor	0x2Ch[1:0]=11	6.4	8.0	9.6	KΩ
R_{DIS_VSS}	VSS power off discharge resistor	0x2Dh[7]=1	1.0	1.2	1.4	KΩ

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{IN}	Input Voltage Range	Reg [46h] bit7=0	8.6		14.7	V
	Input Voltage Range	Reg [46h] bit7=1	4.3		6.0	V
$I_{QVINBK1}$	Quiescent Current into V_{INBK1}	Switching		5	9	mA
$I_{QVINVGL}$	Quiescent Current into V_{INVGL}	Switching		1	2	mA
$I_{QVINGMA}$	Quiescent Current into V_{INGMA}	Switching		9	12	mA
I_{SLEEP}	Sleep on Quiescent Current into VIN	VL Shutdown		5	8	uA
VIN_{UVLO_R}	VIN under-voltage rising lockout Threshold Reg address=[46h] bit7=0	VIN rising	8.1	8.3	8.5	V
VIN_{UVLO_HYS}	VIN under-voltage hysteresis lockout Threshold Reg address=[46h] bit7=0	Hysteresis	700	800	900	mV
VIN_{UVLO_R}	VIN under-voltage rising lockout Threshold Reg address=[46h] bit7=1	VIN rising	4.1	4.2	4.3	V
VIN_{UVLO_HYS}	VIN under-voltage hysteresis lockout Threshold Reg address=[46h] bit7=1	Hysteresis	300	400	500	mV
V_L	VL Output Voltage	VIN=12V	4.9	5.0	5.1	V
FOSC1	VBK,AVDD,VGH,VGL Frequency1	REG 0x29h[7] = 0 Acuracy +/-10%	650	750	850	KHz
FOSC2	VBK,AVDD,VGH,VGL Frequency2	REG 0x29h[7] = 1 Acuracy +/-10%	450	500	550	KHz
FOSC3	VBK,AVDD,VGH,VGL Frequency3	REG 0x29h[6] = 1 Acuracy +/-10%	1100	1250	1400	KHz
T_{SD}	Thermal Shutdown Protection	Rising	140	150	160	℃
LOGIC						
V_{IH}	SDA/SCL/EN Input High Level		1.6			V
V_{IL}	SDA/SCL/EN Input Low Level				0.6	V
I_{IH},I_{IL}	SDA/SCL Input Leakage Current	V_I=0V or 3.3V	-1	0.01	+1	uA
R_{PD}	EN pull down resistor		320	400	480	KΩ
	Input Capacitance			5		pF
V_{OL}	SDA Output Low Voltage	I_{SINK}=6mA	0.3			V

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ASYNC. BOOST CONVERTER(AVDD)						
V_{AVDD1}	AVDD output voltage range1	Reg[46h] bit7=0	13.0		19.8	V
V_{AVDD2}	AVDD output voltage range2	Reg[46h] bit7=1	11		17.3	V
	SWO Output Accuracy	AVDD=17.6V, No load	-2		+2	%
$R_{DS(ON)}$	N-MOSFET ON Resistance	$I_{LX/CS}$=200mA		100	250	mΩ
$R_{DS(ON)}$	SYNC. P-MOSFET ON Resistance	I_O=200mA		0.6	1.0	Ω
GM	Transconductance			200		uA/V
R_{CS}	Current-sense Transresistance		0.15	0.25	0.35	Ω
I_{LIM}	N-MOSFET switch current limit	ILIMIT1 REG 0x00h[7]=0	5	6	7	A
		ILIMIT2 REG 0x00h[7]=1	2.5	3	3.5	A
SS_{AVDD}	Soft-start Period	Programmable softstart		10		ms
I_{LEAK}	Switch Leakage Current	$V_{LX/CS}$=20V		1	5	uA
V_{OVP}	SWI Over Voltage Protection	V_{SWI}Rising,hysteresis=1v	20.5	21.5	22.5	V
	AVDD Line Regulation	V_{IN}=8.6V to 14.7V I_{AVDD}=1mA		0.04		%/V
	AVDD Load Regulation	I_{AVDD}= 1mA to 1.5A	-1		+1	%/A
	AVDD UVP Fault Trip Level	V_{AVDD} Falling	80	85	90	%
	AVDD UVP fault timer duration			50		ms
V_{SC}	SWO Short Circuit Level	V_{AVDD} Falling	15	20	25	%
	Maximum Duty Cycle		85	90		%
V_{GOH}	Gate Output Hi-level			SWI		V
V_{GOL}	Gate Oput Low-level			SWI-6		V
R_{AVDD}	Gate pull-high resistor		8	10	12	KΩ
I_{G_SINK}	Gate Sink Current			8	15	uA
R_{SWO_DCHG}	Power off discharge resistance		3.8	4.7	5.6	KΩ
ISOLATION SWITCH						
	SWI supply voltage range		8		20	V
$R_{DS(ON)}$	Isolation PMOS switch on resistance	V_{SWI}=16.8V,I_{SW}=0.5A		200	250	mΩ
	Switch current		2	2.5	3	A
External N-MOSFET Gate Drvier(Gate of AVDD)						
V_{GATE_OH}	Gate High Voltage		4.5	5	5.5	V
V_{GATE_OL}	Gate Low Voltage		0		0.3	V
V_{CS_OCP}	External NMOS Switch Current Limit	R_{CS}=50mΩ	0.25	0.3	0.35	V
R_{DSON_GH}	Gate to VL High-Side On Resistance			5		Ω
R_{DSON_GL}	Gate to GND Low-side On Resistance			5		Ω

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ASYNC BOOST CONVERTER(VGH)						
V_{VGH_NT}	Adjustable Normal Temperature Output Voltage Range	Reg[03h],5bits/26 steps	20		42	V
V_{VGH_LT}	Adjustable Low Temperature Output Voltage Range	Reg[04h],5bits/26 steps	20		42	V
	Output voltage tolerance	VGH=30V, No Load.	-2		+2	%
$R_{DS(ON)}$	Low-side NMOS Switch on resistance			0.45	0.65	Ω
I_{LIMIT}	NMOS Switch Current Limit	ILIMIT1 REG 0x03h[7]=0	1.5	2	2.5	A
		ILIMIT2 REG 0x03h[7]=1	0.75	1	1.25	A
I_{LEAK}	NMOS Switch Leakage Current	V_{LXVGH}=45V		1	5	uA
	Line Regulation	V_{AVDD}=8.6V to 14.7V I_{GH}=0.1A		0.1		%/V
	Load Regulation	I_{GH}=1mA to 0.1A		0.3		%/A
T_{SS}	Soft-start Time	Programmable softstart		3		ms
	Output OVP Fault-Trip Level	V_{GH} rising, hysteresis:3V		45		V
	Output UVP Fault-Trip Level	V_{GH} falling	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	V_{GH} falling	15	20	25	%
R_{DIS}	Power off Discharge Resistance		24	30	36	KΩ
VGH CHARGE PUMP REGULATOR(VGH)						
V_{VGH_NT}	Adjustable Normal Temperature Output Voltage Range	Reg[03h],5bits/26 steps	20		42	V
V_{VGH_LT}	Adjustable Low Temperature Output Voltage Range	Reg[04h],5bits/26 steps	20		42	V
	Output voltage tolerance	VGH=30V, No Load.	-2		+2	%
	DRVP Leakage Current	V_{DRVP}=40V		1	5	uA
	DRVP Sink Current	VGH=27V	7	10	15	mA
	DRVP Short Circuit Current	V_{GH}<V_{GH}*20%		400		uA
	Line Regulation	V_{AVDD}=8.6V to 14.7V I_{GH}=0.1A		0.1		%/V
	Load Regulation	V_{DRVP}=10V, I_{DRVP}=50uA to 1mA		0.4		%
	Soft-start Time	Programmable softstart		3		ms
	Output OVP Fault-Trip Level	V_{GH} rising, hysteresis:1V	43	44	45	V
	Output UVP Fault-Trip Level	V_{GH} falling		80		%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	V_{GH} falling		20		%
R_{DIS}	Power off Discharge Resistance		24	30	36	KΩ

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGL INVERTING CONVERTER(VGL)						
V_{VGL_NT}	Adjustable Normal Temperature Output Voltage Range	Reg[05h], 5bits/31 steps	-18		-3	V
$V_{VGL\_LT/HT}$	Adjustable Low/High Temperature Output Voltage Range	Reg[06h], 5bits/31 steps	-18		-3	V
V_{VGL_OFFSET}	VGL_NT Output Offset	Reg[05h],bit7=1		-0.25		V
	Output Voltage Tolerance	VGL=-8.0V, No load.	-2		+2	%
	Maximum Duty Cycle		80	90		%
$R_{DS(ON)}$	PMOS Switch On-Resistance	I_{VGL_SW}=100mA		0.5	0.6	Ω
I_{LIMIT}	PMOS Switch Current Limit	ILIMIT1 REG 0x05h[6]=0	1.5	2.0	2.5	A
		ILIMIT2 REG 0x05h[6]=1	0.75	1.0	1.25	A
I_{LEAK}	PMOS Switch Leakage Current	V_{VGL_SW}=-16.0V		1	5	uA
	Line Regulation	V_{IN}=8.6V to 14.7V I_{GL}=0.1A		0.1		%/V
	Load Regulation	I_{GL}=1mA to 200mA		0.3		%/A
T_{SS}	Soft-start time			3		ms
	VGL Output OVP Fault-Trip Level	V_{GL} falling, hysteresis:110%	115	120	125	%
	VGL Output UVP Fault-Trip Level	V_{GL} rising	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	V_{GL} rising	15	20	25	%
R_{DIS}	Power off Discharge Resistance		8	10	12	KΩ
VGL CHARGE PUMP REGULATOR(VGL)						
V_{VGL_NT}	Adjustable Normal Temperature Output Voltage Range	Reg[05h], 5bits/31 steps	-18		-3	V
$V_{VGL\_LT/HT}$	Adjustable Low/High Temperature Output Voltage Range	Reg[06h], 5bits/31 steps	-18		-3	V
V_{VGL_OFFSET}	VGL_NT Output Offset	Reg[05h],bit7=1		-0.25		V
	Output Voltage Tolerance	VGL=-8.0V, No load.	-2		+2	%
	DRVN Leakage Current	V_{DRVN}=-16V		1	5	uA
	DRVN Source Current		10	20	30	mA
I_{DRVN_SC}	DRVN Short Circuit Current	V_{GL}>V_{GL}*20%		400		uA
T_{SS}	Soft-start Time			3		ms
	Output OVP Fault-Trip Level	V_{GL}falling,hysteresis:0.5v	115	120	125	%
	Output UVP Fault-Trip Level	V_{GL} rising	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	V_{GL} rising	15	20	25	%
R_{DIS}	Power off Discharge Resistance		8	10	12	KΩ

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSS1 NEGATIVE REGULATOR(VSS1)						
VSS1	Adjustable Output Voltage Range	Reg[07h], 5bits/27 steps	-16		-3	V
VSS_{OFFSET}	VSS Output Offset	Reg[07h],bit6=1		-0.25		V
	Output Voltage Tolerance	VSS1=-6.0V, No load.	-2		+2	%
I_{LIMIT}	Current Limit		50	100		mA
T_{SS}	Soft-start Time			3		ms
	Ouput UVP Fault-Trip Level	V_{SS1} falling	75	80	85	%
	UVP fault timer duration			50		ms
INL	Integral Nonlinearity	No load	-1		+1	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
	Load Regulation	I_{VSS1}=-50mA to 50mA		±0.5		mV/mA
R_{DIS}	Power off Discharge Resistance		1	1.2	1.4	KΩ
THERMAL COMPENSATION(VGH&VGL&VCOM1)						
VTC1	VGH&VGL lower bound voltage of VTC1	Reg[2Eh], 4bits/16 steps	0.4		3.4	V
VTC2	VGH&VGL upper bound voltage of VTC2	Reg[2Eh], 4bits/16 steps	0.4		3.4	V
$VCOM1_{VTC1}$	VCOM lower bound voltage of VTC1	Reg[2Fh], 4bits/16 steps	0.4		3.4	V
$VCOM1_{VTC2}$	VCOM upper bound voltage of VTC2	Reg[2Fh], 4bits/16 steps	0.4		3.4	V
SYNC BUCK CONVERTER(VBK)						
VBK	VBK Output Voltage Range	Reg[01h], 5bits/32 steps	1.8		3.35	V
	Output Voltage Tolerance	VBK=3.3V, No load.	-1		+1	%
	Maximum Duty Cycle		85	90		%
$R_{DS(ON)\_HS}$	High-side PMOS switch on resistance	I_{LXBK1}=500mA		400	600	mΩ
$R_{DS(ON)\_LS}$	Low-side NMOS switch on resistance	I_{LXBK1}=-500mA		200	400	mΩ
I_{LIMIT}	High-side PMOS switch current limit		2.0	2.5	3.0	A
I_{PEAK_HS}	High-side switch leakage current	V_{LXBK1}=0V		1	5	uA
I_{PEAK_LS}	Low-side switch leakage current	V_{LXBK1_SW}=14V		1	5	uA
	Line Regulation	V_{IN}=8.6V to 14.7V I_{VBK}=500mA		0.05		%/V
	Load Regulation	I_{VBK}=1mA to 2.0A	-1		+1	%
T_{SS}	Soft-start Time			3		ms
	Output OVP Fault-Trip Level	V_{VBK} rising	115	120	125	%
	Output UVP Fault-Trip Level	V_{VBK} falling	75	80	85	%
	UVP fault timer duration	V_{VBK} falling		50		ms
	Output SCP Fault-Trip Level		15	20	25	%
R_{DIS}	Power off Discharge Resistance		0.8	1	1.2	KΩ

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HAVDD OPAMP(HAVDD)						
	HAVDD voltage resolution			7		bits
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	HAVDD=1/2*AVDD No load	-2		+2	LSB
V_{OH}	Output voltage swing high	I_{HAVDD}=+100mA		V_{VAA}-2		V
V_{OL}	Output voltage swing low	I_{HAVDD}=-100mA		2	2.5	V
I_{OUT}	Output Continuous Current	HAVDD=1/2*AVDD	±200	±250	±300	mA
I_{SC}	Short Circuit Current		±50		±100	mA
CMRR	Input common-mode rejection ratio	AVDD=15V,f=10KHz 2V amplifude sin signal		80		dB
PSRR	Power supply rejection ratio	AVDD sweeps from 8V to 18V		60		dB
SR	Slew rate			45		V/us
BW	-3dB bandwidth			20		MHz
	Output OVP Fault-Trip Level	V_{HAVDD} rising	115	120	125	%
	Output UVP Fault-Trip Level	V_{HAVDD} falling	75	80	85	%
R_{DIS}	Power off Discharge Resistance			10		KΩ
GAMMA BUFFERS(GMA1 TO GMA14)						
V_{SWO_GMA}	Supply Range		11		19.8	V
	Gamma Voltage Resolution	GMA1 to 14, 10bits/1024 steps		V_{AVDD}/ 1024		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	GMA=1/2 code No load	-2		+2	LSB
$V_{GMA1-14}$	Output Voltage Range	$I_{GMA1\ to\ 14}$ =sinking or source 5mA	GND +0.2		V_{AVDD} -0.2	V
I_{OUT}	Output Current (setting 14ch gma)	$V_{GMA1\ to\ 14}$ drop 0.5V	±50	±75	±100	mA
I_{SC}	Short Circuit Current (setting 14ch gma)	$V_{GMA1\ to\ 14}$ to V_{SWO_GMA} or $V_{GMA1\ to\ 14}$ to GND	±10	±20	±30	mA
I_{OUT}	Output Current (1,7,8,14 4ch)	$V_{GMA1\ to\ 14}$ drop 0.5V	±100	±150	±200	mA
I_{SC}	Short Circuit Current (1,7,8,14 4ch)	$V_{GMA1\ to\ 14}$ to V_{SWO_GMA} or $V_{GMA1\ to\ 14}$ to GND	±20	±40	±60	mA
T_{D_GMA}	Program to Output Delay	From ACK falling edge to programming gamma change 50% voltage at output		15		us
	Load Regulation	$I_{GMA1\ to\ 14}$=-12mA to 12mA		±0.5+ Rd		mV/ mA

Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCOM1 BUFFERS & VCOM2 DAC(VCOM1&VCOM2)						
V_{SWO_GMA}	Supply Range		11		19.8	V
V_{VCOM1_NT}/ $V_{VCOM2DAC}$	Adjustable Normal Temperature Output Voltage Range	Reg[08h], 7bits/128 steps Res1=(vcom.max-vcom.min)/127	0*res1+vcom.min		127*res1+vcom.min	V
V_{VCOM1_HT}	Adjustable Low Temperature Output Voltage Range	Reg[09h], 7bits/128 steps Res1=(vcom.max-vcom.min)/127	0*res1+vcom.min		127*res1+vcom.min	V
V_{VCOM_MAX}	Adjustable VCOM_MAX	Reg[0Ah],7bits/128 steps	1*V_{AVDD}/128		128*V_{AVDD}/127	V
$V_{VCOMMIN}$	Adjustable VCOM_MIN	Reg[0Bh],7bits/128 steps	0*V_{AVDD}/128		127*V_{AVDD}/127	V
	VCOM1&VCOM2DAC voltage resolution	VCOM1&VCOM2DAC will be clamped between vcom.max and vcom.min		V_{AVDD}/128		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	No load	-2		+2	LSB
V_{VCOM1} $V_{VCOM2DAC}$	Output Voltage Range	VCOM1&VCOM2DAC will be clamped between vcom.max and vcom.min	GND +0.5		V_{AVDD} -0.5	V
T_{D_VCOM1} $T_{D\_VCOM2DAC}$	Program to Output Delay	From ACK falling edge to programming VCOM change 50% voltage at output		1		us
I_{OUT}	VCOM1 Output Continuous Current		±200	±250	±300	mA
I_{SC}	VCOM1 Short Circuit Current		±50		±100	mA
	Load Regulation	I_{VCOM1}=-100mA to 100mA	-1		+1	mV/mA
R_{DIS}	Power off Discharge Resistance	Reg[2Ch], 2bits/4 steps	dis		8	KΩ
FAULT SIGNAL(FAULT)						
R_{FAULT}	FAULT Pull Up Resistance	Up to VL(VBK ok detect)	80	100	120	KΩ
V_{FAULT_HIV}	FAULT High Level Input Voltage		2			V
V_{FAULT_LIV}	FAULT Low Level Input Voltage				1	V
	FAULT ON Voltage	I_{IN}=3mA			0.5	V

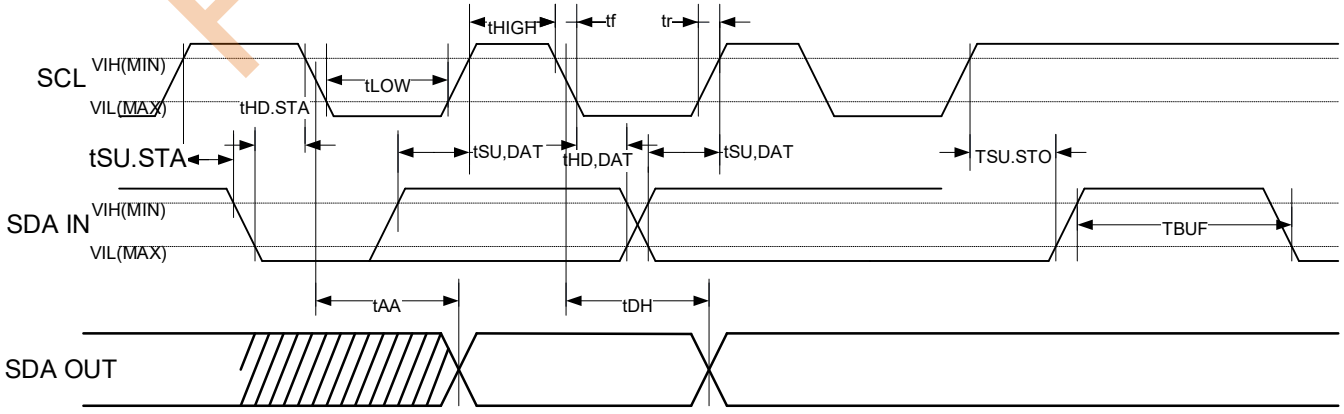
Electrical Characteristics

(V_{IN} = 12V, V_{AVDD} = 16V, V_{BK} = 3.3V, V_{HAVDD} = 8V, V_{VGH} = 28V, V_{VGL} = -10V, V_{VSS1} = -6V with typical values T_A=25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

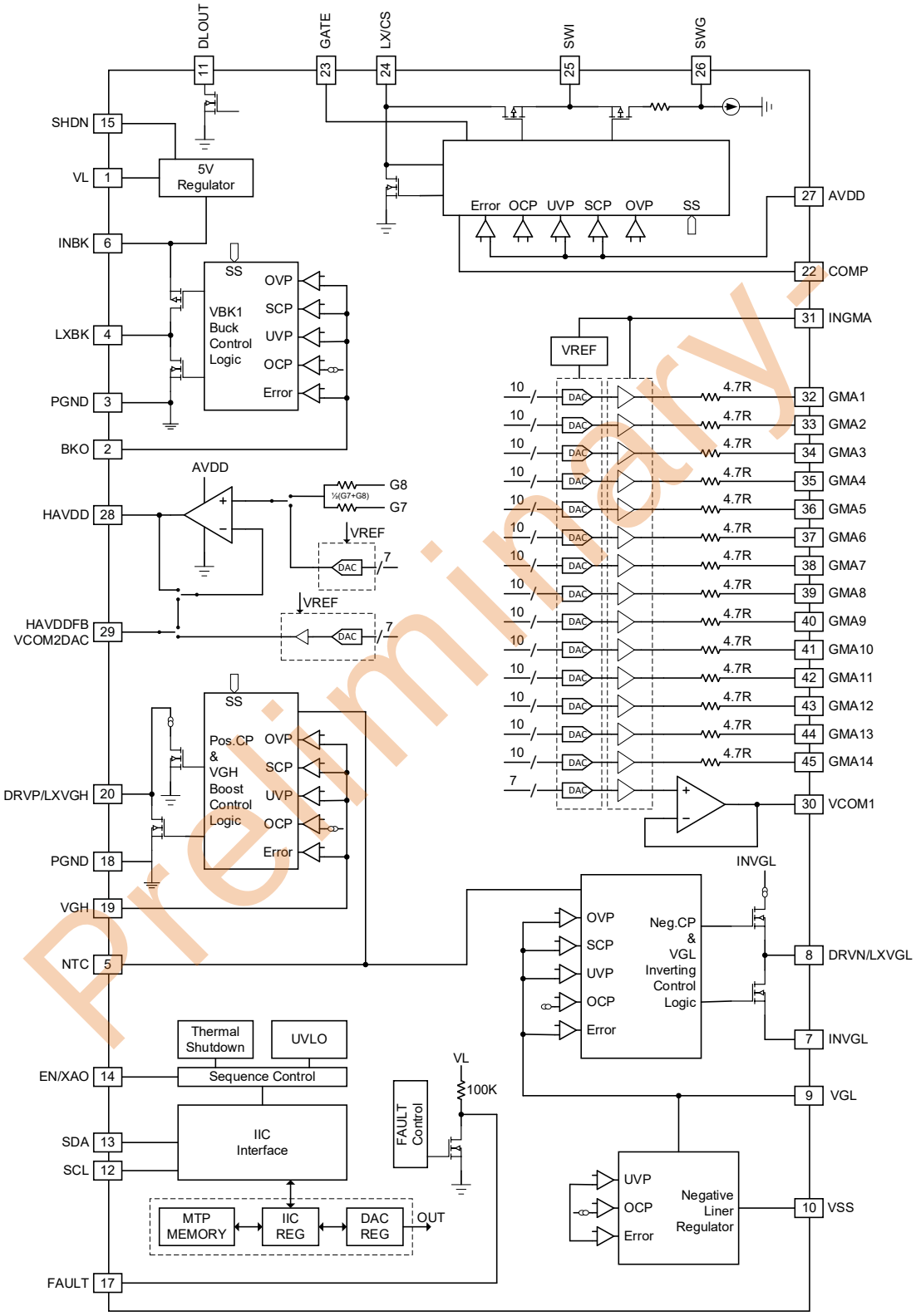
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IIC INTERFACE(SDA,SCL)						
V_{IH}	High Level Input Voltage		1.6	---	---	V
V_{IL}	Low Level Input Voltage		---	---	0.5	V
IIC TIMING CHARCTERISTICS						
F_{SCL}	Serial-Clock Frequency		10	---	400	KHz
T_{BUF}	Bus Free Time Between STOP and START Conditions		1300	---	---	nS
$T_{HD.STA}$	Hold Time(Repeated) START Condition		600	---	---	nS
T_{LOW}	SCL Pulse-Width Low		1300	---	---	nS
T_{HIGH}	SCL Pulse-Width High		600	---	---	nS
$T_{SU.STA}$	Setup Time for a Repeated START Condition		600	---	---	nS
$T_{HD.DAT}$	Data Hold Time		50	---	800	nS
$T_{SU.DAT}$	Data Setup Time		100	---	---	nS
T_R	SDA and SCL Receiving Rise Time	CB is IN pF	20+ 0.1CB	---	300	nS
T_F	SDA and SCL Receiving Fall Time	CB is IN pF	20+ 0.1CB	---	300	nS
CIN	SDA and SCL Input Capacitance			---	400	pF
$T_{SU.STO}$	Setup Time for STOP Condition		600	---	---	nS
TAA	Clock Low to Data Out Valid		100	---	900	nS
	MTP start up Blanking Time			30	40	ms
	Program MTP Blanking Time			45	60	ms
	Read MTP Blanking Time			1.5	5	ms

I2C Serial-Interface

The LP6262QVF communicates through an industry standard 2-wire I2C serial-interface to receive data in slave mode. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. A master device, usually a microcontroller or a digital signal processor, controls the bus.

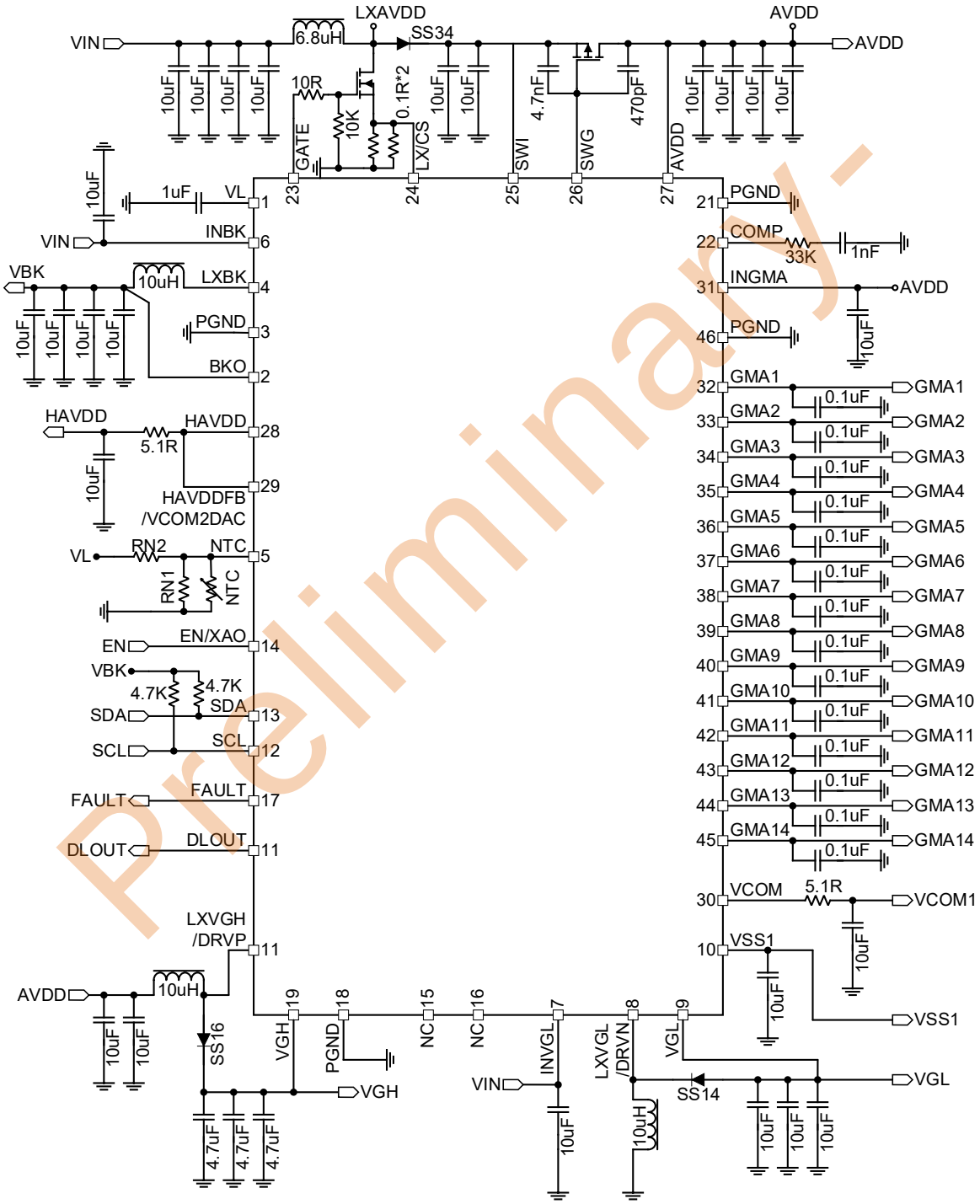


Functional Block Diagram



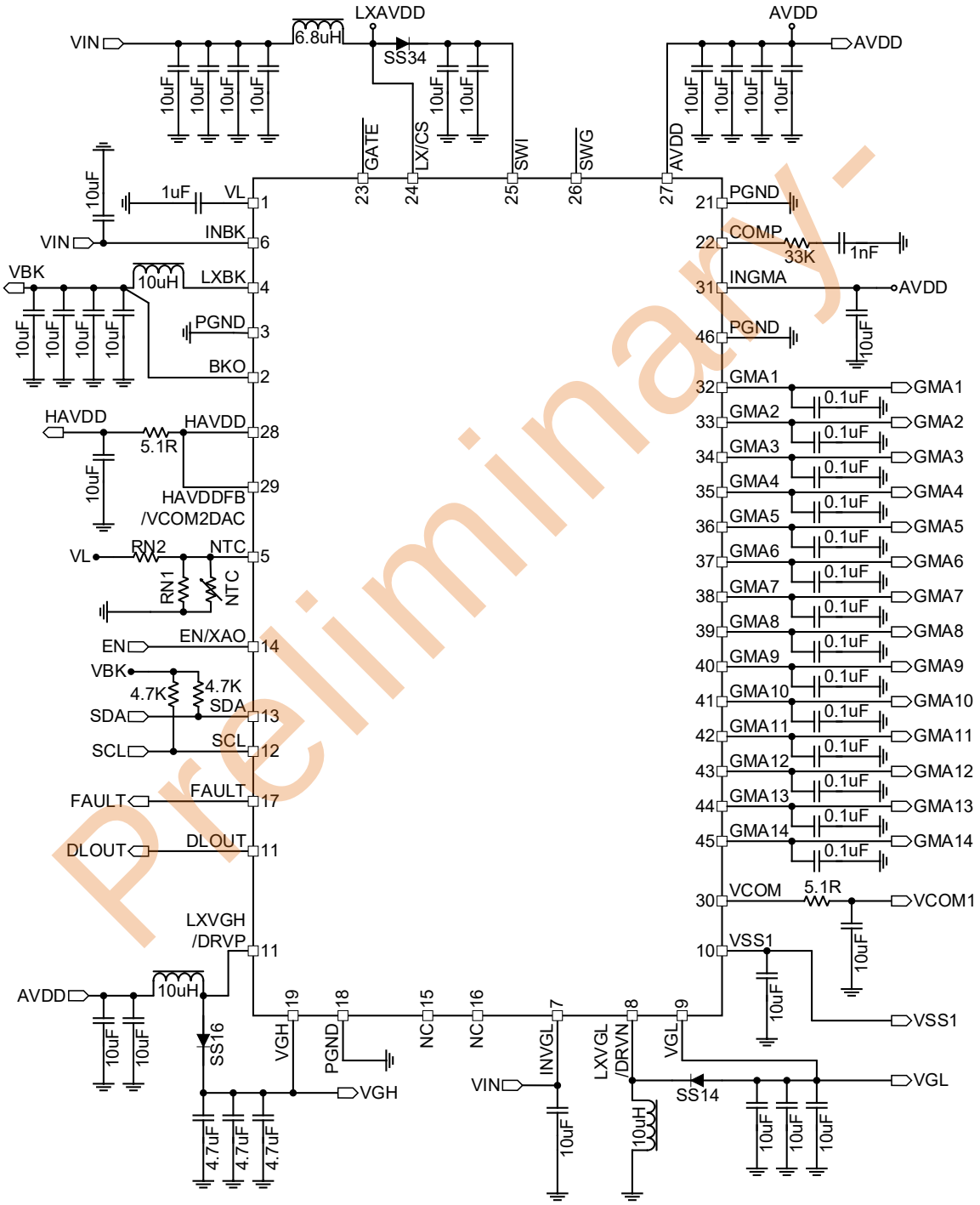
Typical Application Circuit_1

Channel	Type Selection
AVDD Converter	Boost Controller
AVDD Isolation Switch	External ISO-PMOS Switch
VGH	Boost Converter
VGL	Buck-Boost Converter



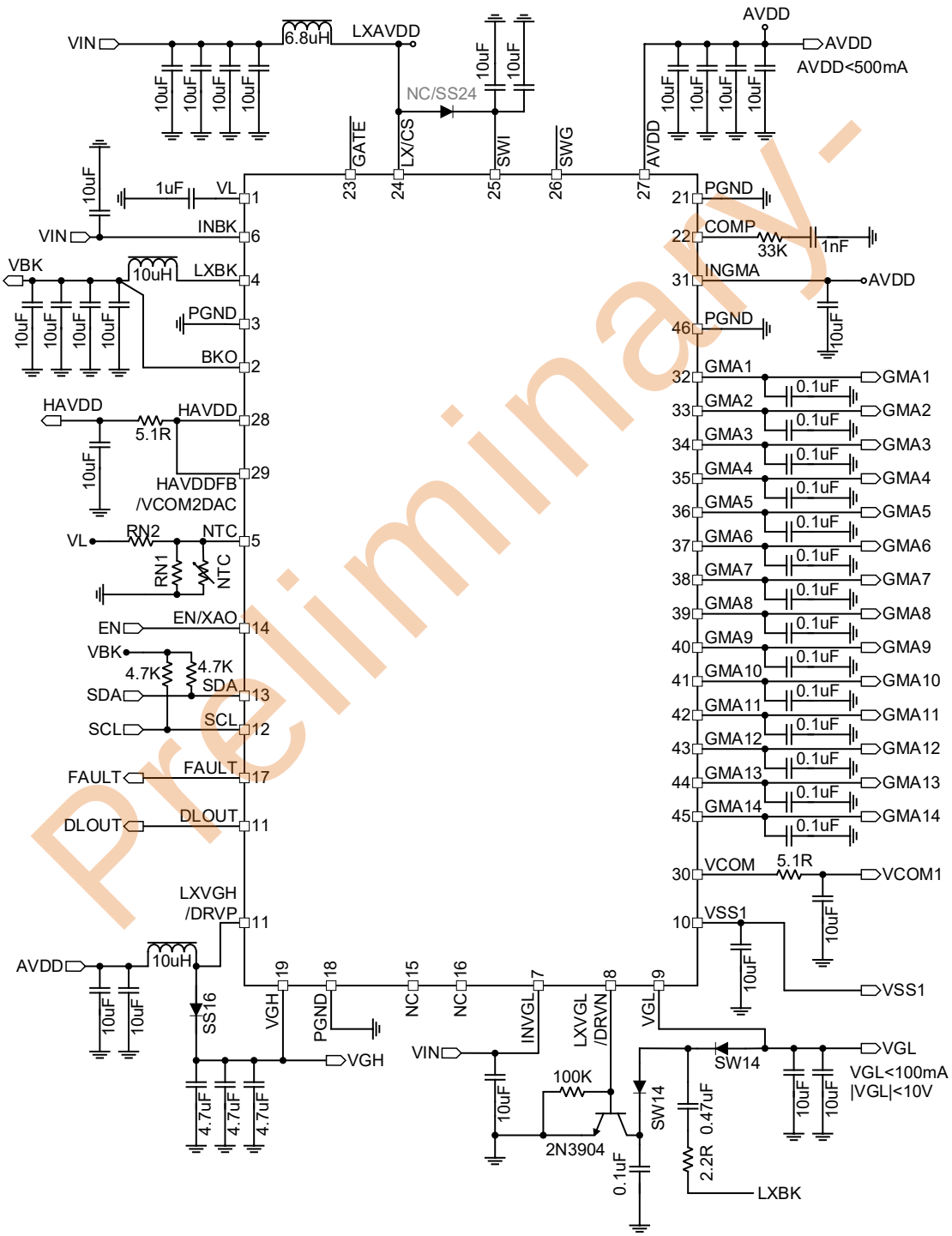
Typical Application Circuit_2

Channel	Type Selection
AVDD Converter	Boost Converter Internal power MOS
AVDD Isolation Switch	Internal ISO-PMOS Switch
VGH	Boost Converter
VGL	Buck-Boost Converter

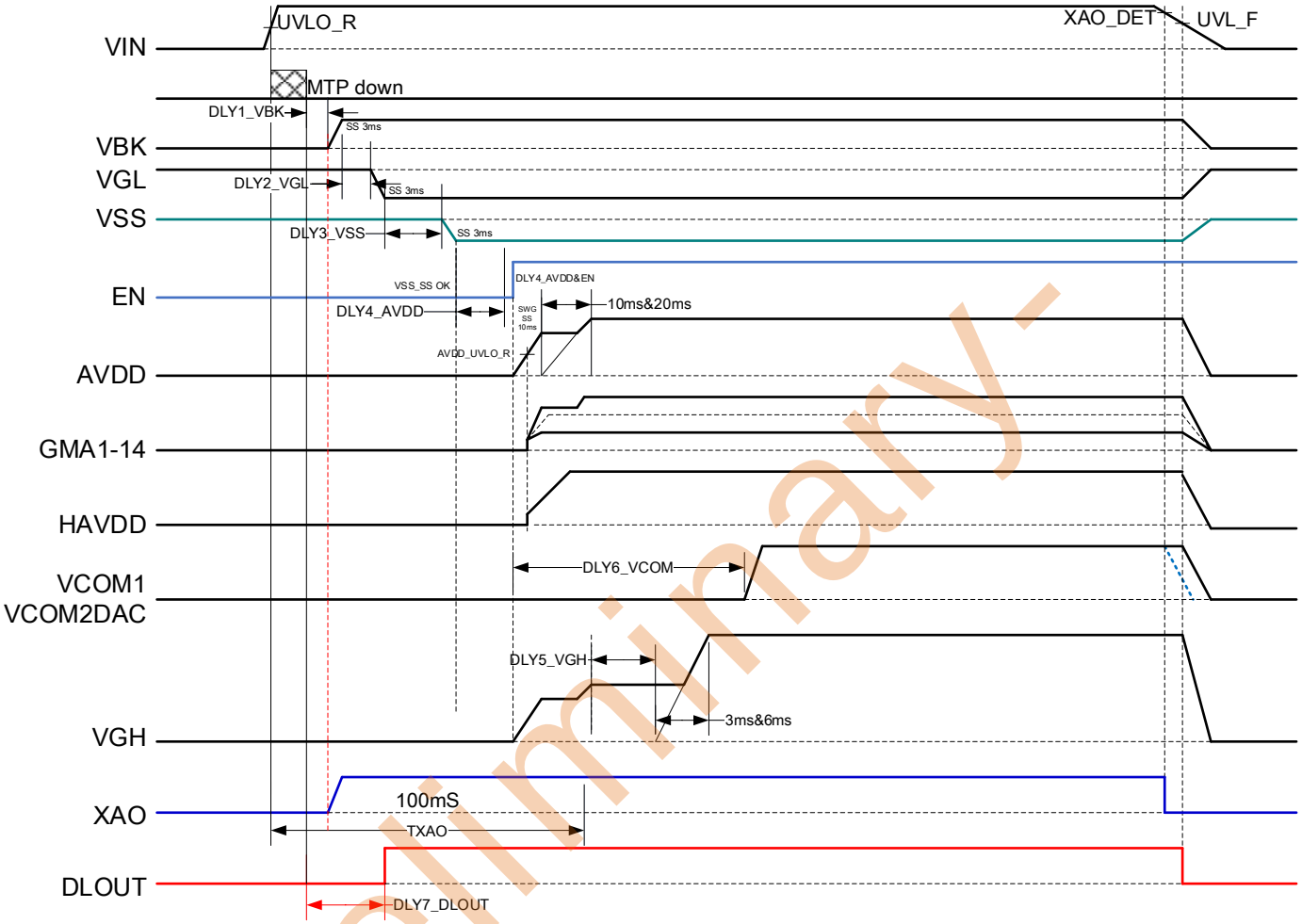


Typical Application Circuit_3

Channel	Type Selection
AVDD Converter	Boost Converter Internal power MOS
AVDD High-side SYNC PMOS	Internal SYN PMOS
AVDD Isolation Switch	Internal ISO-PMOS Switch
VGH	Boost Converter
VGL	Charge Pump and Pump source LXBK



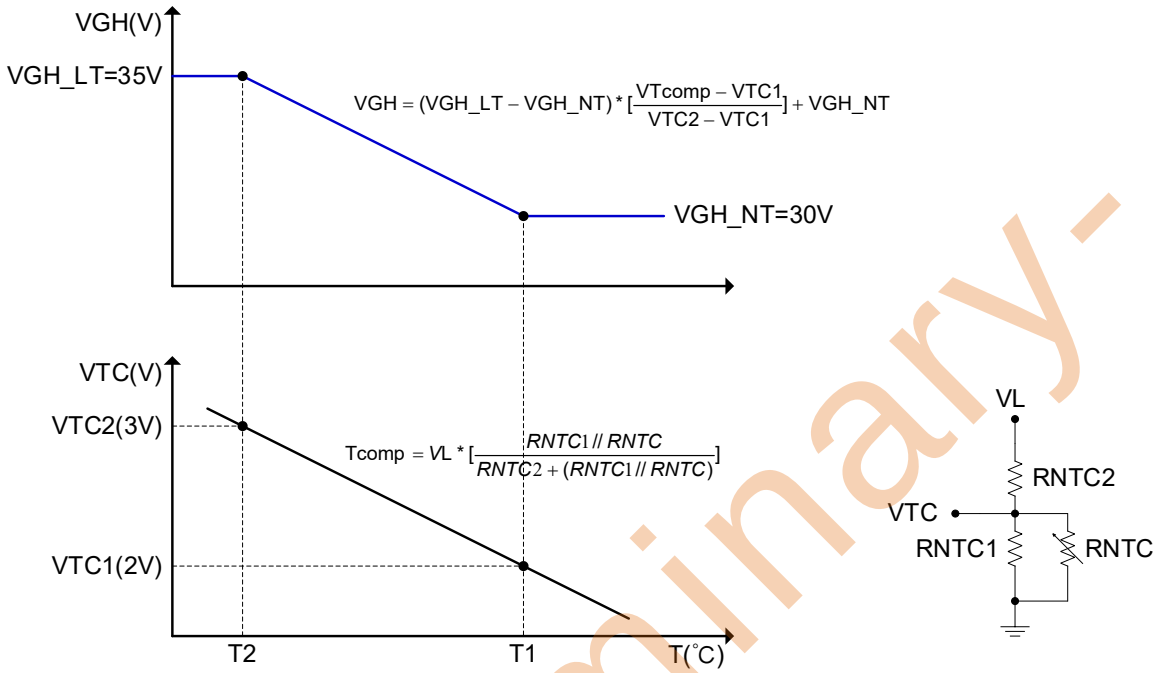
Timing Diagram



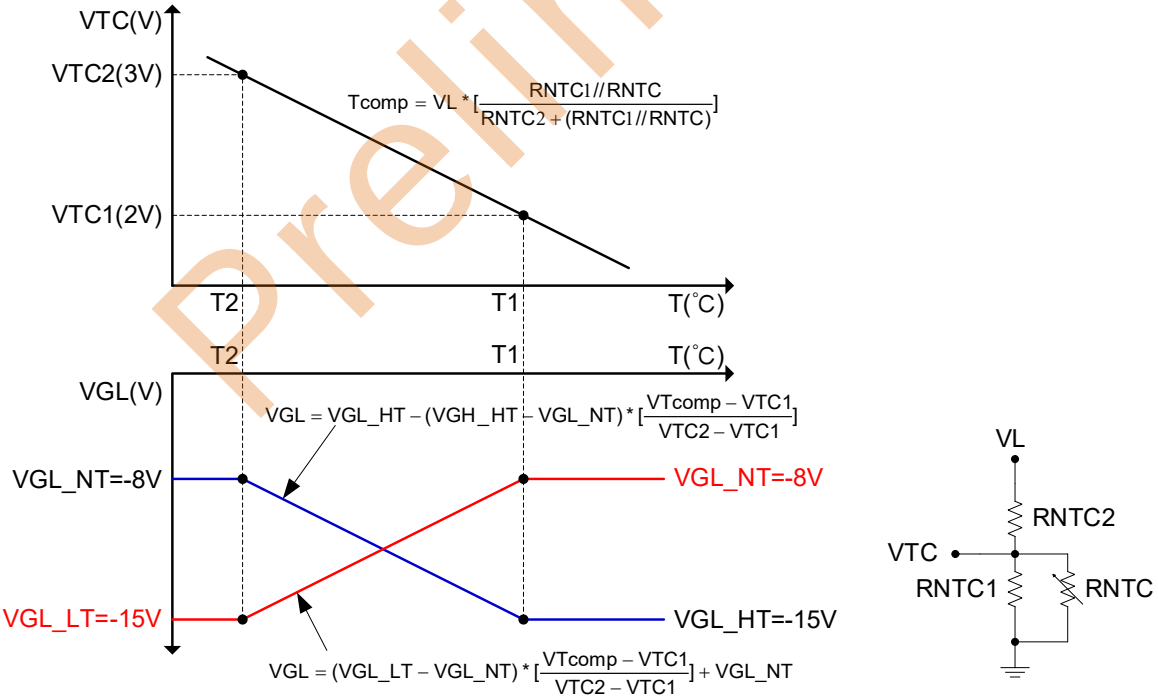
Temperature Compensation Function

VGH, VGL and VCOM channel can be temperature compensated,allowing its output voltage to transition which monitor NTC voltage connected a NTC(Negative Temperature Coefficient) Resistor to GND (see Figures 1). VTC1 and VTC2 defines the high/low boundary Voltage as VNTC variation.

VGH temperature compensation curve

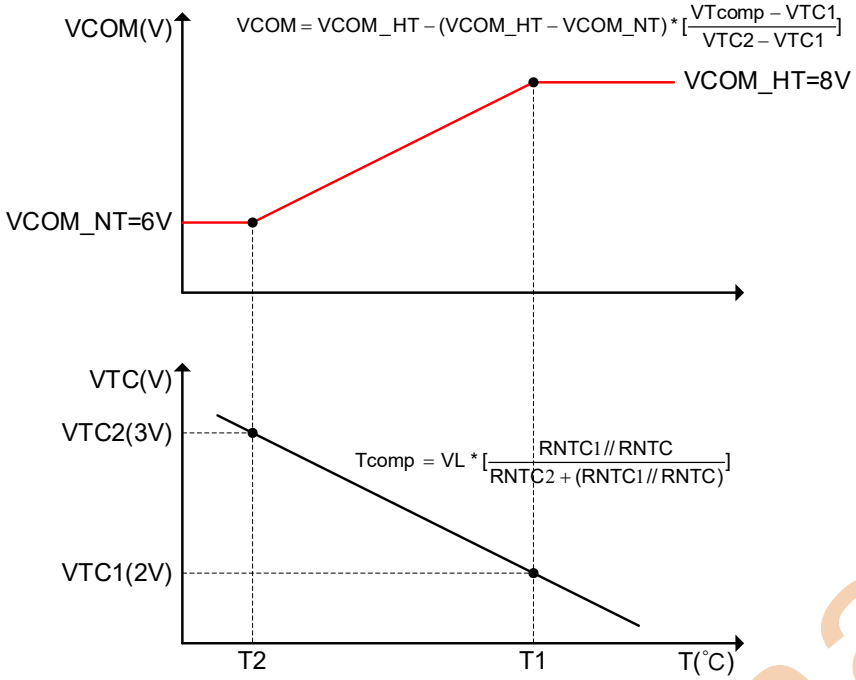


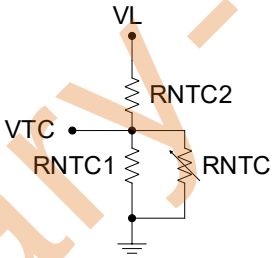
VGL temperature compensation curve



C Curve is negative temperature compensation
D Curve is positive temperature cimpensation

VCOM1 temperature compensation curve





Device Address Setting

PMIC Slave Address

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Write Address	Read Address
0	1	0	0	0	0	0	R/W	0x40	0x41

Only for VCOM1_NT Device slave Address (0x2Bh[7]=0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Write Address	Read Address
1	1	1	0	1	0	0	R/W	0xE8	0xE9

Only for VCOM1_NT Device slave Address (0x2Bh[7]=1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Write Address	Read Address
1	1	1	0	1	0	1	R/W	0xEA	0xEB

Control Byte Define:

Register Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
0xFF	[7:0] Control Register								00 : Read data from DAC register 01 : Read data from MTP 40 : Write VCOM1 data from DAC to MTP 80 : Write all DAC into MTP

PMIC IIC Command Device address (40h/41h)

1. Write single byte of data to DAC register Example: Write Address 07h

Start	01000000(Slave ID)	Slave ACK	00000111(Register)	Slave ACK	Data 07h	Slave ACK	Stop

2. Write multiple byte of data to DAC register Example: Write Address 00h~0Fh

Start	01000000(Slave ID)	Slave ACK	00000000(Register)	Slave ACK	Data 00h	Slave ACK

Data 01h	Slave ACK	……	Slave ACK	Data 0Fh	Slave ACK	Stop

3. Write All DAC Register into EEPROM

Start	01000000(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	10000000(Control Data)	Slave ACK	Stop

4. Write VCOM1 Data Register into EEPROM

Start	01000000(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	01000000(Control Data)	Slave ACK	Stop

5. Read single byte of data from DAC register

Start	01000000(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000000(Control Data)	Slave ACK	Stop

Start	01000000 (Slave ID)	Slave ACK	00000000 (Data Address)	Slave ACK	Start	01000001 (Slave ID)	Slave ACK	Data 00h	Master ACK	Stop

6. Read data from DAC register Example: Reading Register Address 00h~0Fh

Start	01000000(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000000(Control Data)	Slave ACK	Stop

Start	01000000(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK

Start	01000001(Slave ID)	Slave ACK	Data 00h	Master ACK	Data 01h	Master ACK

……	Master ACK	Data 0Fh	Master N-ACK	Stop

7. Read single byte of data from MTP

Start	01000000(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000001(Control Data)	Slave ACK	Stop

Start	01000000 (Slave ID)	Slave ACK	00000000 (Data Address)	Slave ACK	Start	01000001 (Slave ID)	Slave ACK	Data 00h	Master ACK	Stop

8. Read data from MTP Example: Reading Data from MTP Address 00h~0Fh

Start	01000000(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000001(Control Data)	Slave ACK	Stop

Start	01000000(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK

Start	01000001(Slave ID)	Slave ACK	Data 00h	Master ACK	Data 01h	Master ACK

……	Master ACK	Data 0Fh	Master NACK	Stop

Only VCOM1_NT IIC Command Device address (E8h/E9h or EAh/EBh)

1. Load VCOM1_NT MTP data to DAC register(RESET)

Start	11101000(Slave ID)	Slave ACK	00000000(REG ADDR)	Slave ACK	01000000(Control Data)	Slave ACK	Stop

2. Write VCOM1_NT DAC register into MTP (VCOM_NT_WR_MTP)

Start	11101000(Slave ID)	Slave ACK	00000000(REG ADDR)	Slave ACK	00001000(Control Data)	Slave ACK	Stop

3. Set VCOM1 output enable=1(OUT_EN)

Start	11101000(Slave ID)	Slave ACK	00000000(REG ADDR)	Slave ACK	00000010(Control Data)	Slave ACK	Stop

4. Write VCOM1_NT data to DAC register

Start	11101000(Slave ID)	Slave ACK	00000001(REG ADDR)	Slave ACK	Data 01h	Slave ACK	Stop

5. Read VCOM1_NT byte of data from DAC register

Start	11101000 (Slave ID)	Slave ACK	00000001 (Data Address)	Slave ACK	Start	11101001 (Slave ID)	Slave ACK	Data 01h	Master ACK	Stop

6. Read Fault Status byte of data from DAC register

Start	11101000 (Slave ID)	Slave ACK	00000002 (Data Address)	Slave ACK	Start	11101001 (Slave ID)	Slave ACK	Data 02h	Master ACK	Stop

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1_NT Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x00h (29h)	[7] AVDD Switching Limit	$AVDD_{LIMIT}$	0: 5A(MIN.) 1: 2.5A(MIN.)		0: 5A
	[6] AVDD Output voltage offset	AVDD_F	0: 0V(by 0x00h[5:0] setting) 1: -0.5V		0: 0V
	[5:0] AVDD output voltage	AVDD	@[46h] bit7=0 13.5V(00h) to 19.8V(3Fh) @[46h] bit7=1 11V(00h) to 17.3V(3Fh)	0.1V	17.6V(29h)
0x01h (1Eh)	[4:0] VBK output voltage	VBK	1.8V(00h) to 3.35V(1Fh)	0.05V	3.3V(1Eh)
0x02h (40h)	[6:0] HAVDD output voltage	HAVDD	Res2*(0+192)(00h) to Res2*(127+192)(7Fh) Res2=AVDD/512	AVDD/512	Res2*(64+192) (40h)
0x03h (0Ah)	[7] VGH Switching Limit	VGH_{LIMIT}	0: 1.5A(MIN.) 1: 0.75A(MIN.)		0: 1.5A
	[4:0] VGH normal temperature voltage	VGH_NT	20V(00h) to 42V(16h)	1V	30V(0Ah)
0x04h (0Fh)	[7] VGH low temperature enable	VGH_LT_EN	0: Disable 1: Enable		0: Disable
	[4:0] VGH low temperature voltage	VGH_LT	20V(00h) to 42V(16h)	1V	35V(0Fh)
0x05h (0Ah)	[7] VGL normal temperature Voltage offset	VGL_OFFSET	0: Disable 1: -0.25V		0: Disable
	[6] VGL Switching Limit	VGL_{LIMIT}	0: 1.5A(MIN.) 1: 0.75A(MIN)		0: 1.5A
	[4:0] VGL normal temperature voltage	VGL_NT	-3V(00h) to -18V(1Eh)	0.5V	-8V(0Ah)
0x06h (12h)	[7] VGL temperature compensation enable	VGL_LT/HT_EN	0: Disable 1: Enable		0: Disable
	[6] VGL low or high temperature Compensation selection	VGL_LT/HT_SEL	0: VGL_LT 1: VGL_HT		0: VGL_LT
	[4:0] VGL low/high temperature voltage	VGL_LT/HT	-3V(00h) to -18V(1Eh)	0.5V	-12V(12h)
0x07h (06h)	[7] VCOM1 high temperature Enable	VCOM1_HT_EN	0: Disable 1: Enable		0: Disable
	[6] VSS1 output voltage offset	VSS1_OFFSET	0: Disable 1: -0.25V		0: Disable
	[4:0] VSS1 output voltage	VSS1	-3V(00h) to -16V(1Ah)	0.5V	-6V(06h)
0x08h (7Eh)	[7:1] VCOM1 normal Temperature voltage	VCOM1_NT	VCOM.MIN to VCOM.MAX Res1=(vcom.max-vcom.min)/127	Res1	63*Res1+vcom.min (7Eh)
0x09h (BAh)	[7:1] VCOM1 high temperature Voltage	VCOM1_HT	VCOM.MIN to VCOM.MAX Res1=(vcom.max-vcom.min)/127	Res1	93*Res1+vcom.min (BAh)
0x0Ah (3Fh)	[6:0] VCOM1&VCOM2DAC High limit voltage	VCOM_MAX	1*Res3(00h) to 128*Res3(7Fh) Res3=VAVDD/128	Res3	64*Res3 (3Fh)
0x0Bh (26h)	[6:0] VCOM1&VCOM2DAC Low limit voltage	VCOM_MIN	0*Res3(00h) to 127*Res3(7Fh) Res3=VAVDD/128	Res3	38*Res3 (26h)

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1_NT Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x0Ch 0x0Dh	[9:0] Gamma1 output voltage	GAMMA1	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x0Eh 0x0Fh	[9:0] Gamma2 output voltage	GAMMA2	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x10h 0x11h	[9:0] Gamma3 output voltage	GAMMA3	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x12h 0x13h	[9:0] Gamma4 output voltage	GAMMA4	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x14h 0x15h	[9:0] Gamma5 output voltage	GAMMA5	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x16h 0x17h	[9:0] Gamma6 output voltage	GAMMA6	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x18h 0x19h	[9:0] Gamma7 output voltage	GAMMA7	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x1Ah 0x1Bh	[9:0] Gamma8 output voltage	GAMMA8	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x1Ch 0x1Dh	[9:0] Gamma9 output voltage	GAMMA9	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x1Eh 0x1Fh	[9:0] Gamma10 output voltage	GAMMA10	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x20h 0x21h	[9:0] Gamma11 output voltage	GAMMA11	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x22h 0x23h	[9:0] Gamma12 output voltage	GAMMA12	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x24h 0x25h	[9:0] Gamma13 output voltage	GAMMA13	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x26h 0x27h	[9:0] Gamma14 output voltage	GAMMA14	0V(000h) to VAVDD(3FFh) Res4=VAVDD/1024	Res4	512*Res4 (200h)
0x28h (7Fh)	[7] Group B Enable (Group B: AVDD, HAVDD, VGH, VGL, VSS1, PGMA, VCOM1, VCOM2DAC)	Group_B_EN	0: Disable 1: Enable		0: Disable
	[6] VGL enable	VGL_EN	0: Disable 1: Enable		1: Enable
	[5] VSS1 enable	VSS1_EN	0: Disable 1: Enable		1: Enable
	[4] AVDD enable	AVDD_EN	0: Disable 1: Enable		1: Enable
	[3] HAVDD enable	HAVDD_EN	0: Disable 1: Enable		1: Enable
	[2] Gamma enable	GMA_EN	0: Disable 1: Enable		1: Enable
	[1] VCOM1 enable	VCOM1_EN	0: Disable 1: Enable		1: Enable
	[0] VGH enable	VGH_EN	0: Disable 1: Enable		1: Enable

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1_NT Device Address: 0xE8h or 0xEAh

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x29h (00h)	[7] Frequency select (VBK,AVDD,VGH,VGL)	FREQ_SEL1	0: 750KHz 1: 500KHz		0: 750KHz
	[6] Frequency select (VBK,AVDD,VGH,VGL)	FREQ_SEL2	0: 0x29h[7] setting 1: 1250KHz		0: 0x29h[7]
	[5] Isolation PMOS Internal or External select	ISO_PMOS INT/EXT	0: External 1: Internal		0: External
	[4] AVDD NMOS_Internal or External select	AVDD_MOS _INT/EXT	0: Internal 1: External @[29h] bit3 output keep boost and bit1 output keep LXBK1		0: Internal
	[3] VGH structure type	VGH_TYPE	0: Boost 1: Charge pump (AVDD internal only)		0: Boost
	[2] VGL structure type	VGL_TYPE	0: Inverting Buck-Boost 1: Charge pump AVDD internal or AVDD External@[29h] bit1 keep LXBK1 only		0: Inverting
	[1] VGL charge pump source	VGL_PUMP _SOURCE	0: LXBK1 1: LX/CS		0: LXBK1
	[0] Gamma channel type	GMA_CH_ TYPE	0: 14_CH(1 to 14_CH) 1: 4_CH(1,7,8,14_CH) Other channel Hiz		0: 14_CH
0x2Ah (05h)	[7:6] Delay7_DLOUT	DLY7_DLO	00(0ms) to 11(6ms)	2ms	00: 0ms
	[5:4] Delay1_VBK	DLY1_VBK	@[46h] bit7=0,00(0ms) to 11(6ms) bit7=1,00(0ms)to11(120ms)	bit7=0,2ms bit7=1,40ms	00: 0ms
	[3:2] Delay2_VGL	DLY2_VGL	00(0ms) to 11(15ms)	5ms	01: 5ms
	[1:0] Delay3_VSS1	DLY3_VSS1	00(0ms) to 11(6ms)	2ms	01: 2ms
0x2Bh (28h)	[7] ADJ E8h/EAh address	ADJ_ADDR	0: E8/E9 address 1: EA/EB address		0: E8/E9
	[6:5] Delay4_AVDD	DLY4_AVDD	00(0ms) to 11(15ms)	5ms	01: 5ms
	[4:3] Delay5_VGH	DLY5_VGH	00(0ms) to 11(6ms)	2ms	01: 2ms
	[2:0] Delay6_VCOM1/2DAC	DLY6_VCOM	000(0ms) to 111(210ms)	30ms	000: 0ms
0x2Ch (FFh)	[7] All discharge enable	ALL_DIS_EN	0: Disable 1: Enable		1: Enable
	[6] Buck1 discharge	BK1_DIS	0: 0.5KΩ 1: 1KΩ		1: 1KΩ
	[5] AVDD discharge	AVDD_DIS	0: 1.4KΩ 1: 4.7KΩ		1: 4.7KΩ
	[4] VGH discharge	VGH_DIS	0: 1.5KΩ 1: 30KΩ		1: 30KΩ
	[3] VGL discharge enable	VGL_DIS	0: Disable 1: 10KΩ		1: 10KΩ
	[2] HAVDD discharge enable	HAVDD_DIS	0: Disable 1: 10KΩ		1: 10KΩ
	[1:0] VCOM1 discharge enable	VCOM1_DIS	00: Disable 01: 20Ω 10: 1KΩ 11: 8KΩ		11: 8KΩ

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1_NT Device Address: 0xE8h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x2Dh (85h)	[7] VSS1 discharge enable	VSS1_DIS	0: Disable 1: 1.2KΩ		1: 1.2KΩ
	[4] VCOM1 delay power off1	VCOM1_DLY_OFF1	0: VIN_UVLO_F 1: XON discharge threshold		0: VIN_UVLO_F
	[3] HAVDD feedback mode Select	HAVDD_FB	0: (G7+G8)/2 1: HAVDD DAC register		0: (G7+G8)/2
	[2] AVDD GDMOS SCP Select	AVDD_GD_SCP	0: GD_SC_Mode1 Power up of three fail attempts And AVDD FIMV1 detect 1: GD_SC_Mode2 Power Up of three fail attempts And AVDD FIMV2 detect		1: GD_SC_2
	[1] AVDD soft start	AVDD_SS	0: 10ms 1: 20ms		0: 10ms
	[0] VGH soft start	VGH_SS	0: 3ms 1: 6ms		1: 6ms
0x2Eh (D8h)	[7:4] VGH&VGL_VTC2	VGH_VTC2	0000(0.4V) to 1111(3.4V)	0.2V	1101: 3.0V
	[3:0] VGL&VGL_VTC1	VGH_VTC1	0000(0.4V) to 1111(3.4V)	0.2V	1000: 2.0V
0x2Fh (41h)	[7:4] VCOM1_VTC2	VCOM_VTC2	0000(0.4V) to 1111(3.4V)	0.2V	0100: 1.2V
	[3:0] VCOM1_VTC1	VCOM_VTC1	0000(0.4V) to 1111(3.4V)	0.2V	0001: 0.6V
0x30h (1Ah)	[5:4] AVDD external driving Of gate	AVDD_EXT_DRV	00: EXT_DRV1_FF 01: EXT_DRV2_F 10: EXT_DRV3_S 11: EXT_ERV4_SS		01: EXT_DRV2_F
	[3:2] VGH boost converter Compensation	VGH_Boost_COMP	00: VGH_COMP1_FF 01: VGH_COMP2_F 10: VGH_COMP3_S 11: VGH_COMP4_SS		10: VGH_COMP3_S
	[1:0] VGL Inverter Compensation	VGL_Inverter_COMP	00: VGL_COMP1_FF 01: VGL_COMP2_F 10: VGL_COMP3_S 11: VGL_COMP4_SS		10: VGL_COMP3_S
0x31h (02h)	[7] EN pin function select	EN_PIN_SEL	0: EN input function 1: XON output function		0: EN input
	[6] VCOM1 delay power off2	VCOM_DLY_OFF2	0: Follow 0x2Dh[4] setting 1: Follow AVDD falling 5V		0: 0x2Dh[4]
	[5] HAVDD delay power off	HAVDD_DLY_OFF	0: Follow VIN_UVLO_F 1: Follow AVDD falling 5V		0: UVLO_F
	[4] Gma1-14 delay power off	GMA_DLY_OFF	0: Follow VIN_UVLO_F 1: Follow AVDD falling 5V		0: UVLO_F
	[3:0] XON discharge Threshold	XON_DIS_THR	@[46h] bit7=0 00h(6.5V) to 0Fh(10.25V) @[46h] bit7=1 00h(3.63V)to 0Fh(vin_uvlo)	0.25V	0010: 7V

PMIC Register Map:

PMIC Device Address: 0x40h only VCOM1_NT Device Address: 0xE8h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x44h (00h)	[7] SLEEP MODE Enable	SLEEP_EN	0: Disable 1: Enable	0	0: Disable
	[6:5] Sleep power off delay time	SLEEP_POFF_DLY	00: 5ms 01: 10ms 10: 15ms 11: 20ms	0	0: 5ms
	[4:2] Sleep XAO off delay time	SLEEP_XAO_DLY	000: Follow SLEEP_POFF_DLY 001: Follow SHDN pull high 010: SLEEP_POFF_DLY -2ms 011: SLEEP_POFF_DLY -5ms 100: SLEEP_POFF_DLY -10ms 101: SLEEP_POFF_DLY +50us 110: SLEEP_POFF_DLY +100us 111: SLEEP_POFF_DLY +500us	0	0: UVLO_F
0x45h (00h)	[7:1] VCOM2DAC normal voltage	VCOM2DAC	VCOM.MIN to VCOM.MAX Res1= (vcom.max-vcom.min)/127	Res1	0*Res1+ VCOM.MIN (00h)
0x46h (00h)	[7] MNT MODE select	MNT_MODE _EN	0: TV MODE (VIN=12V) 1: MNT MODE (VIN=5V)		0: TV
	[0] VCOM2DAC enable	VCOM2DAC _EN	0: Disable 1: Enable		0: Disable

Register Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default value
0xFF	[7:6]&[0] Control Register								00 : Read data from DAC register 01 : Read data from MTP 40 : Write VCOM1 data from DAC to MTP 80 : Write all DAC into EEPROM

PMIC Register Map:

Only VCOM1_NT Device Address: 0xE8h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x00h	[4] Down load VCOM1_NT Data from MTP to DAC register	RESET	0: Disable 1: Enable		0: Disable
	[3] Write VCOM1_NT data From DAC register to MTP	VCOM1_NT _WR_MTP	0: Disable 1: Enable		0: Disable
	[1] VCOM1 output Enable	OUT_EN	0: Disable(VCOM1 Hiz) 1: Enable		1: Enable
0x01h	[7:1] VCOM1_NT normal Temperature voltage	VCOM1_NT	VCOM.MIN to VCOM.MAX Res1= (vcom.max-vcom.min)/127	Res1	63*Res1+ VCOMMIN (7Eh)
0x02h	[7] OTP	OTP_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[6] Check Sum Fail	CHECK_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[5] VBK UVP or SCP	VBK_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[4] AVDD UVP or SCP	AVDD_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[3] VGH UVP or SCP	VGH_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[2] VGL UVP or SCP	VGL_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[1] VSS1 UVP	VSS1_FT	0: Normal 1: Fault Read only IC restart		0: Normal
	[0] HAVDD UVP or SCP	HAVDD_FT	0: Normal 1: Fault Only Fault Indication		0: Normal

VCOM1 control --- 00h,(02h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	RESET	WR to MTP	Reserved	OUT_EN	Reserved

Bit	Name	Description
Bit4	RESET	Down load VCOM1_NT data from MTP to DAC register 0: Disable 1: Enable
Bit3	WR to MTP	Write VCOM1_NT data from DAC register to MTP 0: Disable 1: Enable
Bit1	OUT_EN	VCOM1_NT DAC output Enable 0: Disable(VCOM1 output is HI-Z) 1: Enable

VCOM1_NT --- 01h,(7Eh)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	1	1	1	1	1	Reserved

Registers and DAC settings

AVDD output voltage(0x00h) --- Default Code 29h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AVDD_OCP	AVDD_F	AVDD					
0	0	1	0	1	0	0	1

Bit	Name	Description
Bit7	AVDD_OCP	AVDD Switching Current Limit 0: 5.0A 1: 2.5A
Bit6	AVDD_F	AVDD output voltage offset 0: 0V 1: -0.5V

TV_MODE_EN @0x46h bit7=0 and 0x00h bit6=0

DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)
00h	13.5	10h	15.1	20h	16.7	30h	18.3
01h	13.6	11h	15.2	21h	16.8	31h	18.4
02h	13.7	12h	15.3	22h	16.9	32h	18.5
03h	13.8	13h	15.4	23h	17.0	33h	18.6
04h	13.9	14h	15.5	24h	17.1	34h	18.7
05h	14.0	15h	15.6	25h	17.2	35h	18.8
06h	14.1	16h	15.7	26h	17.3	36h	18.9
07h	14.2	17h	15.8	27h	17.4	37h	19.0
08h	14.3	18h	15.9	28h	17.5	38h	19.1
09h	14.4	19h	16.0	29h	17.6	39h	19.2
0Ah	14.5	1Ah	16.1	2Ah	17.7	3Ah	19.3
0Bh	14.6	1Bh	16.2	2Bh	17.8	3Bh	19.4
0Ch	14.7	1Ch	16.3	2Ch	17.9	3Ch	19.5
0Dh	14.8	1Dh	16.4	2Dh	18.0	3Dh	19.6
0Eh	14.9	1Eh	16.5	2Eh	18.1	3Eh	19.7
0Fh	15.0	1Fh	16.6	2Fh	18.2	3Fh	19.8

TV_MODE_EN @0x46h bit7=0 and 0x00h bit6=1

DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)
00h	13.0	10h	14.6	20h	16.2	30h	17.8
01h	13.1	11h	14.7	21h	16.3	31h	17.9
02h	13.2	12h	14.8	22h	16.4	32h	18.0
03h	13.3	13h	14.9	23h	16.5	33h	18.1
04h	13.4	14h	15.0	24h	16.6	34h	18.2
05h	13.5	15h	15.1	25h	16.7	35h	18.3
06h	13.6	16h	15.2	26h	16.8	36h	18.4
07h	13.7	17h	15.3	27h	16.9	37h	18.5
08h	13.8	18h	15.4	28h	17.0	38h	18.6
09h	13.9	19h	15.5	29h	17.1	39h	18.7
0Ah	14.0	1Ah	15.6	2Ah	17.2	3Ah	18.8
0Bh	14.1	1Bh	15.7	2Bh	17.3	3Bh	18.9
0Ch	14.2	1Ch	15.8	2Ch	17.4	3Ch	19.0
0Dh	14.3	1Dh	15.9	2Dh	17.5	3Dh	19.1
0Eh	14.4	1Eh	16.0	2Eh	17.6	3Eh	19.2
0Fh	14.5	1Fh	16.1	2Fh	17.7	3Fh	19.3

MNT_MODE_EN @0x46h bit7=1 (don't care 0x00h bit6 setting)

DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)	DAC Value	AVDD Voltage(V)
00h	11	10h	12.6	20h	14.2	30h	15.8
01h	11.1	11h	12.7	21h	14.3	31h	15.9
02h	11.2	12h	12.8	22h	14.4	32h	16.0
03h	11.3	13h	12.9	23h	14.5	33h	16.1
04h	11.4	14h	13.0	24h	14.6	34h	16.2
05h	11.5	15h	13.1	25h	14.7	35h	16.3
06h	11.6	16h	13.2	26h	14.8	36h	16.4
07h	11.7	17h	13.3	27h	14.9	37h	16.5
08h	11.8	18h	13.4	28h	15.0	38h	16.6
09h	11.9	19h	13.5	29h	15.1	39h	16.7
0Ah	12.0	1Ah	13.6	2Ah	15.2	3Ah	16.8
0Bh	12.1	1Bh	13.7	2Bh	15.3	3Bh	16.9
0Ch	12.2	1Ch	13.8	2Ch	15.4	3Ch	17.0
0Dh	12.3	1Dh	13.9	2Dh	15.5	3Dh	17.1
0Eh	12.4	1Eh	14.0	2Eh	15.6	3Eh	17.2
0Fh	12.5	1Fh	14.1	2Fh	15.7	3Fh	17.3

VBK output voltage(0x01h) --- Default Code 1Eh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	1	1	1	1	0

DAC Value	VBK Voltage(V)	DAC Value	VBK Voltage(V)	DAC Value	VBK Voltage(V)	DAC Value	VBK Voltage(V)
00h	1.80	08h	2.20	10h	2.60	18h	3.00
01h	1.85	09h	2.25	11h	2.65	19h	3.05
02h	1.90	0Ah	2.30	12h	2.70	1Ah	3.10
03h	1.95	0Bh	2.35	13h	2.75	1Bh	3.15
04h	2.00	0Ch	2.40	14h	2.80	1Ch	3.20
05h	2.05	0Dh	2.45	15h	2.85	1Dh	3.25
06h	2.10	0Eh	2.50	16h	2.90	1Eh	3.30
07h	2.15	0Fh	2.55	17h	2.95	1Fh	3.35

HAVDD output voltage(0x02h) --- Default Code 40h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	1	0	0	0	0	0	0

HAVDD=Res2*(HAVDD_CODE+192)
Res2=AVDD/512
HAVDD_CODE=0 ~ 127

DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)	DAC Value	HAVDD Voltage(V)
00h	Res2*(0+192)	20h	Res2*(32+192)	40h	Res2*(64+192)	60h	Res2*(96+192)
01h	Res2*(1+192)	21h	Res2*(33+192)	41h	Res2*(65+192)	61h	Res2*(97+192)
02h	Res2*(2+192)	22h	Res2*(34+192)	42h	Res2*(66+192)	62h	Res2*(98+192)
03h	Res2*(3+192)	23h	Res2*(35+192)	43h	Res2*(67+192)	63h	Res2*(99+192)
04h	Res2*(4+192)	24h	Res2*(36+192)	44h	Res2*(68+192)	64h	Res2*(100+192)
05h	Res2*(5+192)	25h	Res2*(37+192)	45h	Res2*(69+192)	65h	Res2*(101+192)
06h	Res2*(6+192)	26h	Res2*(38+192)	46h	Res2*(70+192)	66h	Res2*(102+192)
07h	Res2*(7+192)	27h	Res2*(39+192)	47h	Res2*(71+192)	67h	Res2*(103+192)
08h	Res2*(8+192)	28h	Res2*(40+192)	48h	Res2*(72+192)	68h	Res2*(104+192)
09h	Res2*(9+192)	29h	Res2*(41+192)	49h	Res2*(73+192)	69h	Res2*(105+192)
0Ah	Res2*(10+192)	2Ah	Res2*(42+192)	4Ah	Res2*(74+192)	6Ah	Res2*(106+192)
0Bh	Res2*(11+192)	2Bh	Res2*(43+192)	4Bh	Res2*(75+192)	6Bh	Res2*(107+192)
0Ch	Res2*(12+192)	2Ch	Res2*(44+192)	4Ch	Res2*(76+192)	6Ch	Res2*(108+192)
0Dh	Res2*(13+192)	2Dh	Res2*(45+192)	4Dh	Res2*(77+192)	6Dh	Res2*(109+192)
0Eh	Res2*(14+192)	2Eh	Res2*(46+192)	4Eh	Res2*(78+192)	6Eh	Res2*(110+192)
0Fh	Res2*(15+192)	2Fh	Res2*(47+192)	4Fh	Res2*(79+192)	6Fh	Res2*(111+192)
10h	Res2*(16+192)	30h	Res2*(48+192)	50h	Res2*(80+192)	70h	Res2*(112+192)
11h	Res2*(17+192)	31h	Res2*(49+192)	51h	Res2*(81+192)	71h	Res2*(113+192)
12h	Res2*(18+192)	32h	Res2*(50+192)	52h	Res2*(82+192)	72h	Res2*(114+192)
13h	Res2*(19+192)	33h	Res2*(51+192)	53h	Res2*(83+192)	73h	Res2*(115+192)
14h	Res2*(20+192)	34h	Res2*(52+192)	54h	Res2*(84+192)	74h	Res2*(116+192)
15h	Res2*(21+192)	35h	Res2*(53+192)	55h	Res2*(85+192)	75h	Res2*(117+192)
16h	Res2*(22+192)	36h	Res2*(54+192)	56h	Res2*(86+192)	76h	Res2*(118+192)
17h	Res2*(23+192)	37h	Res2*(55+192)	57h	Res2*(87+192)	77h	Res2*(119+192)
18h	Res2*(24+192)	38h	Res2*(56+192)	58h	Res2*(88+192)	78h	Res2*(120+192)
19h	Res2*(25+192)	39h	Res2*(57+192)	59h	Res2*(89+192)	79h	Res2*(121+192)
1Ah	Res2*(26+192)	3Ah	Res2*(58+192)	5Ah	Res2*(90+192)	7Ah	Res2*(122+192)
1Bh	Res2*(27+192)	3Bh	Res2*(59+192)	5Bh	Res2*(91+192)	7Bh	Res2*(123+192)
1Ch	Res2*(28+192)	3Ch	Res2*(60+192)	5Ch	Res2*(92+192)	7Ch	Res2*(124+192)
1Dh	Res2*(29+192)	3Dh	Res2*(61+192)	5Dh	Res2*(93+192)	7Dh	Res2*(125+192)
1Eh	Res2*(30+192)	3Eh	Res2*(62+192)	5Eh	Res2*(94+192)	7Eh	Res2*(126+192)
1Fh	Res2*(31+192)	3Fh	Res2*(63+192)	5Fh	Res2*(95+192)	7Fh	Res2*(127+192)

VGH_NT output voltage(0x03h) --- Default Code 0Ah

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGH_OCP	Reserved	Reserved	VGH_NT				
0			0	1	0	1	0

Bit	Name	Description
Bit7	VGH_OCP	VGH Switching Current Limit 0: 1.5A 1: 0.75A

DAC Value	VGH_NT Voltage(V)	DAC Value	VGH_NT Voltage(V)	DAC Value	VGH_NT Voltage(V)	DAC Value	VGH_NT Voltage(V)
00h	20	08h	28	10h	36	18h	42
01h	21	09h	29	11h	37	19h	42
02h	22	0Ah	30	12h	38	1Ah	42
03h	23	0Bh	31	13h	39	1Bh	42
04h	24	0Ch	32	14h	40	1Ch	42
05h	25	0Dh	33	15h	41	1Dh	42
06h	26	0Eh	34	16h	42	1Eh	42
07h	27	0Fh	35	17h	42	1Fh	42

VGH_LT output voltage(0x04h) --- Default Code 0Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGH_LT_EN	---	---	VGH_LT[4:0]				
0	Reserved	Reserved	0	1	1	1	1

Bit	Name	Description
Bit7	VGH_LT_EN	VGH temperature compensation enable 0: Disable 1: Enable

DAC Value	VGH_LT Voltage(V)	DAC Value	VGH_LT Voltage(V)	DAC Value	VGH_LT Voltage(V)	DAC Value	VGH_LT Voltage(V)
00h	20	08h	28	10h	36	18h	42
01h	21	09h	29	11h	37	19h	42
02h	22	0Ah	30	12h	38	1Ah	42
03h	23	0Bh	31	13h	39	1Bh	42
04h	24	0Ch	32	14h	40	1Ch	42
05h	25	0Dh	33	15h	41	1Dh	42
06h	26	0Eh	34	16h	42	1Eh	42
07h	27	0Fh	35	17h	42	1Fh	42

VGL_NT output voltage(0x05h) --- Default Code 0Ah

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGL_NT_offset	VGL_OCP	---	VGL_NT				
0	0	Reserved	0	1	0	1	0

Bit	Name	Description
Bit7	VGL_NT_OFFSET	VGL normal temperature voltage offset 0: Disable 1: VGL_NT-0.25V
Bit6	VGL_OCP	VGL Switching Current Limit 0: 1.5A 1: 0.75A

DAC Value	VGL_NT Voltage(V)	DAC Value	VGL_NT Voltage(V)	DAC Value	VGL_NT Voltage(V)	DAC Value	VGL_NT Voltage(V)
00h	-3.0	08h	-7.0	10h	-11.0	18h	-15.0
01h	-3.5	09h	-7.5	11h	-11.5	19h	-15.5
02h	-4.0	0Ah	-8.0	12h	-12.0	1Ah	-16.0
03h	-4.5	0Bh	-8.5	13h	-12.5	1Bh	-16.5
04h	-5.0	0Ch	-9.0	14h	-13.0	1Ch	-17.0
05h	-5.5	0Dh	-9.5	15h	-13.5	1Dh	-17.5
06h	-6.0	0Eh	-10.0	16h	-14.0	1Eh	-18.0
07h	-6.5	0Fh	-10.5	17h	-14.5	1Fh	-18.0

VGL_LT/HT output voltage(0x06h) --- Default Code 12h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGL_LT/HT_EN	VGL_LT/HT_SEL	---	VGL_NT				
0	0	Reserved	1	0	0	1	0

Bit	Name	Description
Bit7	VGL_LT/HT_EN	VGL_LT/HT temperature compensation enable 0: Disable 1: Enable
Bit6	VGL_LT/HT_SEL	VGL_LT/HT temperature compensation select 0: VGL_LT 1: VGL_HT

DAC Value	VGL_LT/HT Voltage(V)	DAC Value	VGL_LT/HT Voltage(V)	DAC Value	VGL_LT/HT Voltage(V)	DAC Value	VGL_LT/HT Voltage(V)
00h	-3.0	08h	-7.0	10h	-11.0	18h	-15.0
01h	-3.5	09h	-7.5	11h	-11.5	19h	-15.5
02h	-4.0	0Ah	-8.0	12h	-12.0	1Ah	-16.0
03h	-4.5	0Bh	-8.5	13h	-12.5	1Bh	-16.5
04h	-5.0	0Ch	-9.0	14h	-13.0	1Ch	-17.0
05h	-5.5	0Dh	-9.5	15h	-13.5	1Dh	-17.5
06h	-6.0	0Eh	-10.0	16h	-14.0	1Eh	-18.0
07h	-6.5	0Fh	-10.5	17h	-14.5	1Fh	-18.0

VCOM1_HT_EN & VSS1 output voltage(0x07h) --- Default Code 06h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM1_HT_EN	VSS1_offset	---	VSS1				
0	0	Reserved	0	0	1	1	0

Bit	Name	Description
Bit7	VCOM1_HT_EN	VCOM1 high temperature enable 0: Disable 1: Enable
Bit6	VSS1_OFFSET	VSS1 output voltage offset 0: Disable 1: VSS1-0.25V

DAC Value	VSS1 Voltage(V)	DAC Value	VSS1 Voltage(V)	DAC Value	VSS1 Voltage(V)	DAC Value	VSS1 Voltage(V)
00h	-3.0	08h	-7.0	10h	-11.0	18h	-15.0
01h	-3.5	09h	-7.5	11h	-11.5	19h	-15.5
02h	-4.0	0Ah	-8.0	12h	-12.0	1Ah	-16.0
03h	-4.5	0Bh	-8.5	13h	-12.5	1Bh	-16.0
04h	-5.0	0Ch	-9.0	14h	-13.0	1Ch	-16.0
05h	-5.5	0Dh	-9.5	15h	-13.5	1Dh	-16.0
06h	-6.0	0Eh	-10.0	16h	-14.0	1Eh	-16.0
07h	-6.5	0Fh	-10.5	17h	-14.5	1Fh	-16.0

VCOM1_NT output voltage(0x08h) --- Default Code 7Eh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM1_NT							---
0	1	1	1	1	1	1	Reserved

DAC Value	VCOM1_NT Voltage(V)	DAC Value	VCOM1_NT Voltage(V)	DAC Value	VCOM1_NT Voltage(V)	DAC Value	VCOM1_NT Voltage(V)
00h	0*Res1+V.MIN	40h	32*Res1+V.MIN	80h	64*Res1+V.MIN	C0h	96*Res1+V.MIN
02h	1*Res1+V.MIN	42h	33*Res1+V.MIN	82h	65*Res1+V.MIN	C2h	97*Res1+V.MIN
04h	2*Res1+V.MIN	44h	34*Res1+V.MIN	84h	66*Res1+V.MIN	C4h	98*Res1+V.MIN
06h	3*Res1+V.MIN	46h	35*Res1+V.MIN	86h	67*Res1+V.MIN	C6h	99*Res1+V.MIN
08h	4*Res1+V.MIN	48h	36*Res1+V.MIN	88h	68*Res1+V.MIN	C8h	100*Res1+V.MIN
0Ah	5*Res1+V.MIN	4Ah	37*Res1+V.MIN	8Ah	69*Res1+V.MIN	CAh	101*Res1+V.MIN
0Ch	6*Res1+V.MIN	4Ch	38*Res1+V.MIN	8Ch	70*Res1+V.MIN	CCh	102*Res1+V.MIN
0Eh	7*Res1+V.MIN	4Eh	39*Res1+V.MIN	8Eh	71*Res1+V.MIN	CEh	103*Res1+V.MIN
10h	8*Res1+V.MIN	50h	40*Res1+V.MIN	90h	72*Res1+V.MIN	D0h	104*Res1+V.MIN
12h	9*Res1+V.MIN	52h	41*Res1+V.MIN	92h	73*Res1+V.MIN	D2h	105*Res1+V.MIN
14h	10*Res1+V.MIN	54h	42*Res1+V.MIN	94h	74*Res1+V.MIN	D4h	106*Res1+V.MIN
16h	11*Res1+V.MIN	56h	43*Res1+V.MIN	96h	75*Res1+V.MIN	D6h	107*Res1+V.MIN
18h	12*Res1+V.MIN	58h	44*Res1+V.MIN	98h	76*Res1+V.MIN	D8h	108*Res1+V.MIN
1Ah	13*Res1+V.MIN	5Ah	45*Res1+V.MIN	9Ah	77*Res1+V.MIN	DAh	109*Res1+V.MIN
1Ch	14*Res1+V.MIN	5Ch	46*Res1+V.MIN	9Ch	78*Res1+V.MIN	DCh	110*Res1+V.MIN
1Eh	15*Res1+V.MIN	5Eh	47*Res1+V.MIN	9Eh	79*Res1+V.MIN	DEh	111*Res1+V.MIN
20h	16*Res1+V.MIN	60h	48*Res1+V.MIN	A0h	80*Res1+V.MIN	E0h	112*Res1+V.MIN
22h	17*Res1+V.MIN	62h	49*Res1+V.MIN	A2h	81*Res1+V.MIN	E2h	113*Res1+V.MIN
24h	18*Res1+V.MIN	64h	50*Res1+V.MIN	A4h	82*Res1+V.MIN	E4h	114*Res1+V.MIN
26h	19*Res1+V.MIN	66h	51*Res1+V.MIN	A6h	83*Res1+V.MIN	E6h	115*Res1+V.MIN
28h	20*Res1+V.MIN	68h	52*Res1+V.MIN	A8h	84*Res1+V.MIN	E8h	116*Res1+V.MIN
2Ah	21*Res1+V.MIN	6Ah	53*Res1+V.MIN	AAh	85*Res1+V.MIN	EAh	117*Res1+V.MIN
2Ch	22*Res1+V.MIN	6Ch	54*Res1+V.MIN	ACh	86*Res1+V.MIN	ECh	118*Res1+V.MIN
2Eh	23*Res1+V.MIN	6Eh	55*Res1+V.MIN	AEh	87*Res1+V.MIN	EEh	119*Res1+V.MIN
30h	24*Res1+V.MIN	70h	56*Res1+V.MIN	B0h	88*Res1+V.MIN	F0h	120*Res1+V.MIN
32h	25*Res1+V.MIN	72h	57*Res1+V.MIN	B2h	89*Res1+V.MIN	F2h	121*Res1+V.MIN
34h	26*Res1+V.MIN	74h	58*Res1+V.MIN	B4h	90*Res1+V.MIN	F4h	122*Res1+V.MIN
36h	27*Res1+V.MIN	76h	59*Res1+V.MIN	B6h	91*Res1+V.MIN	F6h	123*Res1+V.MIN
38h	28*Res1+V.MIN	78h	60*Res1+V.MIN	B8h	92*Res1+V.MIN	F8h	124*Res1+V.MIN
3Ah	29*Res1+V.MIN	7Ah	61*Res1+V.MIN	BAh	93*Res1+V.MIN	FAh	125*Res1+V.MIN
3Ch	30*Res1+V.MIN	7Ch	62*Res1+V.MIN	BCh	94*Res1+V.MIN	FCh	126*Res1+V.MIN
3Eh	31*Res1+V.MIN	7Eh	63*Res1+V.MIN	BEh	95*Res1+V.MIN	FEh	127*Res1+V.MIN

VCOM1_NT voltage formula
VCOM1_NT=Res1*VCOM1_NT CODE+VCOMMIN
Res1=(VCOMMAX-VCOMMIN)/127
VCOM1_NT CODE=0 ~ 127

VCOM1_HT output voltage(0x09h) --- Default Code BAh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM1_HT							---
1	0	1	1	1	0	1	Reserved

DAC Value	VCOM1_HT Voltage(V)	DAC Value	VCOM1_HT Voltage(V)	DAC Value	VCOM1_HT Voltage(V)	DAC Value	VCOM1_HT Voltage(V)
00h	0*Res1+V.MIN	40h	32*Res1+V.MIN	80h	64*Res1+V.MIN	C0h	96*Res1+V.MIN
02h	1*Res1+V.MIN	42h	33*Res1+V.MIN	82h	65*Res1+V.MIN	C2h	97*Res1+V.MIN
04h	2*Res1+V.MIN	44h	34*Res1+V.MIN	84h	66*Res1+V.MIN	C4h	98*Res1+V.MIN
06h	3*Res1+V.MIN	46h	35*Res1+V.MIN	86h	67*Res1+V.MIN	C6h	99*Res1+V.MIN
08h	4*Res1+V.MIN	48h	36*Res1+V.MIN	88h	68*Res1+V.MIN	C8h	100*Res1+V.MIN
0Ah	5*Res1+V.MIN	4Ah	37*Res1+V.MIN	8Ah	69*Res1+V.MIN	CAh	101*Res1+V.MIN
0Ch	6*Res1+V.MIN	4Ch	38*Res1+V.MIN	8Ch	70*Res1+V.MIN	CCh	102*Res1+V.MIN
0Eh	7*Res1+V.MIN	4Eh	39*Res1+V.MIN	8Eh	71*Res1+V.MIN	CEh	103*Res1+V.MIN
10h	8*Res1+V.MIN	50h	40*Res1+V.MIN	90h	72*Res1+V.MIN	D0h	104*Res1+V.MIN
12h	9*Res1+V.MIN	52h	41*Res1+V.MIN	92h	73*Res1+V.MIN	D2h	105*Res1+V.MIN
14h	10*Res1+V.MIN	54h	42*Res1+V.MIN	94h	74*Res1+V.MIN	D4h	106*Res1+V.MIN
16h	11*Res1+V.MIN	56h	43*Res1+V.MIN	96h	75*Res1+V.MIN	D6h	107*Res1+V.MIN
18h	12*Res1+V.MIN	58h	44*Res1+V.MIN	98h	76*Res1+V.MIN	D8h	108*Res1+V.MIN
1Ah	13*Res1+V.MIN	5Ah	45*Res1+V.MIN	9Ah	77*Res1+V.MIN	DAh	109*Res1+V.MIN
1Ch	14*Res1+V.MIN	5Ch	46*Res1+V.MIN	9Ch	78*Res1+V.MIN	DCh	110*Res1+V.MIN
1Eh	15*Res1+V.MIN	5Eh	47*Res1+V.MIN	9Eh	79*Res1+V.MIN	DEh	111*Res1+V.MIN
20h	16*Res1+V.MIN	60h	48*Res1+V.MIN	A0h	80*Res1+V.MIN	E0h	112*Res1+V.MIN
22h	17*Res1+V.MIN	62h	49*Res1+V.MIN	A2h	81*Res1+V.MIN	E2h	113*Res1+V.MIN
24h	18*Res1+V.MIN	64h	50*Res1+V.MIN	A4h	82*Res1+V.MIN	E4h	114*Res1+V.MIN
26h	19*Res1+V.MIN	66h	51*Res1+V.MIN	A6h	83*Res1+V.MIN	E6h	115*Res1+V.MIN
28h	20*Res1+V.MIN	68h	52*Res1+V.MIN	A8h	84*Res1+V.MIN	E8h	116*Res1+V.MIN
2Ah	21*Res1+V.MIN	6Ah	53*Res1+V.MIN	AAh	85*Res1+V.MIN	EAh	117*Res1+V.MIN
2Ch	22*Res1+V.MIN	6Ch	54*Res1+V.MIN	ACh	86*Res1+V.MIN	ECh	118*Res1+V.MIN
2Eh	23*Res1+V.MIN	6Eh	55*Res1+V.MIN	AEh	87*Res1+V.MIN	EEh	119*Res1+V.MIN
30h	24*Res1+V.MIN	70h	56*Res1+V.MIN	B0h	88*Res1+V.MIN	F0h	120*Res1+V.MIN
32h	25*Res1+V.MIN	72h	57*Res1+V.MIN	B2h	89*Res1+V.MIN	F2h	121*Res1+V.MIN
34h	26*Res1+V.MIN	74h	58*Res1+V.MIN	B4h	90*Res1+V.MIN	F4h	122*Res1+V.MIN
36h	27*Res1+V.MIN	76h	59*Res1+V.MIN	B6h	91*Res1+V.MIN	F6h	123*Res1+V.MIN
38h	28*Res1+V.MIN	78h	60*Res1+V.MIN	B8h	92*Res1+V.MIN	F8h	124*Res1+V.MIN
3Ah	29*Res1+V.MIN	7Ah	61*Res1+V.MIN	BAh	93*Res1+V.MIN	FAh	125*Res1+V.MIN
3Ch	30*Res1+V.MIN	7Ch	62*Res1+V.MIN	BCh	94*Res1+V.MIN	FCh	126*Res1+V.MIN
3Eh	31*Res1+V.MIN	7Eh	63*Res1+V.MIN	BEh	95*Res1+V.MIN	FEh	127*Res1+V.MIN

VCOM1_HT voltage formula
VCOM1_HT=Res1*VCOM1_HT CODE+VCOMMIN
Res1=(VCOMMAX-VCOMMIN)/127
VCOM1_HT CODE=0 ~ 127

VCOM_MAX output voltage(0x0Ah) --- Default Code 3Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
---	VCOM_MAX						
Reserved	0	1	1	1	1	1	1

DAC Value	VCOM_MAX Voltage(V)	DAC Value	VCOM_MAX Voltage(V)	DAC Value	VCOM_MAX Voltage(V)	DAC Value	VCOM_MAX Voltage(V)
00h	1*Res3	20h	33*Res3	40h	65*Res3	60h	97*Res3
01h	2*Res3	21h	34*Res3	41h	66*Res3	61h	98*Res3
02h	3*Res3	22h	35*Res3	42h	67*Res3	62h	99*Res3
03h	4*Res3	23h	36*Res3	43h	68*Res3	63h	100*Res3
04h	5*Res3	24h	37*Res3	44h	69*Res3	64h	101*Res3
05h	6*Res3	25h	38*Res3	45h	70*Res3	65h	102*Res3
06h	7*Res3	26h	39*Res3	46h	71*Res3	66h	103*Res3
07h	8*Res3	27h	40*Res3	47h	72*Res3	67h	104*Res3
08h	9*Res3	28h	41*Res3	48h	73*Res3	68h	105*Res3
09h	10*Res3	29h	42*Res3	49h	74*Res3	69h	106*Res3
0Ah	11*Res3	2Ah	43*Res3	4Ah	75*Res3	6Ah	107*Res3
0Bh	12*Res3	2Bh	44*Res3	4Bh	76*Res3	6Bh	108*Res3
0Ch	13*Res3	2Ch	45*Res3	4Ch	77*Res3	6Ch	109*Res3
0Dh	14*Res3	2Dh	46*Res3	4Dh	78*Res3	6Dh	110*Res3
0Eh	15*Res3	2Eh	47*Res3	4Eh	79*Res3	6Eh	111*Res3
0Fh	16*Res3	2Fh	48*Res3	4Fh	80*Res3	6Fh	112*Res3
10h	17*Res3	30h	49*Res3	50h	81*Res3	70h	113*Res3
11h	18*Res3	31h	50*Res3	51h	82*Res3	71h	114*Res3
12h	19*Res3	32h	51*Res3	52h	83*Res3	72h	115*Res3
13h	20*Res3	33h	52*Res3	53h	84*Res3	73h	116*Res3
14h	21*Res3	34h	53*Res3	54h	85*Res3	74h	117*Res3
15h	22*Res3	35h	54*Res3	55h	86*Res3	75h	118*Res3
16h	23*Res3	36h	55*Res3	56h	87*Res3	76h	119*Res3
17h	24*Res3	37h	56*Res3	57h	88*Res3	77h	120*Res3
18h	25*Res3	38h	57*Res3	58h	89*Res3	78h	121*Res3
19h	26*Res3	39h	58*Res3	59h	90*Res3	79h	122*Res3
1Ah	27*Res3	3Ah	59*Res3	5Ah	91*Res3	7Ah	123*Res3
1Bh	28*Res3	3Bh	60*Res3	5Bh	92*Res3	7Bh	124*Res3
1Ch	29*Res3	3Ch	61*Res3	5Ch	93*Res3	7Ch	125*Res3
1Dh	30*Res3	3Dh	62*Res3	5Dh	94*Res3	7Dh	126*Res3
1Eh	31*Res3	3Eh	63*Res3	5Eh	95*Res3	7Eh	127*Res3
1Fh	32*Res3	3Fh	63*Res3	5Fh	96*Res3	7Fh	128*Res3

VCOM_MAX voltage formula
VCOM_MAX=Res3*[(VCOM_MAX CODE)+1]
Res3=VAVDD/128

VCOM_MIN output voltage(0x0Bh) --- Default Code 26h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
---	VCOM_MIN						
Reserved	0	1	0	0	1	1	0

DAC Value	VCOM_MIN Voltage(V)	DAC Value	VCOM_MIN Voltage(V)	DAC Value	VCOM_MIN Voltage(V)	DAC Value	VCOM_MIN Voltage(V)
00h	0*Res3	20h	32*Res3	40h	64*Res3	60h	96*Res3
01h	1*Res3	21h	33*Res3	41h	65*Res3	61h	97*Res3
02h	2*Res3	22h	34*Res3	42h	66*Res3	62h	98*Res3
03h	3*Res3	23h	35*Res3	43h	67*Res3	63h	99*Res3
04h	4*Res3	24h	36*Res3	44h	68*Res3	64h	100*Res3
05h	5*Res3	25h	37*Res3	45h	69*Res3	65h	101*Res3
06h	6*Res3	26h	38*Res3	46h	70*Res3	66h	102*Res3
07h	7*Res3	27h	39*Res3	47h	71*Res3	67h	103*Res3
08h	8*Res3	28h	40*Res3	48h	72*Res3	68h	104*Res3
09h	9*Res3	29h	41*Res3	49h	73*Res3	69h	105*Res3
0Ah	10*Res3	2Ah	42*Res3	4Ah	74*Res3	6Ah	106*Res3
0Bh	11*Res3	2Bh	43*Res3	4Bh	75*Res3	6Bh	107*Res3
0Ch	12*Res3	2Ch	44*Res3	4Ch	76*Res3	6Ch	108*Res3
0Dh	13*Res3	2Dh	45*Res3	4Dh	77*Res3	6Dh	109*Res3
0Eh	14*Res3	2Eh	46*Res3	4Eh	78*Res3	6Eh	110*Res3
0Fh	15*Res3	2Fh	47*Res3	4Fh	79*Res3	6Fh	111*Res3
10h	16*Res3	30h	48*Res3	50h	80*Res3	70h	112*Res3
11h	17*Res3	31h	49*Res3	51h	81*Res3	71h	113*Res3
12h	18*Res3	32h	50*Res3	52h	82*Res3	72h	114*Res3
13h	19*Res3	33h	51*Res3	53h	83*Res3	73h	115*Res3
14h	20*Res3	34h	52*Res3	54h	84*Res3	74h	116*Res3
15h	21*Res3	35h	53*Res3	55h	85*Res3	75h	117*Res3
16h	22*Res3	36h	54*Res3	56h	86*Res3	76h	118*Res3
17h	23*Res3	37h	55*Res3	57h	87*Res3	77h	119*Res3
18h	24*Res3	38h	56*Res3	58h	88*Res3	78h	120*Res3
19h	25*Res3	39h	57*Res3	59h	89*Res3	79h	121*Res3
1Ah	26*Res3	3Ah	58*Res3	5Ah	90*Res3	7Ah	122*Res3
1Bh	27*Res3	3Bh	59*Res3	5Bh	91*Res3	7Bh	123*Res3
1Ch	28*Res3	3Ch	60*Res3	5Ch	92*Res3	7Ch	124*Res3
1Dh	29*Res3	3Dh	61*Res3	5Dh	93*Res3	7Dh	125*Res3
1Eh	30*Res3	3Eh	62*Res3	5Eh	94*Res3	7Eh	126*Res3
1Fh	31*Res3	3Fh	63*Res3	5Fh	95*Res3	7Fh	127*Res3

VCOM_MIN voltage formula
VCOM_MIN=Res3*(VCOM_MIN CODE)
Res3=VAVDD/128

GAMMA 1~14 output voltage(0x0Ch~0x27h)

Address	Name	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0Ch	GMA1	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x0Dh	GMA1	00h	0	0	0	0	0	0	0	0
0x0Eh	GMA2	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x0Fh	GMA2	00h	0	0	0	0	0	0	0	0
0x10h	GMA3	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x11h	GMA3	00h	0	0	0	0	0	0	0	0
0x12h	GMA4	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x13h	GMA4	00h	0	0	0	0	0	0	0	0
0x14h	GMA5	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x15h	GMA5	00h	0	0	0	0	0	0	0	0
0x16h	GMA6	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x17h	GMA6	00h	0	0	0	0	0	0	0	0
0x18h	GMA7	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x19h	GMA7	00h	0	0	0	0	0	0	0	0
0x1Ah	GMA8	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x1Bh	GMA8	00h	0	0	0	0	0	0	0	0
0x1Ch	GMA9	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x1Dh	GMA9	00h	0	0	0	0	0	0	0	0
0x1Eh	GMA10	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x1Fh	GMA10	00h	0	0	0	0	0	0	0	0
0x20h	GMA11	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x21h	GMA11	00h	0	0	0	0	0	0	0	0
0x22h	GMA12	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x23h	GMA12	00h	0	0	0	0	0	0	0	0
0x24h	GMA13	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x25h	GMA13	00h	0	0	0	0	0	0	0	0
0x26h	GMA14	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	1	0
0x27h	GMA14	00h	0	0	0	0	0	0	0	0

VGAMMA 1~14 voltage formula

$V_{GAMMA\ 1\sim14}$=Res4*$V_{GAMMA\ 1\sim14}$_CODE

Res4=V_{AVDD}/1024

GAMMA 1~14 output voltage (Unit:V)

DAC value	GAMMA 1~14	DAC value	GAMMA 1~14
0000h	0	0200h	Res4*512
0001h	Res4*1	0201h	Res4*513
0002h	Res4*2	0202h	Res4*514
0003h	Res4*3	0203h	Res4*515
0004h	Res4*4	0204h	Res4*516
0005h	Res4*5	0205h	Res4*517
0006h	Res4*6	0206h	Res4*518
0007h	Res4*7	0207h	Res4*519
0008h	Res4*8	0208h	Res4*520
0009h	Res4*9	0209h	Res4*521
000Ah	Res4*10	020Ah	Res4*522
000Bh	Res4*11	020Bh	Res4*523
000Ch	Res4*12	020Ch	Res4*524
000Dh	Res4*13	020Dh	Res4*525
000Eh	Res4*14	020Eh	Res4*526
000Fh	Res4*15	020Fh	Res4*527
……	……	……	……
……	……	……	……
01F0h	Res4*496	03F0h	Res4*1008
01F1h	Res4*497	03F1h	Res4*1009
01F2h	Res4*498	03F2h	Res4*1010
01F3h	Res4*499	03F3h	Res4*1011
01F4h	Res4*500	03F4h	Res4*1012
01F5h	Res4*501	03F5h	Res4*1013
01F6h	Res4*502	03F6h	Res4*1014
01F7h	Res4*503	03F7h	Res4*1015
01F8h	Res4*504	03F8h	Res4*1016
01F9h	Res4*505	03F9h	Res4*1017
01FAh	Res4*506	03FAh	Res4*1018
01FBh	Res4*507	03FBh	Res4*1019
01FCh	Res4*508	03FCh	Res4*1020
01FDh	Res4*509	03FDh	Res4*1021
01FEh	Res4*510	03FEh	Res4*1022
01FFh	Res4*511	03FFh	Res4*1023

Channel Enable Register(0x28h) --- Default Code 7Fh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GroupB_EN	VGL_EN	VSS1_EN	AVDD_EN	HAVDD_EN	GMA_EN	VCOM1_EN	VGH_EN
0	1	1	1	1	1	1	1

Bit	Name	Description
Bit7	GROUP B_EN	GROUP B enable 0: Disable 1: Enable
Bit6	VGL_EN	VGL enable 0: Disable 1: Enable
Bit5	VSS1_EN	VSS1 enable 0: Disable 1: Enable
Bit4	AVDD_EN	AVDD enable 0: Disable 1: Enable
Bit3	HAVDD_EN	HAVDD enable 0: Disable 1: Enable
Bit2	GMA_EN	GMA enable 0: Disable 1: Enable
Bit1	VCOM1_EN	VCOM1 enable 0: Disable 1: Enable
Bit0	VGH_EN	VGH enable 0: Disable 1: Enable

Function Setting(0x29h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FREQ_SEL		ISO_MOS_SEL	AVDD_MOS_SEL	VGH_TYPE	VGL_TYPE	VGL_PUMU_SOURCE	GMA_CH_TYEP
0	0	0	0	0	0	0	0

Bit	Name	Description
Bit7	FREQ_SEL1	Frequency select (VBK,AVDD,VGH,VGL) 0: 750KHz 1: 500KHz
Bit6	FREQ_SEL2	Frequency select (VBK,AVDD,VGH,VGL) 0: by 0x29h[7] setting 1: 1000KHz
Bit5	ISO_PMOS_INT/EXT_SEL	Isolation PMOS Internal/External select 0: External 1: Internal
Bit4	AVDD_MOS_INT/EXT	AVDD NMOS Internal/External select 0: Internal 1: External (@[29h] bit3 output keep boost and bit1 output keep LXBK1)
Bit3	VGH_TYPE	VGH structure type 0: Boost 1: Charge pump (AVDD Internal mode only)
Bit2	VGL_TYPE	VGL structure type 0: Inverting 1: Chrage pump (AVDD internal mode or AVDD external@[29h] bit1 keep LXBK1
Bit1	VGL_PUMP_SOURCE	VGL charge pump source 0: VBK 1: LX/CS
Bit0	GMA_CH_TYPE	GAMMA channel type 0: 14_CH (1 to 14_CH) 1: 4_CH (1,7,8,14_CH, other channel output Hi-Z)

Delay time Setting(0x2Ah) --- Default Code 05h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DLY7_DLOUT		DLY1_VBK		DLY2_VGL		DLY3_VSS1	
0	0	0	0	0	1	0	1

DAC Value	DLY7_DLOUT time(ms)	DAC Value	DLY7_DLOUT time(ms)	DAC Value	DLY7_DLOUT time(ms)	DAC Value	DLY7_DLOUT time(ms)
00h	0	01h	2	02h	4	03h	6

TV MODE [46h] bit7=0

DAC Value	DLY1_VBK time(ms)	DAC Value	DLY1_VBK time(ms)	DAC Value	DLY1_VBK time(ms)	DAC Value	DLY1_VBK time(ms)
00h	0	01h	2	02h	4	03h	6

MNT MODE [46h] bit7=1

DAC Value	DLY1_VBK time(ms)	DAC Value	DLY1_VBK time(ms)	DAC Value	DLY1_VBK time(ms)	DAC Value	DLY1_VBK time(ms)
00h	0	01h	40	02h	80	03h	120

DAC Value	DLY2_VGL time(ms)	DAC Value	DLY2_VGL time(ms)	DAC Value	DLY2_VGL time(ms)	DAC Value	DLY2_VGL time(ms)
00h	0	01h	5	02h	10	03h	15

DAC Value	DLY3_VSS1 time(ms)	DAC Value	DLY3_VSS1 time(ms)	DAC Value	DLY3_VSS1 time(ms)	DAC Value	DLY3_VSS1 time(ms)
00h	0	01h	2	02h	4	03h	6

Delay time Setting(0x2Bh) --- Default Code 28h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIS_ADDR	DLY4_AVDD		DLY5_VGH		DLY6_VCOM		
0	0	1	0	1	0	0	0

Bit	Name	Description
Bit7	ADJ_ADDR	Disable E8h address 0: E8h 1: EAh

DAC Value	DLY4_AVDD time(ms)	DAC Value	DLY4_AVDD time(ms)	DAC Value	DLY4_AVDD time(ms)	DAC Value	DLY4_AVDD time(ms)
00h	0	01h	5	02h	10	03h	15

DAC Value	DLY5_VGH time(ms)	DAC Value	DLY5_VGH time(ms)	DAC Value	DLY5_VGH time(ms)	DAC Value	DLY5_VGH time(ms)
00h	0	01h	2	02h	4	03h	6

DAC Value	DLY6_VCOM time(ms)	DAC Value	DLY6_VCOM time(ms)	DAC Value	DLY6_VCOM time(ms)	DAC Value	DLY6_VCOM time(ms)
00h	0	01h	30	02h	60	03h	90
04h	120	05h	150	06h	180	07h	210

Discharge Setting(0x2Ch) --- Default Code FFh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ALL_DIS_EN	BK1_DIS	AVDD_DIS	VGH_DIS	VGL_DIS	HAVDD_DIS	VCOM1_DIS	
1	1	1	1	1	1	1	1

Bit	Name	Description
Bit7	ALL_DIS_EN	All output channel discharge enable 0: Enable 1: Disable
Bit6	BK1_DIS	Buck1 discharge 0: 0.5KΩ 1: 1KΩ
Bit5	AVDD_DIS	AVDD discharge 0: 1.4KΩ 1: 4.7KΩ
Bit4	VGH_DIS	VGH discharge 0: 1.5KΩ 1: 30KΩ
Bit3	VGL_DIS	VGL discharge 0: Disable 1: 10KΩ
Bit2	HAVDD_DIS	HAVDD discharge 0: Disable 1: 10KΩ
Bit1	VCOM1_DIS	VCOM1 discharge 00: Disable 01: 20Ω 10:1KΩ 11: 8KΩ
Bit0		

Function Setting (0x2Dh) --- Default Code 85h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VSS1_DIS	Reserved	Reserved	VCOM1_DLY_OFF1	HAVDD_FB	AVDD_GD_SCP	AVDD_SS	VGH_SS
1	0	0	0	0	1	0	1

Bit	Name	Description
Bit7	VSS1_DIS	VSS1 discharge 0: Disable 1: 1.2KΩ
Bit6	Reserved	Reserved
Bit5	Reserved	Reserved
Bit4	VCOM1_DLY_OFF1	VCOM1 delay power off 0: VIN_UVLO_F 1: XON discharge threshold
Bit3	HAVDD FB	HAVDD feedback mode select 0: (G7+G8)/2 1: HAVDD DAC register
Bit2	AVDD_GD_SCP	AVDD GDMOS SCP select 0: GD_SCP_MODE1 power up of three fail attempts and AVDD FIMV1 detect 1: GD_SCP_MODE2 power up of three fail attempts and AVDD FIMV2 detect
Bit1	AVDD_SS	AVDD startup softstart time 0: 10ms 1: 20ms
Bit0	VGH_SS	VGH startup softstart time 0: 3ms 1: 6ms

VGH&VGL_VTC1 & VTC2 (0x2Eh) --- Default Code D8h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGH&VGL_VTC2				VGH&VGL_VTC1			
1	1	0	1	1	0	0	0

DAC Value	VGH&VGL VTC2(V)	DAC Value	VGH&VGL VTC2(V)	DAC Value	VGH&VGL VTC2(V)	DAC Value	VGH&VGL VTC2(V)
00h	0.4	04h	1.2	08h	2.0	0Ch	2.8
01h	0.6	05h	1.4	09h	2.2	0Dh	3.0
02h	0.8	06h	1.6	0Ah	2.4	0Eh	3.2
03h	1.0	07h	1.8	0Bh	2.6	0Fh	3.4

DAC Value	VGH&VGL VTC1(V)	DAC Value	VGH&VGL VTC1(V)	DAC Value	VGH&VGL VTC1(V)	DAC Value	VGH&VGL VTC1(V)
00h	0.4	04h	1.2	08h	2.0	0Ch	2.8
01h	0.6	05h	1.4	09h	2.2	0Dh	3.0
02h	0.8	06h	1.6	0Ah	2.4	0Eh	3.2
03h	1.0	07h	1.8	0Bh	2.6	0Fh	3.4

VCOM1_VTC1 & VTC2 (0x2Fh) --- Default Code 41h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM1_VTC2				VCOM1_VTC1			
0	1	0	0	0	0	0	1

DAC Value	VCOM1 VTC2(V)	DAC Value	VCOM1 VTC2(V)	DAC Value	VCOM1 VTC2(V)	DAC Value	VCOM1 VTC2(V)
00h	0.4	04h	1.2	08h	2.0	0Ch	2.8
01h	0.6	05h	1.4	09h	2.2	0Dh	3.0
02h	0.8	06h	1.6	0Ah	2.4	0Eh	3.2
03h	1.0	07h	1.8	0Bh	2.6	0Fh	3.4

DAC Value	VCOM1 VTC1(V)	DAC Value	VCOM1 VTC1(V)	DAC Value	VCOM1 VTC1(V)	DAC Value	VCOM1 VTC1(V)
00h	0.4	04h	1.2	08h	2.0	0Ch	2.8
01h	0.6	05h	1.4	09h	2.2	0Dh	3.0
02h	0.8	06h	1.6	0Ah	2.4	0Eh	3.2
03h	1.0	07h	1.8	0Bh	2.6	0Fh	3.4

Compensation Control (0x30h) --- Default Code 1Ah

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	AVDD_EXT_DRV		VGH_boost_COMP		VGL_inverting_COMP	
0	0	0	1	1	0	1	0

Bit	Name	Description
Bit7	Reserved	Reserved
Bit6	Reserved	Reserved
Bit5 Bit4	AVDD_EXT_DRV	AVDD external drving of Gate 00: EXT_DRV1_FF 01: EXT_DRV2_F 10: EXT_DRV3_S 11: EXT_DRV4_SS
Bit3 Bit2	VGH_Boost_COMP	VGH boost converter compensation 00: VGH_COMP1_FF 01: VGH_COMP2_F 10: VGH_COMP3_S 11: VGH_COMP4_SS
Bit1 Bit0	VGL_Inverting_COMP	VGL inverting compensation 00: VGL_COMP1_FF 01: VGL_COMP2_F 10: VGL_COMP3_S 11: VGL_COMP4_SS

XON discharge threshold (0x31h) --- Default Code 02h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_PIN_SEL	VCOM1_DLY_OFF	HAVDD_DLY_OFF	GMA_DLY_OFF	XON_DIS_TH			
0	0	0	0	0	0	1	0

Bit	Name	Description
Bit7	EN_PIN_SEL	EN pin function select 0: EN input function 1: XON output function
Bit6	VCOM1_DLY_OFF2	VCOM1 delay power off 0: Disabel (follow 0x2D bit4) 1: Enable(follow AVDD=5V)
Bit5	HAVDD_DLY_OFF	HAVDD delay power off 0: Disabel (follow VIN_UVLO_F) 1: Enable(follow AVDD=5V)
Bit4	GMA_DLY_OFF	GMA1-14 delay power off 0: Disabel (follow VIN_UVLO_F) 1: Enable(follow AVDD=5V)

MNT_MODE_EN @0x46h bit7=0 (TV MODE)

DAC Value	XON_TH (V)	DAC Value	XON_TH (V)	DAC Value	XON_TH (V)	DAC Value	XON_TH (V)
00h	6.50	04h	7.50	08h	8.50	0Ch	9.50
01h	6.75	05h	7.75	09h	8.75	0Dh	9.75
02h	7.00	06h	8.00	0Ah	9.00	0Eh	10.00
03h	7.25	07h	8.25	0Bh	9.25	0Fh	10.25

MNT_MODE_EN @0x46h bit7=0 (MNT MODE)

DAC Value	XON_TH (V)	DAC Value	XON_TH (V)	DAC Value	XON_TH (V)	DAC Value	XON_TH (V)
00h	3.63	04h	4.19	08h	4.74	0Ch	5.30
01h	3.77	05h	4.33	09h	4.88	0Dh	5.44
02h	3.91	06h	4.47	0Ah	5.02	0Eh	5.58
03h	4.05	07h	4.60	0Bh	5.16	0Fh	VIN_UVLOF

Sleep Control (0x44h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SLEEP_EN	SLEEP_POFF_DLY		SLEEP_XAO_DLY			Reserved	Reserved
0	0	0	0	0	0	0	0

Bit	Name	Description
Bit7	SLEEP_EN	Sleep Mode Enable 0: Disable 1: Enable
Bit6 Bit5	SLEEP_POFF_DLY	Sleep turn on power off delay time 00: 5ms 01: 10ms 10: 15ms 11: 20ms
Bit4 Bit3 Bit2	SLEEP_XAO_DLY	Sleep tron on xao pull low delay time 000: Follow SLEEP_POFF_DLY 001: Follow SHDN pull high 010: SLEEP_POFF_DLY -2ms 011: SLEEP_POFF_DLY -5ms 100: SLEEP_POFF_DLY -10ms 101: SLEEP_POFF_DLY +50us 110: SLEEP_POFF_DLY +100us 111: SLEEP_POFF_DLY +500us
Bit1	Reserved	Reserved
Bit0	Reserved	Reserved

VCOM2DAC output voltage(0x45h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VCOM2 DAC							---
0	1	1	1	1	1	1	Reserved

DAC Value	VCOM1_HT Voltage(V)	DAC Value	VCOM1_HT Voltage(V)	DAC Value	VCOM1_HT Voltage(V)	DAC Value	VCOM1_HT Voltage(V)
00h	0*Res1+V.MIN	40h	32*Res1+V.MIN	80h	64*Res1+V.MIN	C0h	96*Res1+V.MIN
02h	1*Res1+V.MIN	42h	33*Res1+V.MIN	82h	65*Res1+V.MIN	C2h	97*Res1+V.MIN
04h	2*Res1+V.MIN	44h	34*Res1+V.MIN	84h	66*Res1+V.MIN	C4h	98*Res1+V.MIN
06h	3*Res1+V.MIN	46h	35*Res1+V.MIN	86h	67*Res1+V.MIN	C6h	99*Res1+V.MIN
08h	4*Res1+V.MIN	48h	36*Res1+V.MIN	88h	68*Res1+V.MIN	C8h	100*Res1+V.MIN
0Ah	5*Res1+V.MIN	4Ah	37*Res1+V.MIN	8Ah	69*Res1+V.MIN	CAh	101*Res1+V.MIN
0Ch	6*Res1+V.MIN	4Ch	38*Res1+V.MIN	8Ch	70*Res1+V.MIN	CCh	102*Res1+V.MIN
0Eh	7*Res1+V.MIN	4Eh	39*Res1+V.MIN	8Eh	71*Res1+V.MIN	CEh	103*Res1+V.MIN
10h	8*Res1+V.MIN	50h	40*Res1+V.MIN	90h	72*Res1+V.MIN	D0h	104*Res1+V.MIN
12h	9*Res1+V.MIN	52h	41*Res1+V.MIN	92h	73*Res1+V.MIN	D2h	105*Res1+V.MIN
14h	10*Res1+V.MIN	54h	42*Res1+V.MIN	94h	74*Res1+V.MIN	D4h	106*Res1+V.MIN
16h	11*Res1+V.MIN	56h	43*Res1+V.MIN	96h	75*Res1+V.MIN	D6h	107*Res1+V.MIN
18h	12*Res1+V.MIN	58h	44*Res1+V.MIN	98h	76*Res1+V.MIN	D8h	108*Res1+V.MIN
1Ah	13*Res1+V.MIN	5Ah	45*Res1+V.MIN	9Ah	77*Res1+V.MIN	DAh	109*Res1+V.MIN
1Ch	14*Res1+V.MIN	5Ch	46*Res1+V.MIN	9Ch	78*Res1+V.MIN	DCh	110*Res1+V.MIN
1Eh	15*Res1+V.MIN	5Eh	47*Res1+V.MIN	9Eh	79*Res1+V.MIN	DEh	111*Res1+V.MIN
20h	16*Res1+V.MIN	60h	48*Res1+V.MIN	A0h	80*Res1+V.MIN	E0h	112*Res1+V.MIN
22h	17*Res1+V.MIN	62h	49*Res1+V.MIN	A2h	81*Res1+V.MIN	E2h	113*Res1+V.MIN
24h	18*Res1+V.MIN	64h	50*Res1+V.MIN	A4h	82*Res1+V.MIN	E4h	114*Res1+V.MIN
26h	19*Res1+V.MIN	66h	51*Res1+V.MIN	A6h	83*Res1+V.MIN	E6h	115*Res1+V.MIN
28h	20*Res1+V.MIN	68h	52*Res1+V.MIN	A8h	84*Res1+V.MIN	E8h	116*Res1+V.MIN
2Ah	21*Res1+V.MIN	6Ah	53*Res1+V.MIN	AAh	85*Res1+V.MIN	EAh	117*Res1+V.MIN
2Ch	22*Res1+V.MIN	6Ch	54*Res1+V.MIN	ACh	86*Res1+V.MIN	ECh	118*Res1+V.MIN
2Eh	23*Res1+V.MIN	6Eh	55*Res1+V.MIN	AEh	87*Res1+V.MIN	EEh	119*Res1+V.MIN
30h	24*Res1+V.MIN	70h	56*Res1+V.MIN	B0h	88*Res1+V.MIN	F0h	120*Res1+V.MIN
32h	25*Res1+V.MIN	72h	57*Res1+V.MIN	B2h	89*Res1+V.MIN	F2h	121*Res1+V.MIN
34h	26*Res1+V.MIN	74h	58*Res1+V.MIN	B4h	90*Res1+V.MIN	F4h	122*Res1+V.MIN
36h	27*Res1+V.MIN	76h	59*Res1+V.MIN	B6h	91*Res1+V.MIN	F6h	123*Res1+V.MIN
38h	28*Res1+V.MIN	78h	60*Res1+V.MIN	B8h	92*Res1+V.MIN	F8h	124*Res1+V.MIN
3Ah	29*Res1+V.MIN	7Ah	61*Res1+V.MIN	BAh	93*Res1+V.MIN	FAh	125*Res1+V.MIN
3Ch	30*Res1+V.MIN	7Ch	62*Res1+V.MIN	BCh	94*Res1+V.MIN	FCh	126*Res1+V.MIN
3Eh	31*Res1+V.MIN	7Eh	63*Res1+V.MIN	BEh	95*Res1+V.MIN	FEh	127*Res1+V.MIN

VCOM2 DAC voltage formula
VCOM2DAC=Res1*VCOM2DAC CODE+VCOMMIN
Res1=(VCOMMAX-VCOMMIN)/127
VCOM2DAC CODE=0 ~ 127

MNT&TV (0x46h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MNT_MODE_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCOM2DAC_EN
0	0	0	0	0	0	0	0

Bit	Name	Description
Bit7	MNT_MODE_EN	MNT&TV MODE select 0: TV MODE (VIN=12V) 1: MNT MODE (VIN=5V)
Bit6	Reserved	Reserved
Bit5	Reserved	Reserved
Bit4	Reserved	Reserved
Bit3	Reserved	Reserved
Bit2	Reserved	Reserved
Bit1	Reserved	Reserved
Bit0	VCOM2DAC_EN	VCOM2DAC enable 0: Disable 1: Enable

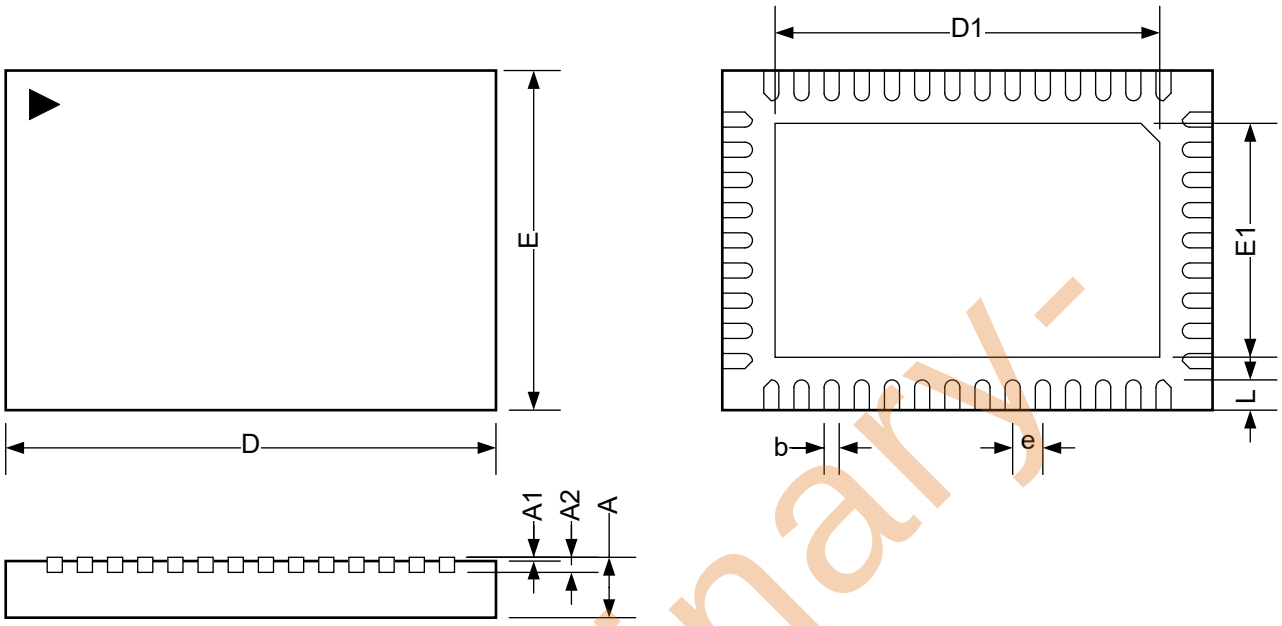
Protection Table
Group A: VBK
Group B: AVDD,HAVDD,VGH,VGL,VSS1,GAMMA,VCOM1,VCOM2DAC (LS OUTPUT)

Block	Protection	Work Condition	Action
VBK	OCP	2.0A	
	UVP	VBK<80%, after 50ms	IC Group A/B shut down,Latch Release IC restart
	SCP	VBK<20%	IC Group A/B shut down,Latch Release IC restart
	OVP	VBK>120%	LXBK1 stop switching, Release OVP-hysteresis
AVDD	OCP	5.0A	
	UVP	AVDD<85%, after 50ms	IC Group B shut down,Latch Release IC restart
	SCP	AVDD<20%	IC Group B shut down,Latch Release IC restart
	OVP	AVDD>21.5V	LX/CS stop switching, Release OVP-hysteresis
VGH	OCP	1.5A	
	UVP	VGH<80%, after 50ms	IC Group B shut down,Latch Release IC restart
	SCP	VGH<20%	IC Group B shut down,Latch Release IC restart
	OVP	VGH>44V	LXVGH stop switching, Release OVP-hysteresis
VGL	OCP	1.5A	
	UVP	VGL<80%, after 50ms	IC Group B shut down,Latch Release IC restart
	SCP	VGL<20%	IC Group B shut down,Latch Release IC restart
	OVP	VGL>120%	LXVGL stop switching, Release OVP-hysteresis
VSS1	OCP	±100mA	
	UVP	VSS1<80%, after 50ms	IC Group B shut down,Latch Release IC restart
HAVDD	OCP	±500mA	Peak current
	SCP	±100mA	Current limit keep
VCOM	OCP	±500mA	Peak curren
	SCP	±100mA	Current limit keep
GMA(14ch)	OCP	±100mA	Peak current
	SCP	±30mA	Current limit keep
GMA(4ch)	OCP	±150mA	Peak current
	SCP	±50mA	Current limit keep
PMIC	OTP	IC temp > 150	IC Group A/B shut down,Latch

Note: SCP and OVP is trigger immediate, no trigger time

Packaging Information

QFN6.5X4.5-46



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	6.40	6.50	6.60	0.2520	0.2559	0.2598
E	4.40	4.50	4.60	0.1732	0.1772	0.1811
D1	5.00	5.10	5.20	0.1969	0.2008	0.2048
E1	3.00	3.10	3.20	0.1181	0.1220	0.1260
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177