

### Features

- Input Supply Range  
TV MODE: 8.6V to 14.7V; MNT MODE: 4.3V to 6.0V
- AVDD Async-Boost Converter:  
TV MODE: 13.0V to 19.8V  
MNT MODE: 11.0V to 17.3V  
500/750KHz/1250KHz Switching Frequency  
5A Switching Current limit  
Controller by 0.3V Over-current Protection
- Programmable Internal/External V<sub>AVDD</sub> Isolation PMOS
- VBK Sync Buck Converter: 1.8V to 3.35V  
500/750KHz/1250KHz Switching Frequency  
2.0A Switching Current Limit
- HAVDD OP  
1 Channel Programmable HAVDD OP  
±500mA Peak Current  
±200mA Output Current  
7-bits DAC resolution
- VGH Async-Boost Converter/Charge pump Regulator:  
20V to 42V  
500/750KHz/1250KHz Switching Frequency  
1.5A Switching Current Limit  
Temperature Compensation: 20V to 42V
- VGL Async-Inverting Converter/Charge pump Regulator: -3V to -18V  
500/750KHz/1250KHz Switching Frequency  
1.5A Async Inverting Switching Current Limit  
Temperature Compensation: -3V to -18V
- VSS1 Negative Regulators: -3V to -16V
- 14-CH Gamma Buffers  
14 Channels Rail-to-Rail Programmable Gamma Buffers  
10 Bits Resolution for reach channel
- 1-CH VCOM1 Buffer  
1 Channel Programmable VCOM Buffer  
7-Bits Resolution for reach Channel
- 1-CH VCOM2 DAC  
1 Channel Programmable VCOM DAC  
7-Bits Resolution for reach Channel
- Invtegrated MTP Non-Volatile Memory
- Programmable Sequence Timing
- Over-Temperature Protection
- IIC Compatible Interface for Register Control
- Available in 6.5mmX4.5mm 46-pin QFN Package

### General Description

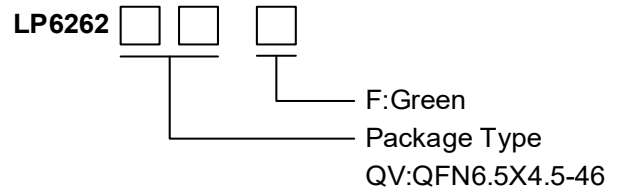
The LP6262 is a programmable multi-functional power solution with integrated gamma buffers, VCOM1 buffer for TFT-LCD. It contains one boost converter controller (AVDD), one ISO MOSFET controller for AVDD power on sequence, one buck converter (VBK), one boost converter/positive charge pump regulator (VGH) with the temperature compensation, one inverting converter/negative charge pump regulator (VGL) with the temperature compensation, one negative regulators (VSS1), 14-CH gamma buffers, 1-CH VCOM1 buffer, 1-CH VCOM2 DAC. All channel output level and sequence can be programmable by I2C interface and integrated Multiple-Time Programmable (MTP) non-volatile memory.

With its high current capabilities, the LP6262 is ideal for large screen LCD TV/MNT panel application with widely supply voltage range and also integrated complete protection functions including, OVP, UVP, OCP and OTP. The LP6262 available in a QFN6.5x4.5-46 pin package.

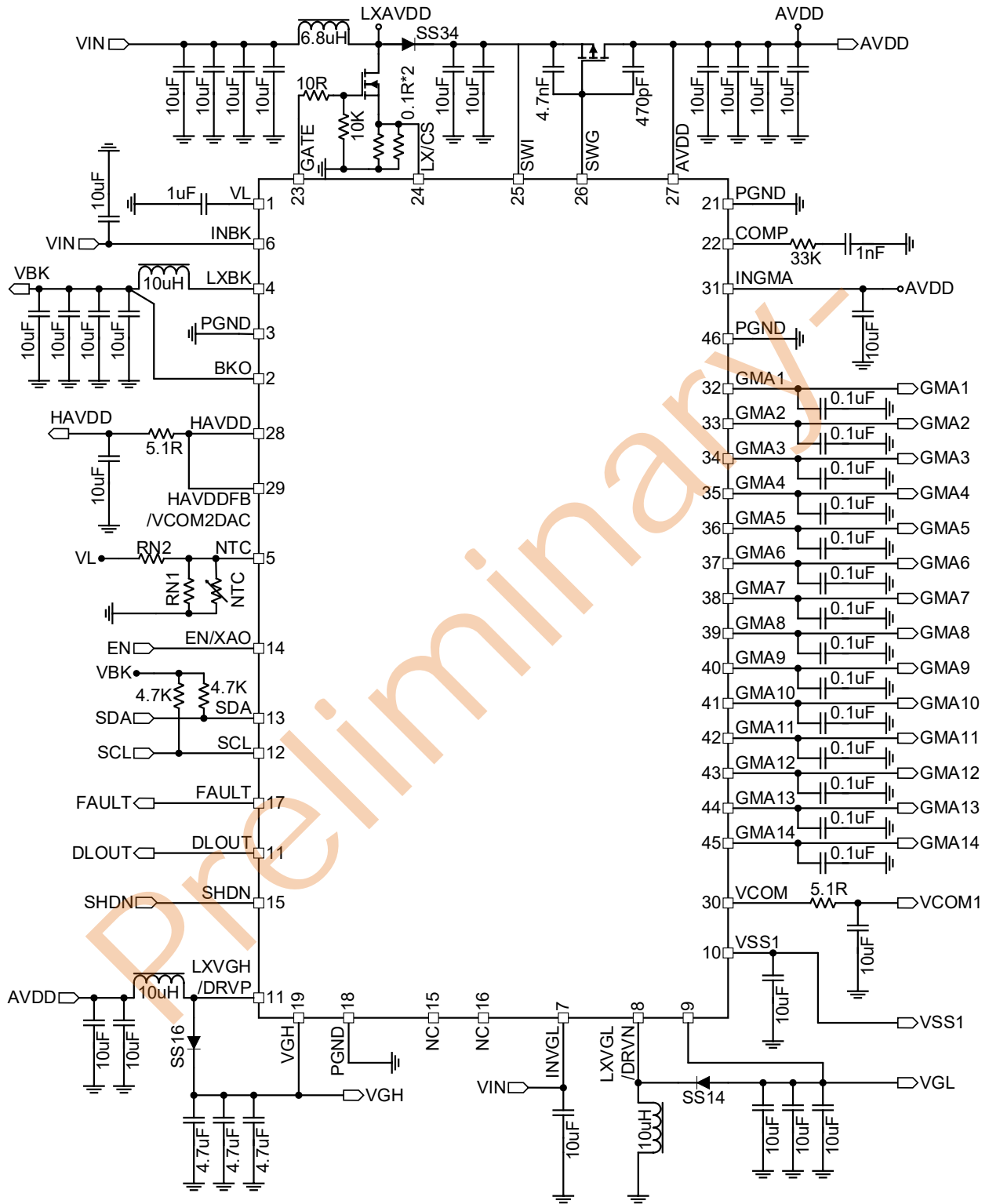
### Applications

- TFT LCD Monitor Panel
- TFT LCD TV Panel

### Order Information



## Typical Application Circuit



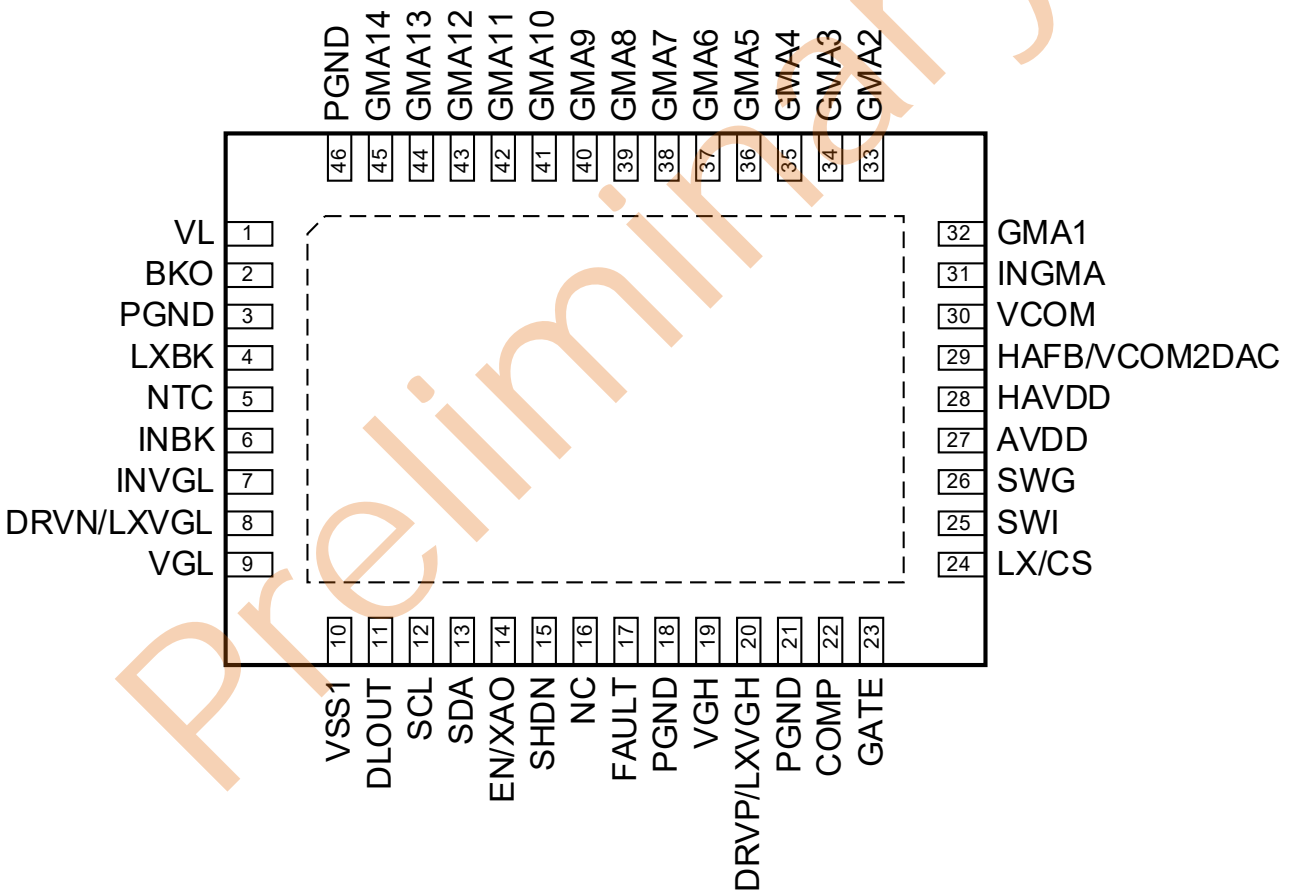
## Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6262QVF	LPS LP6262 YWX	MSL3	QFN6.5X4.5-46	3K/REEL

Marking indication:

Y: Year code. W: Week code. X: Batch numbers.

## Pin Diagram



### LP6262QVF QFN6.5X4.5-46

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

## Pin Description

Pin#	Name	Description
1	VL	5V internal linear regulator output
2	BKO	Feedback voltage input for VBK buck converter
3	PGND	Power Ground
4	LXBK	Switch node of the VBK Buck converter
5	NTC	Temperature compensation node, Connect NTC thermistor and resistors to this pin to control the slope of VGH/VGL/VCOM1 voltage for temperature compensation
6	INBK	Supply voltage input of VBK Buck converter
7	INVGL	Supply voltage input of the Inverting converter
8	DRVN/LXVGL	DRVN: VGL charge pump mode, for negative linear regulator base drive LXVGL: VGL Inverting mode, for switch node of the inverting converter
9	VGL	VGL charge pump mode, for feedback voltage input for VGL charge pump regulator VGL inverting mode, for feedback voltage input for VGL inverting converter
10	VSS1	Negative supply voltage output
11	DLOUT	Delay output signal of the Vcore enable.
12	SCL	Clock input pin of the IIC serial interface
13	SDA	Data input pin of the IIC serial interface
14	EN/XAO	@31h,bit7=0, Enable pin of the AVDD,VGH,HAVDD,VCOM1,VCOM2DAC and Gamma. Enable pin must be connect high signal. 400Kohm pull down resistor connect from this pin to ground @31h,bit7=1, XON pin for the shutdown reset function output and open drain voltage detector output.
15	SHDN	Sleep MODE Control, When SHDN is high Level, the chip goes into sleep mode
16	NC	Floating this pin, Do not connect to any other pin or circuit
17	FAULT	FAULT signal input/output pin. The FAULT pin is open drain output with internal pull up resistor. The output High/Low depended on protection functions. It also can be connected the open drain circuit to control IC operations. (1) Ouput channel UVP/SCP except VBK channel FAULT_O pin is Low active and all output channel shutdown except VBK (2) VBK UVP/SCP FAULT_O pin is Low active and all output channel shutdown (3) External signal FAULT_I pin is Low active and all output channel shutdown except VBK
18	PGND	Power ground
19	VGH	VGH charge pump mode, for feedback voltage input for VGH charge pump regulator VGH boost mode, for feedback voltage input for VGH boost converter
20	DRVP/LXVGH	DRVP: VGH charge pump mode, for positive linear regulator base drive LXVGH: VGH boost mode, for switch node of the boost converter
21	PGND	Power ground
22	COMP	Compensation pin for AVDD Boost converter
23	GATE	External N MOSFET gate driver for AVDD external mode
24	LX/CS	LX: Switch node of the AVDD boost converter for AVDD internal mode CS: External current sense for AVDD external mode
25	SWI	Source input of the AVDD Boost converter isolation P MOSFET
26	SWG	Gate driver of the AVDD Boost converter External isolation P MOSFET
27	AVDD	Drain output of the AVDD Boost converter isolation P MOSFET and Feedback voltage input of the AVDD Boost converter

## Pin Description(continued)

Pin#	Name	Description
28	HAVDD	Output of the AVDD OPAMP
29	HAFB/DAC	HAFB: Negative input of the HAVDD OPAMP VCOM2DAC: VCOM2 DAC output
30	VCOM1	VCOM1 operational amplifier output
31	INGMA	Supply voltage input of Gamma buffer and VCOM OP
32	GMA1	Gamma DAC analog output 1.
33	GMA2	Gamma DAC analog output 2.
34	GMA3	Gamma DAC analog output 3.
35	GMA4	Gamma DAC analog output 4.
36	GMA5	Gamma DAC analog output 5.
37	GMA6	Gamma DAC analog output 6.
38	GMA7	Gamma DAC analog output 7.
39	GMA8	Gamma DAC analog output 8.
40	GMA9	Gamma DAC analog output 9.
41	GMA10	Gamma DAC analog output 10.
42	GMA11	Gamma DAC analog output 11.
43	GMA12	Gamma DAC analog output 12.
44	GMA13	Gamma DAC analog output 13.
45	GMA14	Gamma DAC analog output 14.
46	PGND	Power ground
47	EPAD	Exposed pad. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation

## Absolute Maximum Ratings (Note1)

VL,BKO to PGND	-0.3V to +6V
LXBK to PGND	-0.3V to INBK1+0.3V
INBK,INVGL to PGND	-0.3V to +16.5V
DRVN/LXVGL to PGND	-20V to INVGL+0.3V
DRVN/LXVGL to INVGL	-40V to +0.3V
VGL to PGND	-20V to +0.3V
VSS1 to PGND	-20V to +0.3V
VGL to VSS1	-20V to +0.3V
DLOUT,SCL,SDA,EN/XAO,SHDN,FAULT to PGND	-0.3V to +6V
VGH to PGND	-0.3V to +50V
DRVP/LXVGH to PGND	-0.3V to +50V
COMP to PGND	-0.3V to +6V
GATE to PGND	-0.3V to +6V
LX/CS to GND	-0.3V to +24V
LX/CS to SWI	-0.3V to +24V
SWI to AVDD	-0.3V to +24V
SWI,SWG,AVDD to PGND	-0.3V to +24V
HAVDD, HAFB/VCOM2DAC to PGND	-0.3V to +24V
INGMA to PGND	-0.3V to +24V
VCOM1 to PGND	-0.3V to INGMA+0.3V
GMA1-14 to PGND	-0.3V to INGMA+0.3V
VGH to VGL,VSS1	-0.3V to +60V
AGND to PGND	-0.3V to +0.3V

**Note1:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Ratings (Note2)

HBM (Human Body Model)	2KV
MM (Machine Model)	200V
CDM (Charge Discharge Model)	500V

**Note2:** Devices are ESD sensitive. Handling precaution is recommended.

## Thermal Information

Junction Temperature (TJ)	150°C
Operating Junction Temperature Range (TJ)	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec)	260°C
$\theta_{JA}$ (Junction-to-Ambient Thermal Resistance)	TBD°C/W
$\theta_{JC}$ (Junction-to-Case Thermal Resistance)	TBD°C/W

## Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	Def.	MAX	UNIT
V <sub>IN</sub>	VIN Supply Range		8.6	12	14.7	V
	VIN Supply Range		4.3	5	6.0	V
V <sub>AVDD</sub>	AVDD Output Range1	Step:100mV <sub>REG 0x46[7]=0</sub>	13.0	17.6	19.8	V
	AVDD Output Range2	Step:100mV <sub>REG 0x46[7]=1</sub>	11	15.1	17.3	V
V <sub>BK</sub>	VBK Output Range	Step:50mV	1.8	3.3	3.35	V
V <sub>VGL</sub>	VGL Output Range	Step:250mV	-18	-12	-3.0	V
V <sub>VSS</sub>	VSS Output Range	Step:250mV	-16	-8	-3.0	V
V <sub>VGH</sub>	VGH Output Range	Step:1.0V	20	30	42	V
V <sub>HAVDD</sub>	HAVDD Output Range	Resolution:AVDD/512	192*Res4		319*Res4	V
V <sub>VCOM1</sub>	VCOM1 Output Range	Resolution: (Vcom.max-vcom.min)/127	V <sub>VCOM.MIN</sub>		Res1*127+ V <sub>VCOM.MIN</sub>	V
V <sub>VCOM2DAC</sub>	VCOM2DAC Output Range	Resolution: (Vcom.max-vcom.min)/127	V <sub>VCOM.MIN</sub>		Res1*127+ V <sub>VCOM.MIN</sub>	V
GMA1-14	GMA1-14 AVDD Range	AVDD/1024	0		V <sub>AVDD</sub> /1024 *1023	V
VGH <sub>VTC2</sub>	VGH&VGL VTC2	Step:0.2V	0.4	3.0	3.4	V
VGH <sub>VTC1</sub>	VGH&VGL VTC1	Step:0.2V	0.4	2.0	3.4	V
VCOM <sub>VTC2</sub>	VCOM VTC2	Step:0.2V	0.4	1.2	3.4	V
VCOM <sub>VTC1</sub>	VCOM VTC1	Step:0.2V	0.4	0.6	3.4	V
V <sub>XAO</sub>	XAO Discharge Threshold	Step:0.25V <sub>REG 0x46h[7]=0</sub>	6.5	7.00	10.25	V
	XAO Discharge Threshold	Step:0.14V <sub>REG 0x46h[7]=1</sub>	3.63	3.91	5.58	V

Power off discharge resistor

SYMBOL	PARAMETER	CONDITIONS	MIN	Def.	MAX	UNIT
R <sub>DIS_VBK</sub>	VBK power off discharge resistor	0x2Ch[6]=0	0.4	0.5	0.6	KΩ
R <sub>DIS_VBK</sub>	VBK power off discharge resistor	0x2Ch[6]=1	0.8	1.0	1.2	KΩ
R <sub>DIS_AVDD</sub>	AVDD power off discharge resistor	0x2Ch[5]=0	1.1	1.4	1.7	KΩ
R <sub>DIS_AVDD</sub>	AVDD power off discharge resistor	0x2Ch[5]=1	3.8	4.7	5.6	KΩ
R <sub>DIS_VGH</sub>	VGH power off discharge resistor	0x2Ch[4]=0	1.2	1.5	1.8	KΩ
R <sub>DIS_VGH</sub>	VGH power off discharge resistor	0x2Ch[4]=1	3.8	4.7	5.6	KΩ
R <sub>DIS_VGL</sub>	VGL power off discharge resistor	0x2Ch[3]=1	8	10	12	KΩ
R <sub>DIS_HAVDD</sub>	HAVDD power off discharge resistor	0x2Ch[2]=1	8	10	12	KΩ
R <sub>DIS_VCOM1</sub>	VCOM1 power off discharge resistor	0x2Ch[1:0]=01	16	20	24	Ω
R <sub>DIS_VCOM1</sub>	VCOM1 power off discharge resistor	0x2Ch[1:0]=10	0.8	1.0	1.2	KΩ
R <sub>DIS_VCOM1</sub>	VCOM1 power off discharge resistor	0x2Ch[1:0]=11	6.4	8.0	9.6	KΩ
R <sub>DIS_VSS</sub>	VSS power off discharge resistor	0x2Dh[7]=1	1.0	1.2	1.4	KΩ

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{AVDD} = 16V$ ,  $V_{BK} = 3.3V$ ,  $V_{HAVDD} = 8V$ ,  $V_{VGH} = 28V$ ,  $V_{VGL} = -10V$ ,  $V_{VSS1} = -6V$  with typical values  $T_A=25^\circ C$ )

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>GENERAL</b>						
$V_{IN}$	Input Voltage Range	Reg [46h] bit7=0	8.6		14.7	V
	Input Voltage Range	Reg [46h] bit7=1	4.3		6.0	V
$I_{QVINBK1}$	Quiescent Current into $V_{INBK1}$	Switching		5	9	mA
$I_{QVINVGL}$	Quiescent Current into $V_{INVGL}$	Switching		1	2	mA
$I_{QVINGMA}$	Quiescent Current into $V_{INGMA}$	Switching		9	12	mA
$I_{SLEEP}$	Sleep on Quiescent Current into $V_{IN}$	VL Shutdown		5	8	uA
$V_{INUVLO\_R}$	$V_{IN}$ under-voltage rising lockout Threshold Reg address=[46h] bit7=0	$V_{IN}$ rising	8.1	8.3	8.5	V
$V_{INUVLO\_HYS}$	$V_{IN}$ under-voltage hysteresis lockout Threshold Reg address=[46h] bit7=0	Hysteresis	700	800	900	mV
$V_{INUVLO\_R}$	$V_{IN}$ under-voltage rising lockout Threshold Reg address=[46h] bit7=1	$V_{IN}$ rising	4.1	4.2	4.3	V
$V_{INUVLO\_HYS}$	$V_{IN}$ under-voltage hysteresis lockout Threshold Reg address=[46h] bit7=1	Hysteresis	300	400	500	mV
$V_L$	VL Output Voltage	$V_{IN}=12V$	4.9	5.0	5.1	V
FOSC1	$V_{BK}, AVDD, VGH, VGL$ Frequency1	REG 0x29h[7] = 0 Acuracy +/-10%	650	750	850	KHz
FOSC2	$V_{BK}, AVDD, VGH, VGL$ Frequency2	REG 0x29h[7] = 1 Acuracy +/-10%	450	500	550	KHz
FOSC3	$V_{BK}, AVDD, VGH, VGL$ Frequency3	REG 0x29h[6] = 1 Acuracy +/-10%	1100	1250	1400	KHz
$T_{SD}$	Thermal Shutdown Protection	Rising	140	150	160	$^\circ C$
<b>LOGIC</b>						
$V_{IH}$	SDA/SCL/EN Input High Level		1.6			V
$V_{IL}$	SDA/SCL/EN Input Low Level				0.6	V
$I_{IH}, I_{IL}$	SDA/SCL Input Leakage Current	$V_I=0V$ or 3.3V	-1	0.01	+1	uA
$R_{PD}$	EN pull down resistor		320	400	480	K $\Omega$
	Input Capacitance			5		pF
$V_{OL}$	SDA Output Low Voltage	$I_{SINK}=6mA$	0.3			V

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{AVDD} = 16V$ ,  $V_{BK} = 3.3V$ ,  $V_{HAVDD} = 8V$ ,  $V_{VGH} = 28V$ ,  $V_{VGL} = -10V$ ,  $V_{VSS1} = -6V$  with typical values  $T_A=25^\circ C$ )

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ASYN. BOOST CONVERTER(AVDD)</b>						
$V_{AVDD1}$	AVDD output voltage range1	Reg[46h] bit7=0	13.0		19.8	V
$V_{AVDD2}$	AVDD output voltage range2	Reg[46h] bit7=1	11		17.3	V
	SWO Output Accuracy	AVDD=17.6V, No load	-2		+2	%
$R_{DS(ON)}$	N-MOSFET ON Resistance	$I_{LX/CS}=200mA$		100	250	m $\Omega$
$R_{DS(ON)}$	SYNC. P-MOSFET ON Resistance	$I_O=200mA$		0.6	1.0	$\Omega$
GM	Transconductance			200		$\mu A/V$
$R_{CS}$	Current-sense Transresistance		0.15	0.25	0.35	$\Omega$
$I_{LIM}$	N-MOSFET switch current limit	ILIMIT1 REG 0x00h[7]=0	5	6	7	A
		ILIMIT2 REG 0x00h[7]=1	2.5	3	3.5	A
$SS_{AVDD}$	Soft-start Period	Programmable softstart		10		ms
$I_{LEAK}$	Switch Leakage Current	$V_{LX/CS}=20V$		1	5	$\mu A$
$V_{OVP}$	SWI Over Voltage Protection	$V_{SWI}Rising, hysteresis=1v$	20.5	21.5	22.5	V
	AVDD Line Regulation	$V_{IN}=8.6V$ to $14.7V$ $I_{AVDD}=1mA$		0.04		%/V
	AVDD Load Regulation	$I_{AVDD}= 1mA$ to $1.5A$	-1		+1	%/A
	AVDD UVP Fault Trip Level	$V_{AVDD}$ Falling	80	85	90	%
	AVDD UVP fault timer duration			50		ms
$V_{SC}$	SWO Short Circuit Level	$V_{AVDD}$ Falling	15	20	25	%
	Maximum Duty Cycle		85	90		%
$V_{GOH}$	Gate Output Hi-level			SWI		V
$V_{GOL}$	Gate Oput Low-level			SWI-6		V
$R_{AVDD}$	Gate pull-high resistor		8	10	12	K $\Omega$
$I_{G\_SINK}$	Gate Sink Current			8	15	$\mu A$
$R_{SWO\_DCHG}$	Power off discharge resistance		3.8	4.7	5.6	K $\Omega$
<b>ISOLATION SWITCH</b>						
	SWI supply voltage range		8		20	V
$R_{DS(ON)}$	Isolation PMOS switch on resistance	$V_{SWI}=16.8V, I_{SW}=0.5A$		200	250	m $\Omega$
	Switch current		2	2.5	3	A
<b>External N-MOSFET Gate Drvier(Gate of AVDD)</b>						
$V_{GATE\_OH}$	Gate High Voltage		4.5	5	5.5	V
$V_{GATE\_OL}$	Gate Low Voltage		0		0.3	V
$V_{CS\_OCP}$	External NMOS Switch Current Limit	$R_{CS}=50m\Omega$	0.25	0.3	0.35	V
$R_{DSON\_GH}$	Gate to VL High-Side On Resistance			5		$\Omega$
$R_{DSON\_GL}$	Gate to GND Low-side On Resistance			5		$\Omega$

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ASYNCHRONOUS BOOST CONVERTER(VGH)</b>						
$V_{VGH\_NT}$	Adjustable Normal Temperature Output Voltage Range	Reg[03h],5bits/26 steps	20		42	V
$V_{VGH\_LT}$	Adjustable Low Temperature Output Voltage Range	Reg[04h],5bits/26 steps	20		42	V
	Output voltage tolerance	VGH=30V, No Load.	-2		+2	%
$R_{DS(ON)}$	Low-side NMOS Switch on resistance			0.45	0.65	$\Omega$
$I_{LIMIT}$	NMOS Switch Current Limit	ILIMIT1 REG 0x03h[7]=0	1.5	2	2.5	A
		ILIMIT2 REG 0x03h[7]=1	0.75	1	1.25	A
$I_{LEAK}$	NMOS Switch Leakage Current	$V_{LXVGH}=45V$		1	5	$\mu A$
	Line Regulation	$V_{AVDD}=8.6V$ to $14.7V$ $I_{GH}=0.1A$		0.1		%/V
	Load Regulation	$I_{GH}=1mA$ to $0.1A$		0.3		%/A
$T_{SS}$	Soft-start Time	Programmable softstart		3		ms
	Output OVP Fault-Trip Level	$V_{GH}$ rising, hysteresis:3V		45		V
	Output UVP Fault-Trip Level	$V_{GH}$ falling	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	$V_{GH}$ falling	15	20	25	%
$R_{DIS}$	Power off Discharge Resistance		24	30	36	K $\Omega$
<b>VGH CHARGE PUMP REGULATOR(VGH)</b>						
$V_{VGH\_NT}$	Adjustable Normal Temperature Output Voltage Range	Reg[03h],5bits/26 steps	20		42	V
$V_{VGH\_LT}$	Adjustable Low Temperature Output Voltage Range	Reg[04h],5bits/26 steps	20		42	V
	Output voltage tolerance	VGH=30V, No Load.	-2		+2	%
	DRVP Leakage Current	$V_{DRVP}=40V$		1	5	$\mu A$
	DRVP Sink Current	VGH=27V	7	10	15	mA
	DRVP Short Circuit Current	$V_{GH}<V_{GH}^*20\%$		400		$\mu A$
	Line Regulation	$V_{AVDD}=8.6V$ to $14.7V$ $I_{GH}=0.1A$		0.1		%/V
	Load Regulation	$V_{DRVP}=10V$ , $I_{DRVP}=50\mu A$ to $1mA$		0.4		%
	Soft-start Time	Programmable softstart		3		ms
	Output OVP Fault-Trip Level	$V_{GH}$ rising, hysteresis:1V	43	44	45	V
	Output UVP Fault-Trip Level	$V_{GH}$ falling		80		%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	$V_{GH}$ falling		20		%
$R_{DIS}$	Power off Discharge Resistance		24	30	36	K $\Omega$

## Electrical Characteristics

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VGL INVERTING CONVERTER(VGL)</b>						
$V_{VGL\_NT}$	Adjustable Normal Temperature Output Voltage Range	Reg[05h], 5bits/31 steps	-18		-3	V
$V_{VGL\_LT/HT}$	Adjustable Low/High Temperature Output Voltage Range	Reg[06h], 5bits/31 steps	-18		-3	V
$V_{VGL\_OFFSET}$	VGL_NT Output Offset	Reg[05h],bit7=1		-0.25		V
	Output Voltage Tolerance	VGL=-8.0V, No load.	-2		+2	%
	Maximum Duty Cycle		80	90		%
$R_{DS(ON)}$	PMOS Switch On-Resistance	$I_{VGL\_SW}=100mA$		0.5	0.6	$\Omega$
$I_{LIMIT}$	PMOS Switch Current Limit	ILIMIT1 REG 0x05h[6]=0	1.5	2.0	2.5	A
		ILIMIT2 REG 0x05h[6]=1	0.75	1.0	1.25	A
$I_{LEAK}$	PMOS Switch Leakage Current	$V_{VGL\_SW}=-16.0V$		1	5	$\mu A$
	Line Regulation	$V_{IN}=8.6V$ to $14.7V$ $I_{GL}=0.1A$		0.1		%/V
	Load Regulation	$I_{GL}=1mA$ to $200mA$		0.3		%/A
$T_{SS}$	Soft-start time			3		ms
	VGL Output OVP Fault-Trip Level	$V_{GL}$ falling, hysteresis:110%	115	120	125	%
	VGL Output UVP Fault-Trip Level	$V_{GL}$ rising	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	$V_{GL}$ rising	15	20	25	%
$R_{DIS}$	Power off Discharge Resistance		8	10	12	K $\Omega$
<b>VGL CHARGE PUMP REGULATOR(VGL)</b>						
$V_{VGL\_NT}$	Adjustable Normal Temperature Output Voltage Range	Reg[05h], 5bits/31 steps	-18		-3	V
$V_{VGL\_LT/HT}$	Adjustable Low/High Temperature Output Voltage Range	Reg[06h], 5bits/31 steps	-18		-3	V
$V_{VGL\_OFFSET}$	VGL_NT Output Offset	Reg[05h],bit7=1		-0.25		V
	Output Voltage Tolerance	VGL=-8.0V, No load.	-2		+2	%
	DRVN Leakage Current	$V_{DRVN}=-16V$		1	5	$\mu A$
	DRVN Source Current		10	20	30	mA
$I_{DRVN\_SC}$	DRVN Short Circuit Current	$V_{GL}>V_{GL}*20\%$		400		$\mu A$
$T_{SS}$	Soft-start Time			3		ms
	Output OVP Fault-Trip Level	$V_{GL}$ falling, hysteresis:0.5v	115	120	125	%
	Output UVP Fault-Trip Level	$V_{GL}$ rising	75	80	85	%
	UVP fault timer duration			50		ms
	Output SCP Fault-Trip Level	$V_{GL}$ rising	15	20	25	%
$R_{DIS}$	Power off Discharge Resistance		8	10	12	K $\Omega$

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{AVDD} = 16V$ ,  $V_{BK} = 3.3V$ ,  $V_{HAVDD} = 8V$ ,  $V_{VGH} = 28V$ ,  $V_{VGL} = -10V$ ,  $V_{VSS1} = -6V$  with typical values  $T_A=25^{\circ}C$ )  
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at  $+25^{\circ}C$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VSS1 NEGATIVE REGULATOR(VSS1)</b>						
VSS1	Adjustable Output Voltage Range	Reg[07h], 5bits/27 steps	-16		-3	V
VSS <sub>OFFSET</sub>	VSS Output Offset	Reg[07h],bit6=1		-0.25		V
	Output Voltage Tolerance	VSS1=-6.0V, No load.	-2		+2	%
I <sub>LIMIT</sub>	Current Limit		50	100		mA
T <sub>SS</sub>	Soft-start Time			3		ms
	Output UVP Fault-Trip Level	V <sub>SS1</sub> falling	75	80	85	%
	UVP fault timer duration			50		ms
INL	Integral Nonlinearity	No load	-1		+1	LSB
DNL	Differential Nonlinearity	No load	-1		+1	LSB
	Load Regulation	I <sub>VSS1</sub> =-50mA to 50mA		±0.5		mV/ mA
R <sub>DIS</sub>	Power off Discharge Resistance		1	1.2	1.4	KΩ
<b>THERMAL COMPENSATION(VGH&amp;VGL&amp;VCOM1)</b>						
VTC1	VGH&VGL lower bound voltage of VTC1	Reg[2Eh], 4bits/16 steps	0.4		3.4	V
VTC2	VGH&VGL upper bound voltage of VTC2	Reg[2Eh], 4bits/16 steps	0.4		3.4	V
VCOM1 <sub>VTC1</sub>	VCOM lower bound voltage of VTC1	Reg[2Fh], 4bits/16 steps	0.4		3.4	V
VCOM1 <sub>VTC2</sub>	VCOM upper bound voltage of VTC2	Reg[2Fh], 4bits/16 steps	0.4		3.4	V
<b>SYNC BUCK CONVERTER(VBK)</b>						
VBK	VBK Output Voltage Range	Reg[01h], 5bits/32 steps	1.8		3.35	V
	Output Voltage Tolerance	VBK=3.3V, No load.	-1		+1	%
	Maximum Duty Cycle		85	90		%
R <sub>DS(ON)_HS</sub>	High-side PMOS switch on resistance	I <sub>LXBK1</sub> =500mA		400	600	mΩ
R <sub>DS(ON)_LS</sub>	Low-side NMOS switch on resistance	I <sub>LXBK1</sub> =-500mA		200	400	mΩ
I <sub>LIMIT</sub>	High-side PMOS switch current limit		2.0	2.5	3.0	A
I <sub>PEAK_HS</sub>	High-side switch leakage current	V <sub>LXBK1</sub> =0V		1	5	μA
I <sub>PEAK_LS</sub>	Low-side switch leakage current	V <sub>LXBK1_SW</sub> =14V		1	5	μA
	Line Regulation	V <sub>IN</sub> =8.6V to 14.7V I <sub>VBK</sub> =500mA		0.05		%/V
	Load Regulation	I <sub>VBK</sub> =1mA to 2.0A	-1		+1	%
T <sub>SS</sub>	Soft-start Time			3		ms
	Output OVP Fault-Trip Level	V <sub>VBK</sub> rising	115	120	125	%
	Output UVP Fault-Trip Level	V <sub>VBK</sub> falling	75	80	85	%
	UVP fault timer duration	V <sub>VBK</sub> falling		50		ms
	Output SCP Fault-Trip Level		15	20	25	%
R <sub>DIS</sub>	Power off Discharge Resistance		0.8	1	1.2	KΩ

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{AVDD} = 16V$ ,  $V_{BK} = 3.3V$ ,  $V_{HAVDD} = 8V$ ,  $V_{VGH} = 28V$ ,  $V_{VGL} = -10V$ ,  $V_{VSS1} = -6V$  with typical values  $T_A=25^\circ C$ )  
 The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>HAVDD OPAMP(HAVDD)</b>						
	HAVDD voltage resolution			7		bits
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	HAVDD=1/2*AVDD No load	-2		+2	LSB
VOH	Output voltage swing high	I <sub>HAVDD</sub> =+100mA		V <sub>VAA</sub> -2		V
VOL	Output voltage swing low	I <sub>HAVDD</sub> =-100mA		2	2.5	V
I <sub>OUT</sub>	Output Continuous Current	HAVDD=1/2*AVDD	±200	±250	±300	mA
I <sub>sc</sub>	Short Circuit Current		±50		±100	mA
CMRR	Input common-mode rejection ratio	AVDD=15V,f=10KHz 2V amplifude sin signal		80		dB
PSRR	Power supply rejection ratio	AVDD sweeps from 8V to 18V		60		dB
SR	Slew rate			45		V/us
BW	-3dB bandwidth			20		MHz
	Output OVP Fault-Trip Level	V <sub>HAVDD</sub> rising	115	120	125	%
	Output UVP Fault-Trip Level	V <sub>HAVDD</sub> falling	75	80	85	%
R <sub>Dis</sub>	Power off Discharge Resistance			10		KΩ
<b>GAMMA BUFFERS(GMA1 TO GMA14)</b>						
V <sub>SWO_GMA</sub>	Supply Range		11		19.8	V
	Gamma Voltage Resolution	GMA1 to 14, 10bits/1024 steps		V <sub>AVDD</sub> / 1024		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	GMA=1/2 code No load	-2		+2	LSB
V <sub>GMA1-14</sub>	Output Voltage Range	I <sub>GMA1 to 14</sub> =sinking or source 5mA	GND +0.2		V <sub>AVDD</sub> -0.2	V
I <sub>OUT</sub>	Output Current (setting 14ch gma)	V <sub>GMA1 to 14</sub> drop 0.5V	±50	±75	±100	mA
I <sub>sc</sub>	Short Circuit Current (setting 14ch gma)	V <sub>GMA1 to 14</sub> to V <sub>SWO_GMA</sub> or V <sub>GMA1 to 14</sub> to GND	±10	±20	±30	mA
I <sub>OUT</sub>	Output Current (1,7,8,14 4ch)	V <sub>GMA1 to 14</sub> drop 0.5V	±100	±150	±200	mA
I <sub>sc</sub>	Short Circuit Current (1,7,8,14 4ch)	V <sub>GMA1 to 14</sub> to V <sub>SWO_GMA</sub> or V <sub>GMA1 to 14</sub> to GND	±20	±40	±60	mA
T <sub>D_GMA</sub>	Program to Output Delay	From ACK falling edge to programming gamma change 50% voltage at output		15		us
	Load Regulation	I <sub>GMA1 to 14</sub> =-12mA to 12mA		±0.5+ Rd		mV/ mA

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{AVDD} = 16V$ ,  $V_{BK} = 3.3V$ ,  $V_{HAVDD} = 8V$ ,  $V_{VGH} = 28V$ ,  $V_{VGL} = -10V$ ,  $V_{VSS1} = -6V$  with typical values  $T_A = 25^\circ C$ )

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VCOM1 BUFFERS &amp; VCOM2 DAC(VCOM1&amp;VCOM2)</b>						
$V_{SWO\_GMA}$	Supply Range		11		19.8	V
$V_{VCOM1\_NT}/$ $V_{VCOM2DAC}$	Adjustable Normal Temperature Output Voltage Range	Reg[08h], 7bits/128 steps Res1=(vcom.max-vcom.min)/127	0*res 1+ vcom .min		127*res 1+ vcom .min	V
$V_{VCOM1\_HT}$	Adjustable Low Temperature Output Voltage Range	Reg[09h], 7bits/128 steps Res1=(vcom.max-vcom.min)/127	0*res 1+ vcom .min		127*res 1+ vcom .min	V
$V_{VCOM\_MAX}$	Adjustable VCOM_MAX	Reg[0Ah],7bits/128 steps	1* $V_{AVDD}/128$		128* $V_{AVDD}/127$	V
$V_{VCOMMIN}$	Adjustable VCOM_MIN	Reg[0Bh],7bits/128 steps	0* $V_{AVDD}/128$		127* $V_{AVDD}/127$	V
	VCOM1&VCOM2DAC voltage resolution	VCOM1&VCOM2DAC will be clamped between vcom.max and vcom.min		$V_{AVDD}/128$		V
INL	Integral Nonlinearity	No load	-4		+4	LSB
DNL	Differential Nonlinearity	No load	-2		+2	LSB
$V_{VCOM1}$ $V_{VCOM2DAC}$	Output Voltage Range	VCOM1&VCOM2DAC will be clamped between vcom.max and vcom.min	GND +0.5		$V_{AVDD}$ -0.5	V
$T_{D\_VCOM1}$ $T_{D\_VCOM2DAC}$	Program to Output Delay	From ACK falling edge to programming VCOM change 50% voltage at output		1		us
$I_{OUT}$	VCOM1 Output Continuous Current		$\pm 200$	$\pm 250$	$\pm 300$	mA
$I_{sc}$	VCOM1 Short Circuit Current		$\pm 50$		$\pm 100$	mA
	Load Regulation	$I_{VCOM1} = -100mA$ to $100mA$	-1		+1	mV/ mA
$R_{DIS}$	Power off Discharge Resistance	Reg[2Ch], 2bits/4 steps	dis		8	K $\Omega$
<b>FAULT SIGNAL(FAULT)</b>						
$R_{FAULT}$	FAULT Pull Up Resistance	Up to VL(VBK ok detect)	80	100	120	K $\Omega$
$V_{FAULT\_HIV}$	FAULT High Level Input Voltage		2			V
$V_{FAULT\_LIV}$	FAULT Low Level Input Voltage				1	V
	FAULT ON Voltage	$I_{IN} = 3mA$			0.5	V



















































































