LP3201H

5V/1.0A Synchronous BUCK Switching Converter

Features

- Input voltage range: 2.7V~ 5.5V
- Output voltage range: 0.6V ~VIN
- High efficiency operation
  - Integrated a 120mΩ LS-MOSFET and a 200mΩ HS-MOSFET for SOT23-5/-6 package
  - Integrated a 130mΩ LS-MOSFET and a 215mΩ HS-MOSFET for SOT563 package
  - More than 90% efficiency at 1A load from 5V to 3.3V conversion
- Automatic PFM mode at light load
- ±1.5% V_{REF} accuracy at 25℃
- Low quiescent current: 40μA
- Shutdown current <1μA
- Pseudo fixed 1.5MHz switching frequency
- Adaptive COT control scheme with fast load transient response
- PG output
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- 0.4ms typical soft-start time
- Auto-discharge
- SOT23-5, SOT23-6 and SOT563 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV
- Set-top Box
- WIFI
- Battery powered devices

General Description

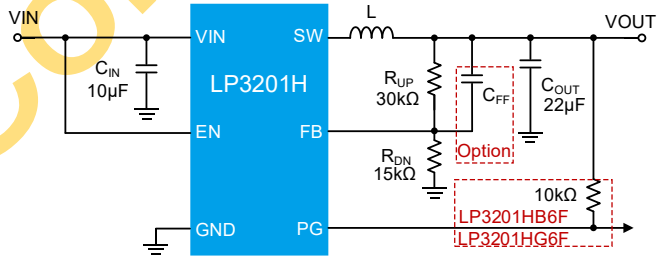
The LP3201H is a synchronous buck converter supporting up to 1.0A output current. The LP3201H employs an adaptive constant-off-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP3201H supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP3201H integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP3201H also integrates multiple protection functions, i.e., over current protection (OCP), over temperature protection (OTP), under voltage lockout (UVLO), and short circuit protection (SCP).

The LP3201H is available in a small SOT23-5, SOT23-6 and SOT563 package.

Typical Application Circuit



Order Information

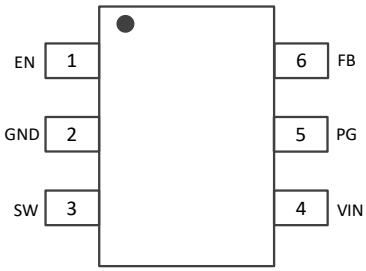
LP3201H □□ □

- F: Pb Free
- Package Type
  - B5: SOT23-5
  - B6: SOT23-6
  - G6: SOT563

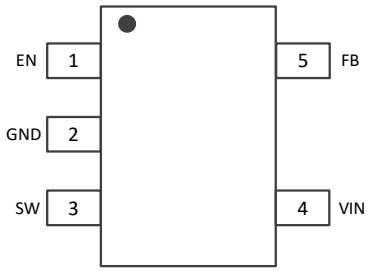
Device Information

Part Number	Top Marking	Operation Mode	Moisture Sensitivity Level	Package	Shipping
LP3201HB5F	**LPS** **A1YWX**	**PFM/PWM**	**LEVEL 3**	**SOT23-5**	**3K/REEL**
LP3201HG6F	**LPS** **H2YWX**	**PFM/PWM**	**LEVEL 3**	**SOT563**	**3K/REEL**
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

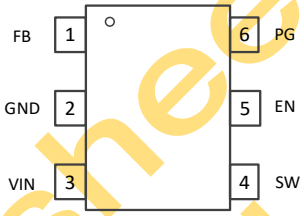
Pin Diagram



SOT23-6（top view）



SOT23-5（top view）



SOT563（top view）

Pin Description

Pin			Name	Description
SOT23-6	SOT23-5	SOT563		
1	1	5	EN	Enable pin. Active high. Logic low disables the device. Do not leave the pin floating.
2	2	2	GND	Ground pin.
3	3	4	SW	Switching node of the converter. Connect the inductor to this pin.
4	4	3	VIN	Power supply voltage pin. Must be closely decoupled to GND with a capacitor. Place the capacitor as close as to the pin as possible.
5	-	6	PG	Power Good. Open drain output, if not used, leave the pin floating.
6	5	1	FB	Feedback pin. Use a resistor divider to set the output voltage.

Absolute Maximum Ratings (Note 1)

VIN, SW, EN Pin to GND ---------- -0.3~6.5V
SW Pin to GND (5ns transient) ---------- -2~8V
Maximum Junction Temperature (T_J) ---------- 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 125℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

HBM (Human Body Model) ---------- 2kV
CDM (Charged Device Model) ---------- 500V

Thermal Information (Note 2)

θ_{JA} (Junction-to-Ambient Thermal Resistance, SOT23-5/SOT23-6) ---------- 160℃/W
θ_{JA} (Junction-to-Ambient Thermal Resistance, SOT563) ---------- 140℃/W

Note 2. Measured using 2S2P JEDEC standard PCB.

Recommended Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	2.7		5.5	V
V_{OUT}	Output voltage	0.6		VIN	V
L	Inductor	0.7		3.3	μH
T_A	Ambient temperature range	-40		85	°C
C_{IN}	Input decoupling capacitor, effective capacitance	4.7		100	μF
C_{OUT}	Output capacitor, effective capacitance	10		100	μF

Electrical Characteristics

(The specifications are measured under conditions V_{IN} = 5V, L=2.2μH, C_{IN} =10μF, C_{OUT} = 22μF, T_J = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_R}	Input under voltage lockout threshold	V_{IN} rising threshold	2.3	2.4	2.5	V
V_{ULVO_H}	UVLO hysteresis	V_{IN} falling		0.1		V
t_{UVLO}	UVLO deglitch time			32		μs
I_{Q_VIN}	Input quiescent current	No switching, EN=3V, FB=1.0V		40	80	μA
I_{SD_VIN}	Input shutdown current	No switching, EN=0V		0.1	1	μA
BUCK CONVERTER						
I_{LIM_PEAK}	High-side peak current limit			1.7		A
I_{LIM_VALLEY}	Low-side valley current limit			1.0		A
I_{ZCD}	Zero current detection	PFM	0.05	0.1	0.15	A
V_{REF}	Reference voltage	T_J=25°C	0.591	0.6	0.609	V
R_{DSON_HS}	High-side FET on resistance	SOT23-5/SOT23-6 package		200		mΩ
		SOT563 package		215		mΩ
R_{DSON_LS}	Low-side FET on resistance	SOT23-5/SOT23-6 package		120		mΩ
		SOT563 package		130		mΩ
F_{sw}	Switching frequency			1500		kHz
t_{EN_DLY}	EN delay time	EN turn high to first switching cycle		100	200	μs
t_{ss}	Soft start time	From 1st switching cycle to 95%V_{ref}		400		μs
t_{SCP}	SCP deglitch time[1]	SCP deglitch time		32		cycle
Thermal Shutdown						
T_{SD_R}	Shutdown temperature threshold	Rising threshold		155		°C
T_{SD_F}	Recovery temperature threshold	Falling threshold		135		°C

EN and PG						
V_{EN_H}	EN high threshold	Rising threshold	1.2			V
V_{EN_L}	EN low threshold				0.4	V
R_{EN_PD}	EN pin pull-down resistance			1000		kΩ
R_{DIS}	SW discharge FET on-resistance	EN=0		1		kΩ
$V_{FB\_PG\_R}$	FB High threshold to trigger PG output	FB rising, reference to VREF		95		%
$V_{FB\_PG\_F}$	FB low threshold to trigger PG output	FB falling reference to VREF		90		%
t_{FB_PG}	PG deglitch	FB rising/falling	5	10	15	μs
R_{ON_PG}	PG FET discharge on-resistance				10	Ω

Typical Characteristics

(T_J = 25℃, V_{IN}=3.3V, R_{UP}=30kΩ, R_{DOWN}=15kΩ,V_{OUT}=1.8V, C_{IN}=10μF, C_{OUT}=22μF, L=2.2μH, unless otherwise noted.)

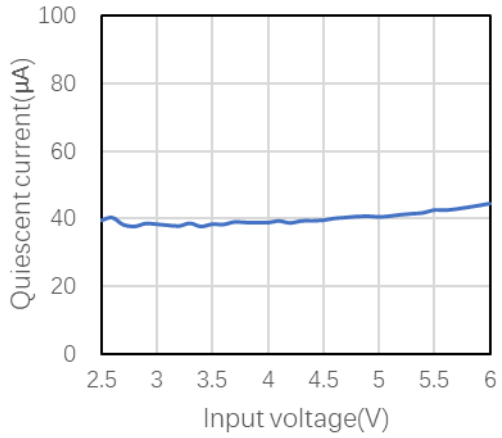


Figure 1 Quiescent vs Input Voltage

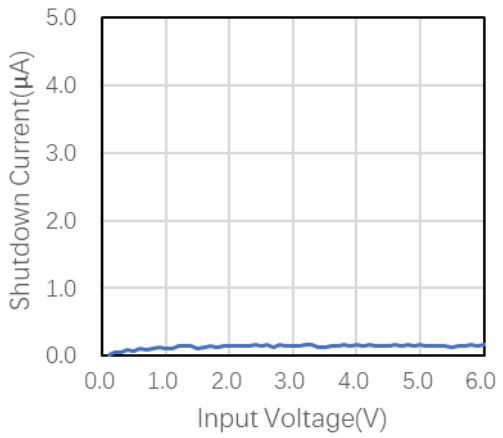


Figure 2. Shutdown Current vs Input Voltage

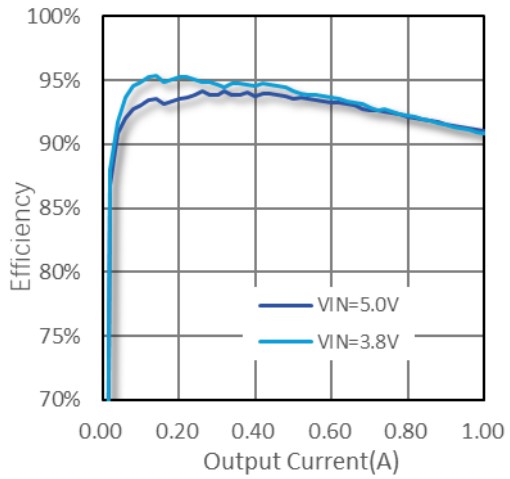


Figure 3 Efficiency vs Output Current
R_{UP}=54kΩ, R_{DOWN}=12kΩ, V_{OUT}=3.3V, SOT23-5 pkg

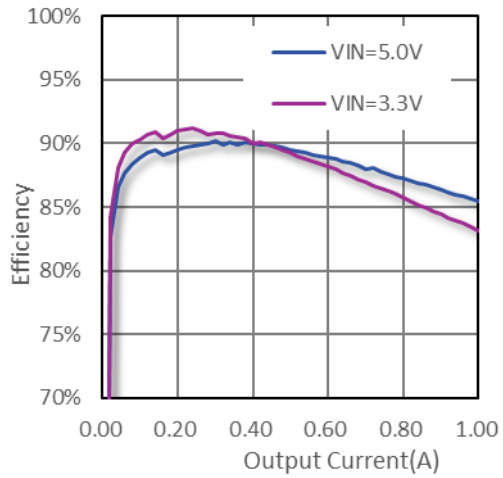


Figure 4 Efficiency vs Output Current
R_{UP}=30kΩ, R_{DOWN}=15kΩ, V_{OUT}=1.8V, SOT23-5 pkg

Start up and Turn off Waveform:

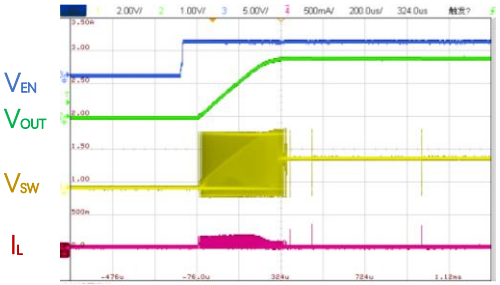


Figure 5 Start up with EN on, no load

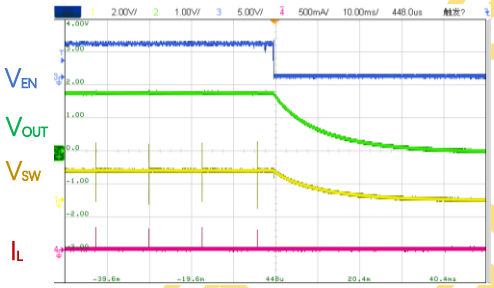


Figure 6 Turn off with EN off, no load

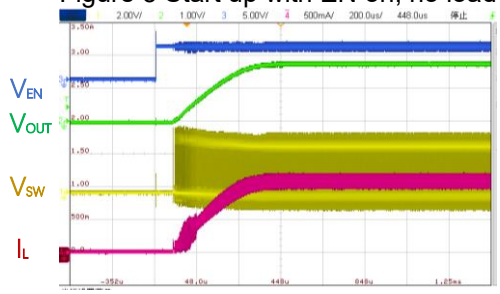


Figure 7 Start up with EN on, Rload=1.8Ω

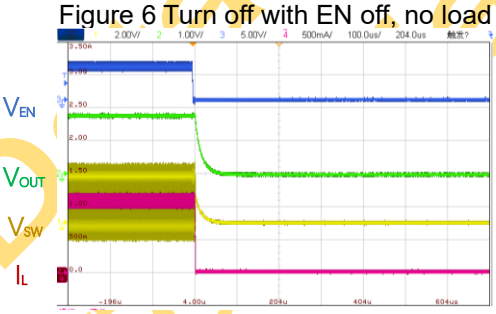


Figure 8 Turn off with EN off, Rload=1.8Ω

PWM operation Waveform:

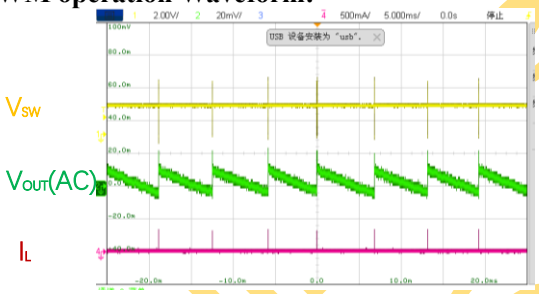


Figure 9. PWM operation with 1mA load,

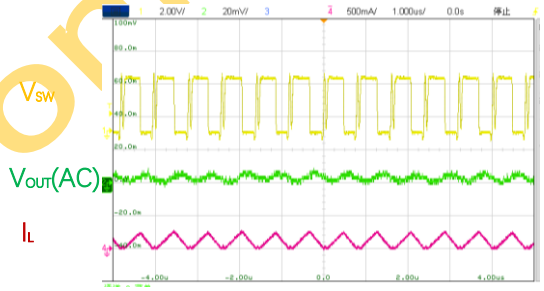


Figure 10. PWM operation with 100mA load

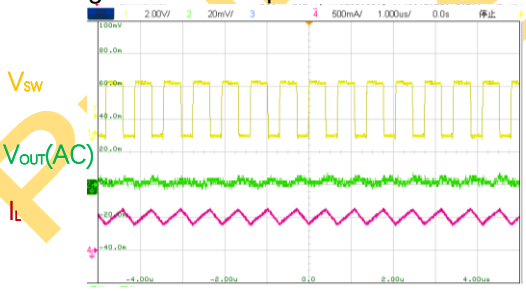


Figure 11. PWM operation with 500mA load,

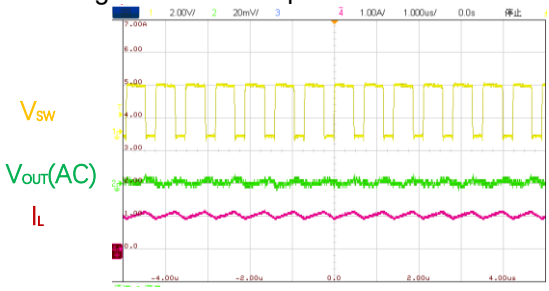


Figure 12. PWM operation with 1A load,

Typical Characteristics(continued)

(T_J = 25℃, V_{IN}=3.3V, R_{UP}=30k, R_{DOWN}=15k,V_{OUT}=1.8V, C_{IN}=10μF, C_{OUT}=22μF, L=2.2μH, unless otherwise noted.)

Load Transient:

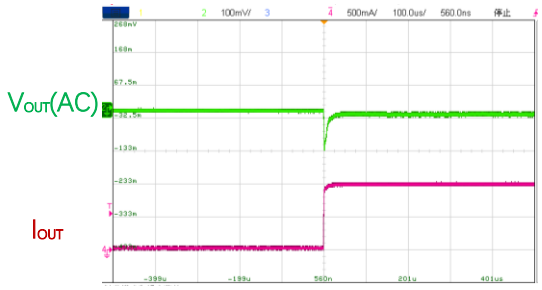


Figure 13. Load Transient no load->1A, CFF=0,

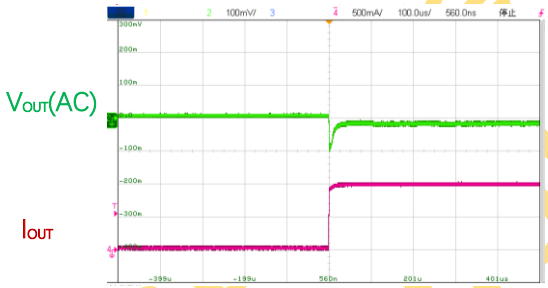


Figure 14. Load Transient no load->1A, CFF=20pF,

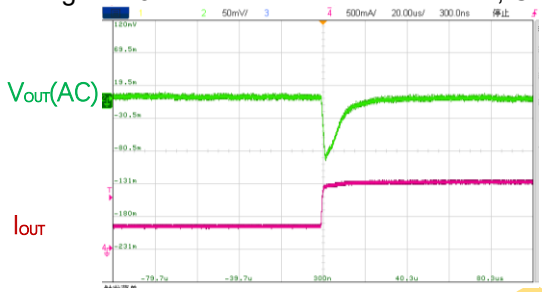


Figure 15. Load Transient 300mA->1A, CFF=0,

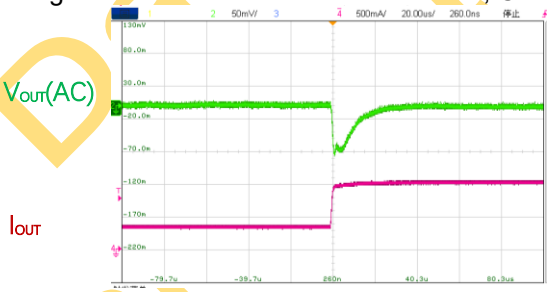
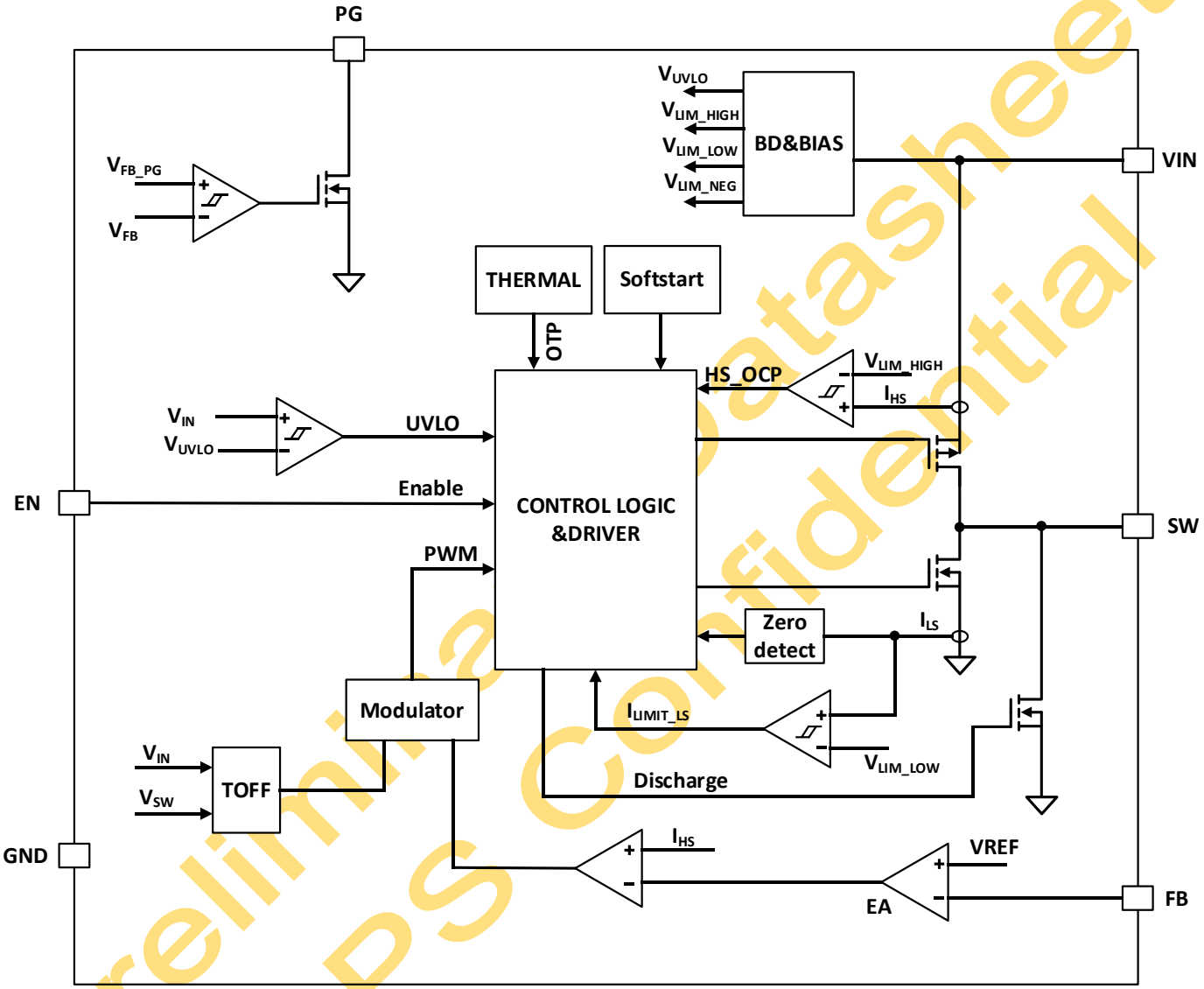


Figure 16. Load Transient 300mA->1A, CFF=20pF,

Functional Block Diagram



Detailed Description

Overview

The LP3201H is a 1.0A synchronous buck converter, supporting 2.7-5.5V input voltage range. The adaptive COT(constant-off-time) control scheme enables fast transient respond and minimizes the output capacitance. The LP3201H supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP3201H automatically transfers between PFM and PWM according to the output current.

Under Voltage Lockout (UVLO)

When the input voltage VIN is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP3201H can be enabled by the EN pin.

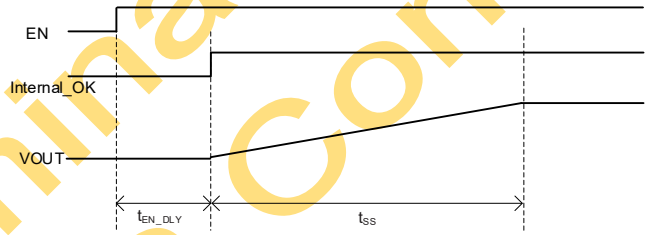
EN Control

The EN pin can be used to control the system power-up sequence. When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold, the LP3201H enables all the internal circuits, delays for 100us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1000kΩ pull-down resistor to ground.

Soft-start

The LP3201H integrates soft-start function with a typical time of 0.4ms (t_{ss}) . After passing the UVLO threshold and enabled by the EN pin with the 100us delay(t_{EN_DLY}), the internal reference voltage ramps from zero to the V_{REF} in 0.4ms and the output voltage ramps up accordingly.



Soft Start Sequence

Constant OFF Time (COT) Control Scheme

The LP3201H integrates the peak current and COT control scheme for pseudo-fixed-frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal off-time (TOFF) generator block monitors the V_{IN} and V_{SW} voltage and turns on the high-side MOSFET to start a switching cycle, when the TOFF timer time expires.

Then, the high-side current (I_{HS}) is monitored and the LP3201H turns off the high-side MOSFET when I_{HS} reaches the error amplifier output voltage.

PFM Operation

The LP3201H is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

Over Current Protection and Short Circuit Protection

The LP3201H protects an over current situation by limiting the both the inductor peak and valley current. The current of low-side MOSFET is monitored when low-side FET is turned ON and the current of high-side is monitored when the high-side FET is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side

valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit pluses a half of the inductor ripple current. The high-side is turned off immediately when the peak current reaches the threshold.

The SCP is realized by monitoring the high-side or low-side current limit. Once the output load draws more current than the current limit, the output voltage drops. When the current limit continues for 32 cycles, the LP3201H shutdowns. The LP3201H restarts after a typical 80us delay. If the SCP condition still holds after soft-start, the LP3201H shutdown again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

Power Good (LP3201HB6F/G6F only)

The LP3201HB6F/G6F integrates power good indicator. When the FB voltage is lower than 90% V_{REF}, PG is pulled to GND by internal circuit. The PG recovers when the FB rises above 95%V_{REF}. A 10kΩ~100kΩ resistor is recommended to connect between V_{OUT} and PG pin. The PG-FET on-resistance is 10Ω.

Active output discharge

The output capacitor is discharged by EN is low, V_{OUT} is not ready or under fault conditions. The resistance between SW and GND is 1000Ω typically.

Output Discharge Logic Table

EN State	Thermal Shutdown	Output Discharge
EN=Low	No thermal shutdown	YES
EN=High		NO
EN=Low	Thermal shutdown	YES
EN=High		YES

Thermal Shutdown

The LP3201H has a thermal protection function. The device will shut down when the internal temperature is higher than 155°C and will restart after the temperature drops below 135°C.

Application Information

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1\right) \times V_{REF}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V.

For better accuracy, the R_{DOWN} is recommended to be lower than 100kΩ to ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current.

For a 1.8V-output application, a 15kΩ R_{DOWN} is selected and the R_{UP} is 30kΩ.

Inductor and Output Capacitor Setting

The inductor ripple of CCM is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * F_{SW}} * \frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.

For a typical 5V input voltage and 3.3V output voltage, a low DCR value, 2.2uH inductor is recommended.

The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor CFF can be selected to improve the transient behavior. The typical capacitance can be 20~100pF.

V_{OUT}	Inductor-L	C_{OUT}	R_{UP}	R_{DOWN}	C_{FF}
1.2V	2.2uH	22uF	15 kΩ	15 kΩ	0-100pF
1.8V	2.2uH	22uF	30 kΩ	15 kΩ	0-100pF
3.3V	2.2uH	22uF	54 kΩ	12 kΩ	0-100pF

Input capacitor

A typical higher than 10μF ceramic capacitor is needed to serve as the bulk capacitor at the VIN pin of the LP3201H. An additional 0.1uF is strongly recommended to provide additional high frequency filtering and should be placed to the VIN pin and GND as close as possible.

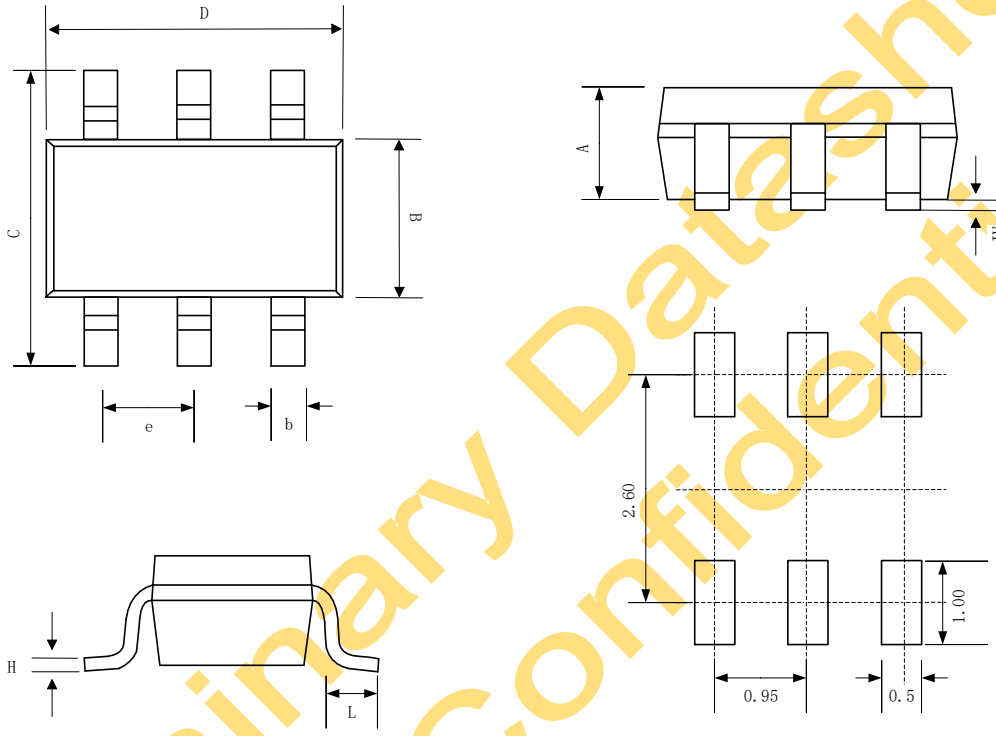
PCB Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

Packaging Information

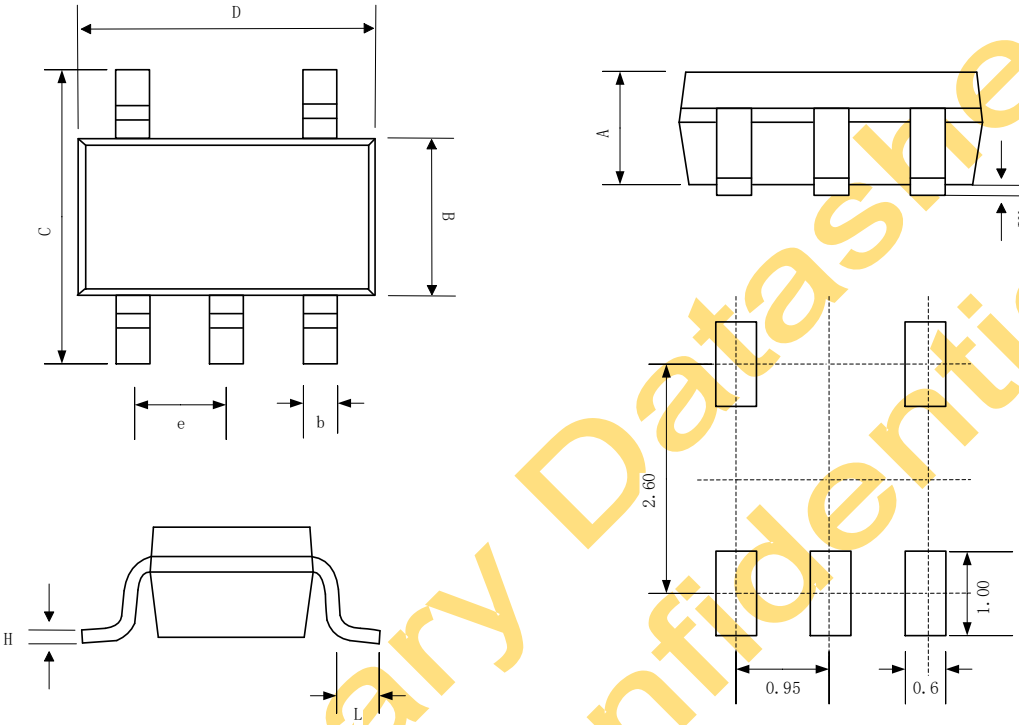
SOT23-6



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

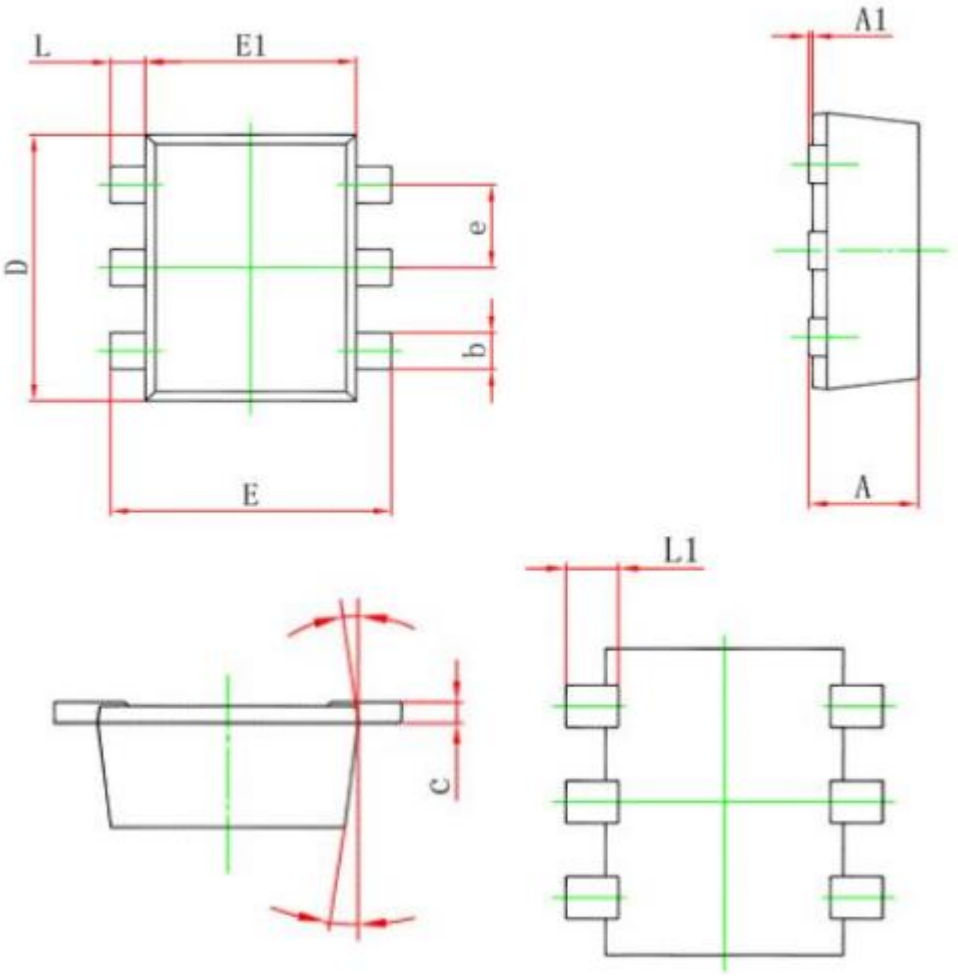
SOT23-5



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

SOT563

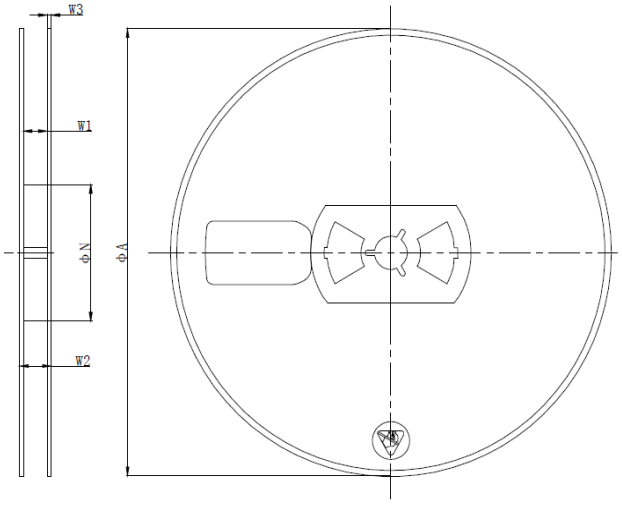


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	0.025	0.050
e	0.450	0.500	0.550
c	0.100	0.150	0.200
D	1.500	1.600	1.700
b	0.150	0.250	0.350
E1	1.100	1.200	1.300
E	1.500	1.600	1.700
L	0.100	0.200	0.300
L1	0.200	0.300	0.400
θ	7° REF		

Tape and Reel Information

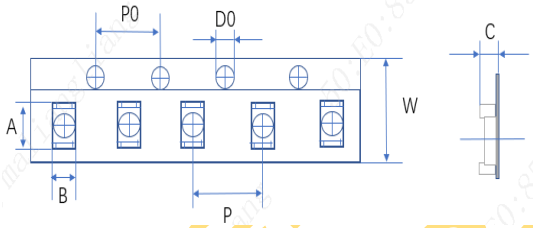
SOT23-5&SOT23-6

REEL DIMENSIONS



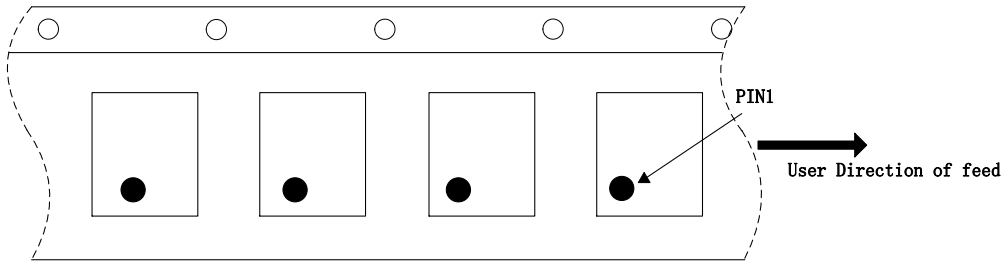
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



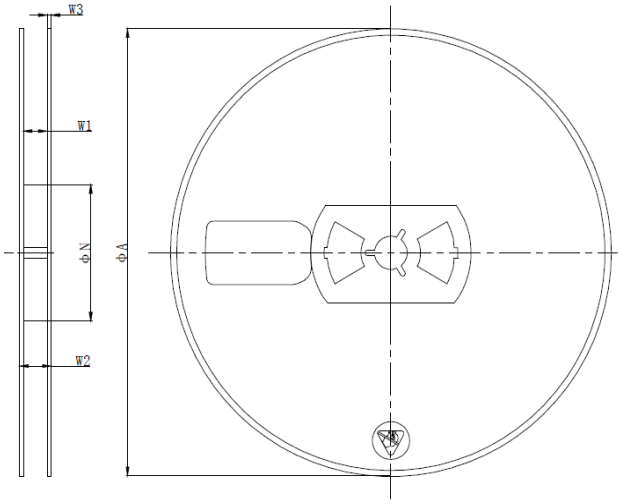
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	3.06	3.26	3.46
P0	3.90	4.00	4.10
P	3.90	4.00	4.10
D0	1.35	1.50	1.65
W	7.70	8.00	8.30
C	1.20	1.40	1.60

PIN1 AND TAPE FEEDING DIRECTION



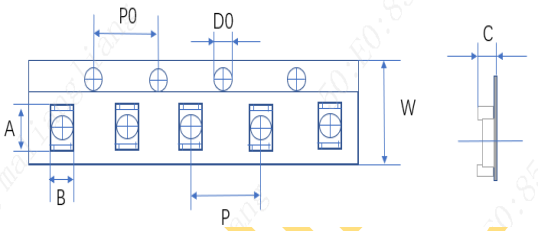
SOT563

REEL DIMENSIONS



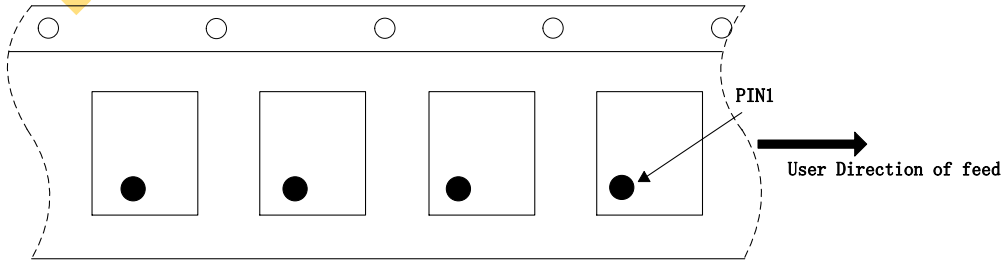
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.63	1.83	2.03
B	1.60	1.80	2.00
P0	3.80	4.00	4.20
P	3.80	4.00	4.20
D0	1.30	1.50	1.70
W	7.70	8.00	8.30
C	0.55	0.75	0.95

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

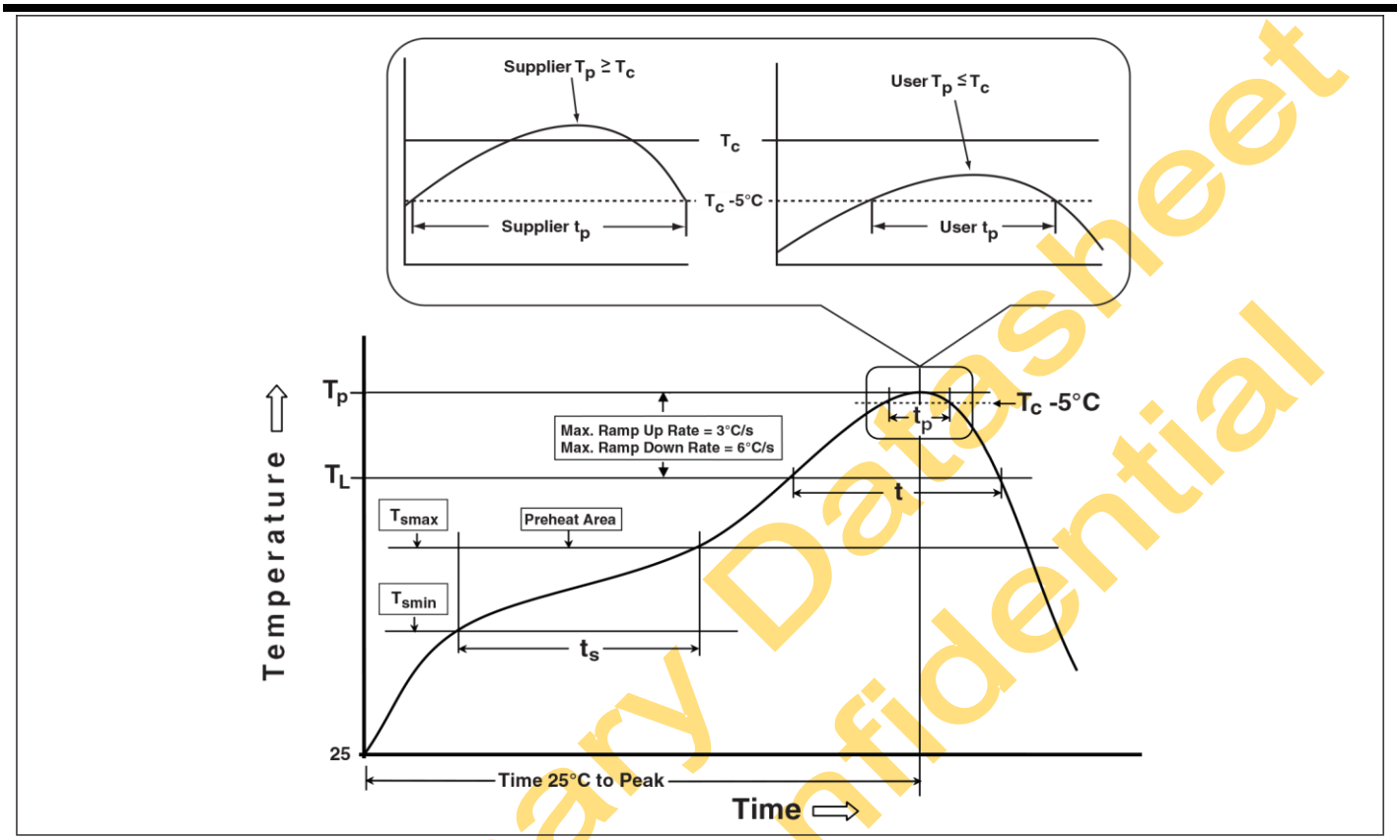


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;

Revision History

Revision	Date	Change Description
Rev0.1	5/24/2025	First version
Rev0.2	7/24/2025	Add SOT563 package information
Rev0.3	3/24/2026	Change SOT563 package top marking from 'A1YWX 'to 'H2YWX'