Features

- 2.5V to 4.8V Input Supply
- Generate two output voltage, positive voltage (VSP) and -1 ratio of negative voltage (VSN)
- Only 5 external capacitors
- TDFN-12 (2.4mmx1.5mm) Exposed Pad Package

Applications

- TFT LCD for smart phone and tablet LCD panel's driver IC

General Description

The LP3100HQVF is an integrated power supply solution optimized for small to medium size thin-film transistor (TFT) liquid crystal displays (LCD's). Primarily intended for smart phone and tablet LCD panel's driver IC.

The positive charge pump has an internal switch and typically can support output current up to 100mA at V_{CI}=3.3V.

Negative charge pump has an internal switch to generate -1 ratio of VSN and typically can support output current up to 100mA at V_{CI}=3.3V.

The pump clock can be synchronized with external signal from driver IC or can be generated by internal circuit fixed to 600kHz.

The LP3100HQVF is available in a thin 12-pin 2.4x1.5 mm TDFN green package.

Order Information

LP3100H □□ □

F: Pb-Free
Package Type
QV: TDFN-12L

Figure 1 Order Information

Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP3100HQVF	LP3100 HYWX	MSL3	TDFN-12L	3K/REEL
Marking indication: Y: Production year W: Production week X: Production batch				

Table 1. Device Information

Typical Application

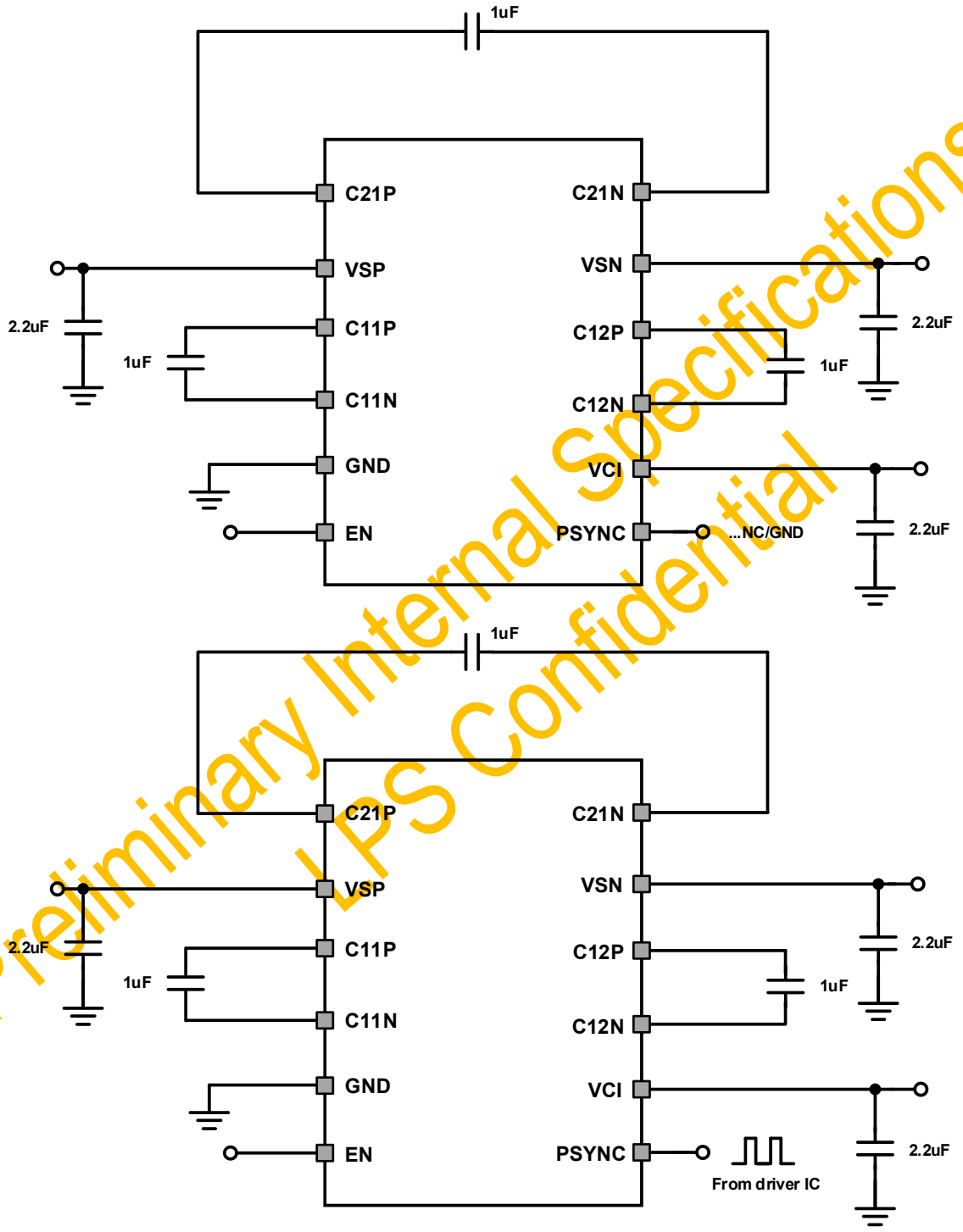
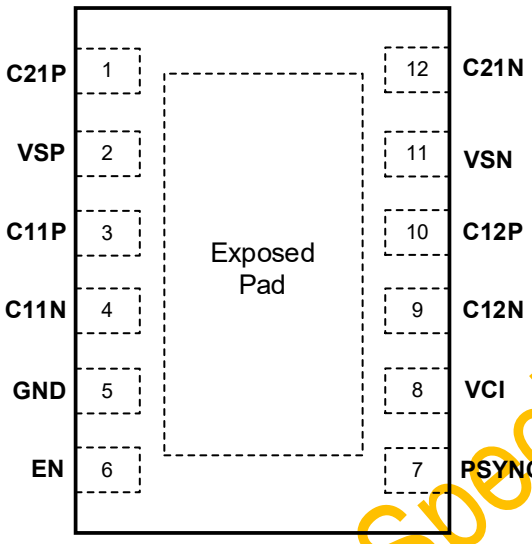


Figure 2 Typical Application Circuit

Pin Diagram



(Top View)

Figure 3 LP3100HQVF TDFN-12L

Pin Description

Pin No.	Pin Name	I/O	Pin Function
1	C21P	I	Capacitor connection pin for the VSN.
2	VSP	O	Positive voltage output pin (VSP).
3	C11P	I	Capacitor connection pin for the VSP.
4	C11N	I	Capacitor connection pin for the VSP.
5	GND	P	Ground pin.
6	EN	I	Enable pin.
7	PSYNC	I	PSYNC pin connect with GND or use external clock from driver IC.
8	VCI	P	Power supply input pin.
9	C12N	I	Capacitor connection pin for the VSP.
10	C12P	I	Capacitor connection pin for the VSP.
11	VSN	O	Negative voltage output pin (VSN).
12	C21N	I	Capacitor connection pin for the VSN.

Table 2. Pin Description

Absolute Maximum Ratings (Note)

VCI ---------- -0.3V to 6V
Control signal voltage ---------- -0.3V to 6V
VSP ---------- 0V to 6V
VSN ---------- 0V to -6V
Operating Junction Temperature Range (TJ) ---------- -40°C to +125°C
Operating Temperature Range (TOP) ---------- -40°C to +85°C
Storage Temperature Range ---------- -55°C to +150°C
Lead soldering Temperature Range (10 seconds) ---------- -40°C to +125°C

Note1：Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

ESD Ratings

HBM (Human Body Model) ---------- +/-2kV
MM (Machine Model) ---------- +/-200V
CDM (Charge Discharge Model) ---------- +/-500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 68℃/W

Electrical Characteristics

(VIN=3V, TA=-40°C to 85°C, unless otherwise specified. Typical values are tested at 25°C ambient temperature)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage	V_{CI}		2.5		4.8	V
VCI Under Voltage Lockout (UVLO)	V_{UVLO}	VCI Rising	2	2.2	2.4	V
		Hysteresis		200		mV
Standby Current	$I_{STANDBY}$				2	uA
Output Voltage VSP						
Output Voltage Range	V_{SP}	VCI=3V. Io=0mA	5.6		6	V
Output Current Capability		VCI=2.8V		35		mA
		VCI=3V		60		mA
		VCI=3.3V		100		mA
Output Voltage VSN						
Output Voltage Range	V_{SN}	VCI=3V. Io=0mA	-5.6		-6	V
Output Current Capability		VCI=2.8V		35		mA
		VCI=3V		60		mA
		VCI=3.3V		100		mA
LOGIC EN/PSYNC						
Threshold Voltage	VIH		1.5			V
	VIL				0.5	V
PSYNC Frequency			50		1200	kHz
Internal Pump Clock Frequency				600		kHz
Enable Pull down Resistor				300		kΩ

Functional Block Diagram

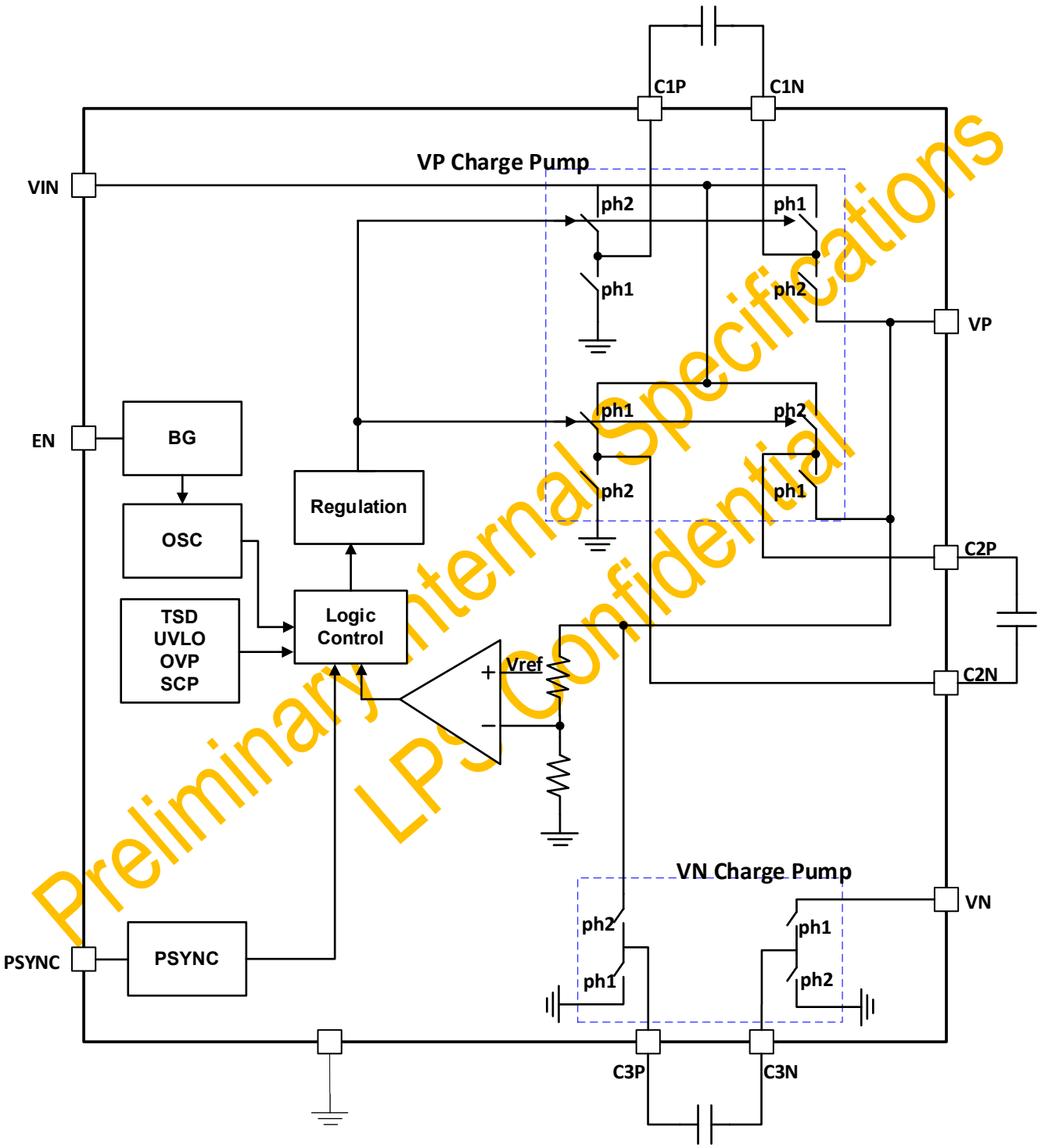


Figure 4 Block Diagram

Application Information

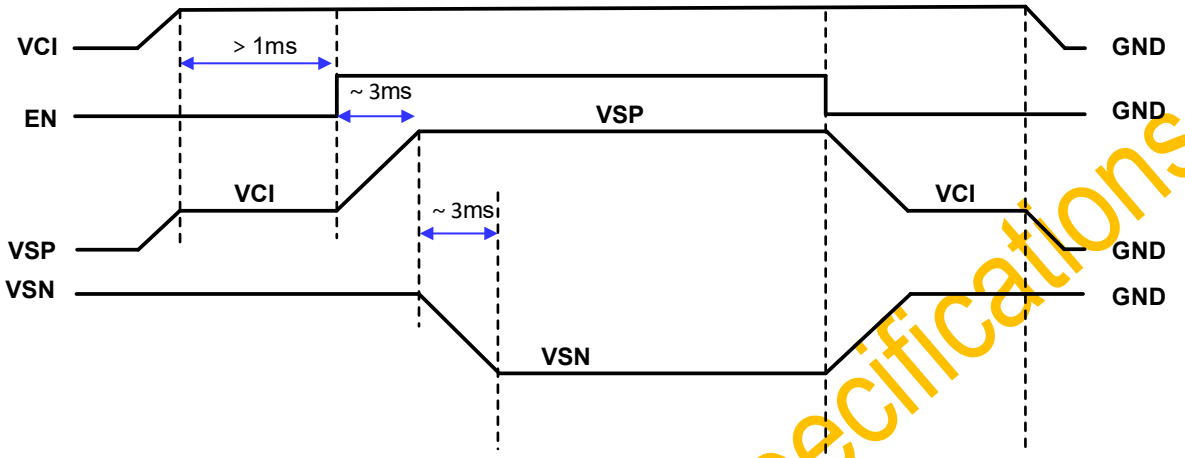


Figure 5 Power sequence of pump clock used internal circuit

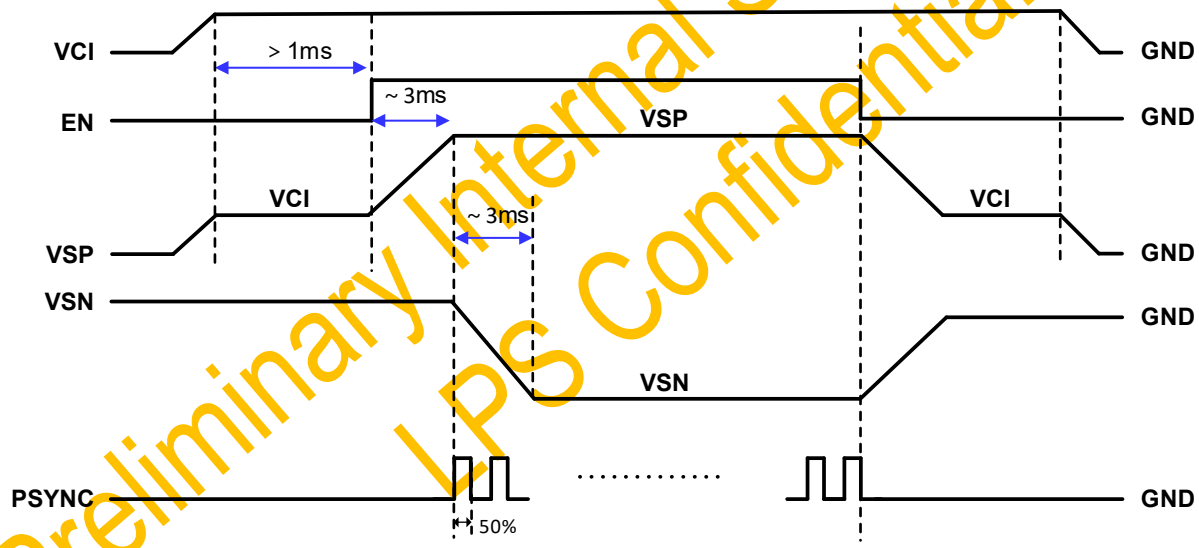


Figure 6 Power sequence of pump clock used synchronized signal

PCB Layout Guideline

1. Pin1 & P12 is Negative Charge pump, C4 Provide energy for VSN, Place the C4 components to Pin1 & P12 as close as possible.
2. Pin3 & Pin4 is Positive Charge pump, C6 Provide energy for VSP, Place the C6 components to Pin3 & P4 as close as possible.
3. Pin9 & Pin10 is Positive Charge pump, C2 Provide energy for VSP, Place the C2 components to Pin1 & P12 as close as possible.
4. Pin 8 requires a stable and clean Input voltage. Place the capacitor C1 stable input voltage. Place the C1 components to pin8 as close as possible.

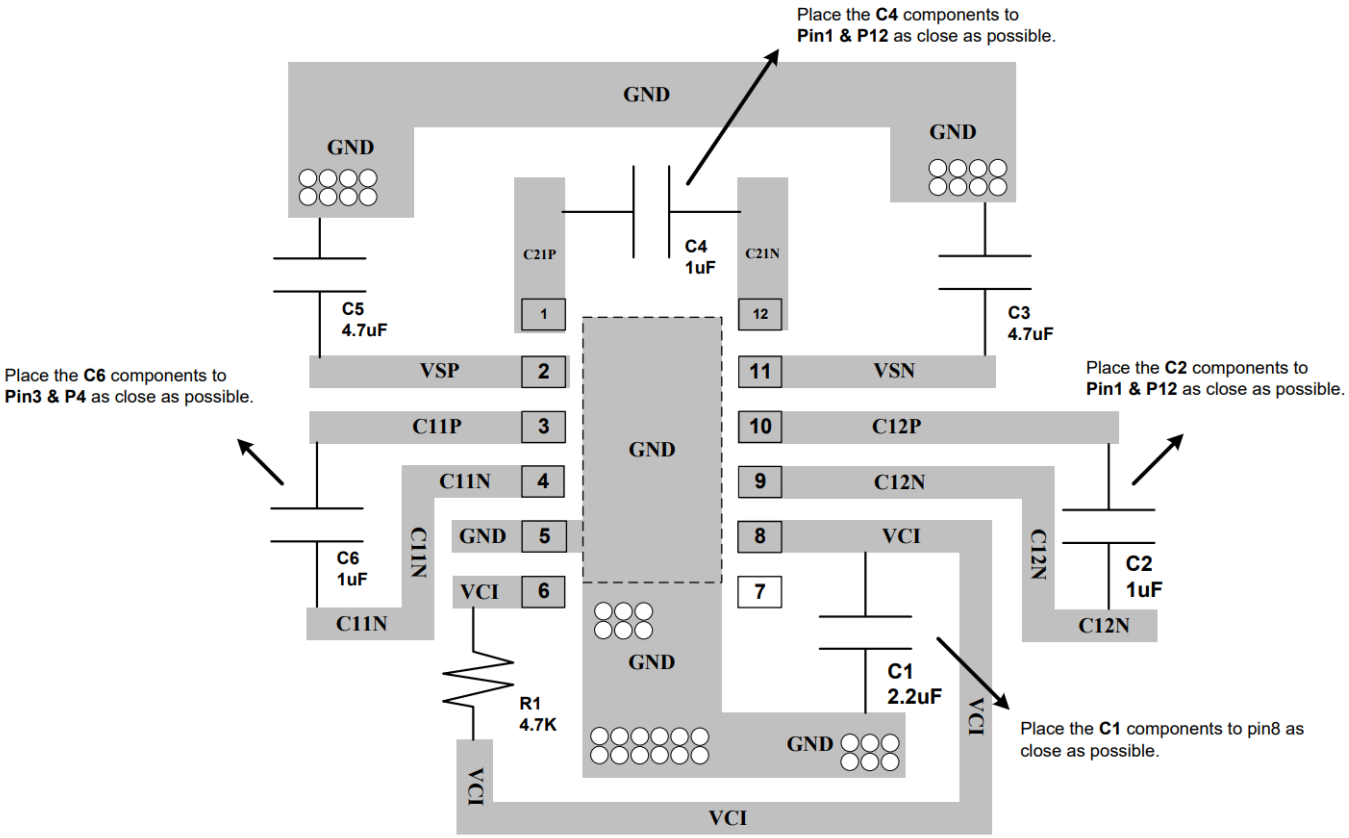
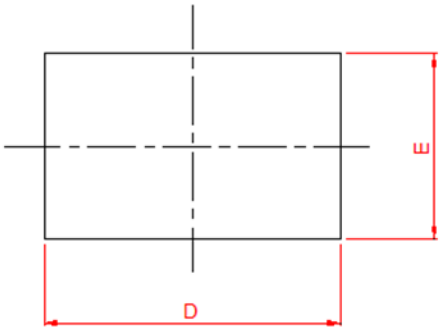


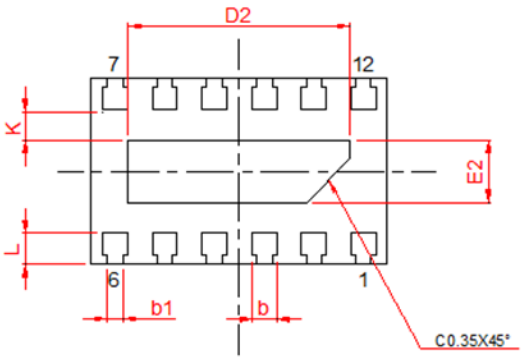
Figure 6 Layout Guideline

Package Information

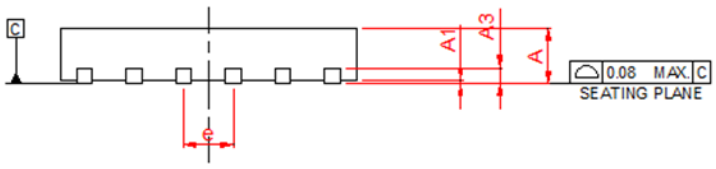
TDFN-12 (2.4mmx1.5mm) Pad Package



TOP VIEW



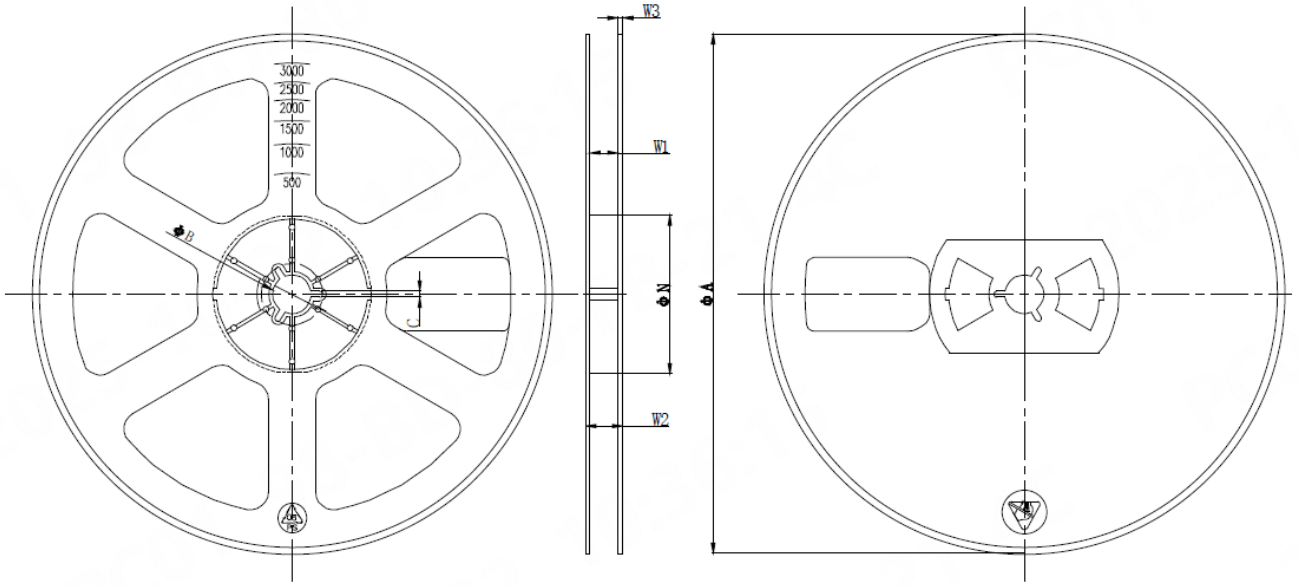
BOTTOM VIEW



SIDE VIEW

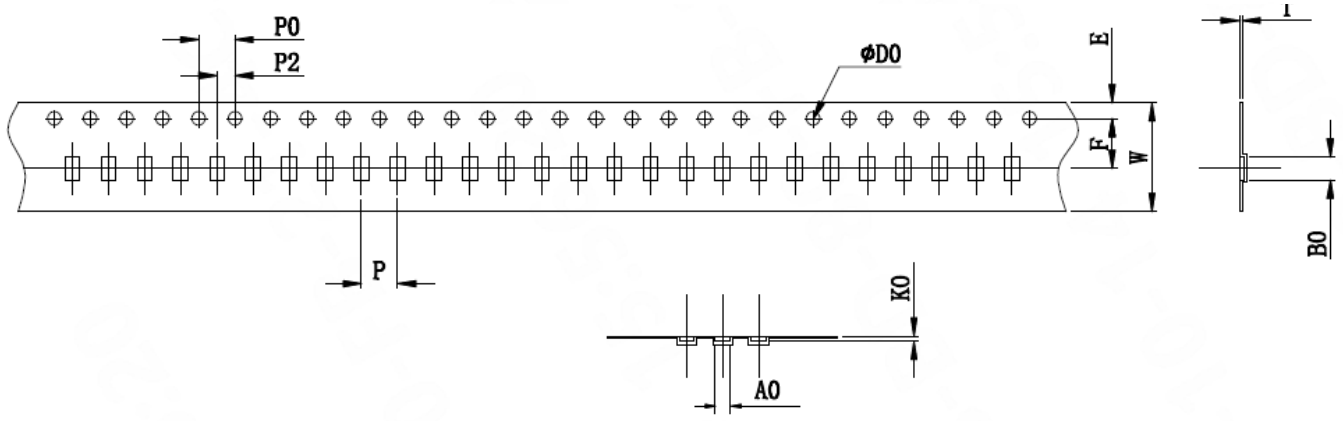
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
★ A	0.50	0.55	0.60
★ A1	0.00	0.02	0.05
★ A3		0.152 REF	
★ b	0.15	0.20	0.25
★ b1	0.075	0.125	0.175
★ D		2.40 BSC	
★ E		1.50 BSC	
★ e		0.40 BSC	
★ L	0.20	0.25	0.30
★ K	0.20	-	-
★ D2	1.75	1.80	1.85
★ E2	0.45	0.50	0.55

Carrier information



ΦA	ΦN	ΦB	C	W1	W2	W3
178±2	54±2	13.2±0.3/0.2	2.2±0.3	9.5±1	13MAX	1.4±0.4

注：
黑色卷盘重量标准：≥40g
其他卷盘重量标准：≥42g



W	E	F	D0	P	P0	P2	A0	B0	K0	T
8.00±0.10	1.75±0.10	3.50±0.10	1.50+0.10 1.50-0.00	4.00±0.10	4.00±0.10	2.00±0.05	1.65±0.05	2.55±0.05	0.60±0.05	0.30±0.05