High Efficiency 3A Boost DC/DC Convertor

General Description

The LP6216 is a current mode boost DC-DC converter. Its PWM circuitry with built-in 3A current power MOSFET makes this converter highly power efficiently. The LP6216 implements a constant frequency 1MHz PWM control scheme. The high frequency PWM operation also saves board space by reducing external component sizes. The LP6216 features automatic shifting to pulse frequency modulation mode at light loads.Highly integration and internal compensation network minimizes as 6 external component counts. Optimized operation frequency can meet the requirement of small LC filters value and low operation current with high efficiency.

The LP6216 includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The LP6216 is available in a small 6-pin SOT23-6 package.

Order Information

LP6216H □□ □

- F: Pb-Free
- Package Type
  B6: SOT23-6

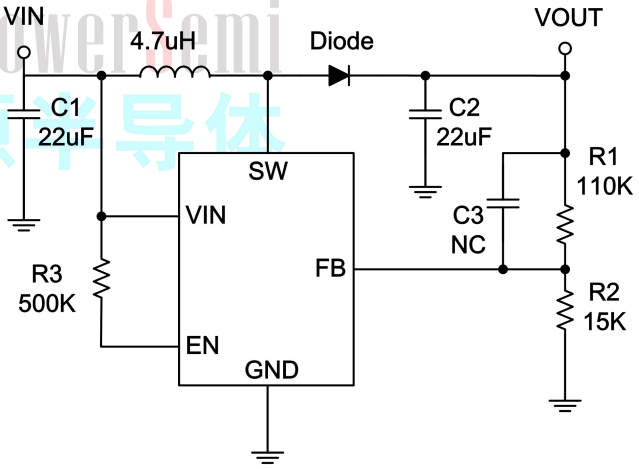
Applications

- ✧ Battery products
- ✧ Host Products
- ✧ Panel

Features

- ◆ Up to 94% efficiency
- ◆ Shut-down current:1uA
- ◆ Input and Output voltage Up to 24V
- ◆ Internal Compensation, Soft-start
- ◆ 1MHz fixed frequency switching
- ◆ High switch on current:3A
- ◆ Available in SOT23-6 Package
- ◆ RoHS Compliant and 100% Lead (Pb)-Free

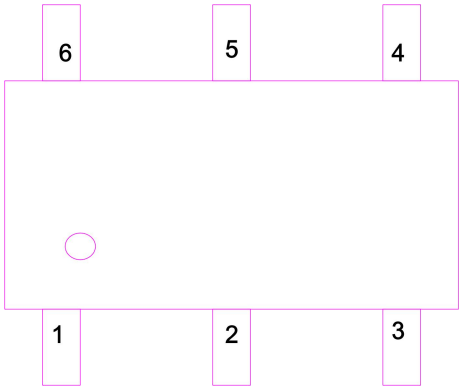
Typical Application Circuit



Marking Information

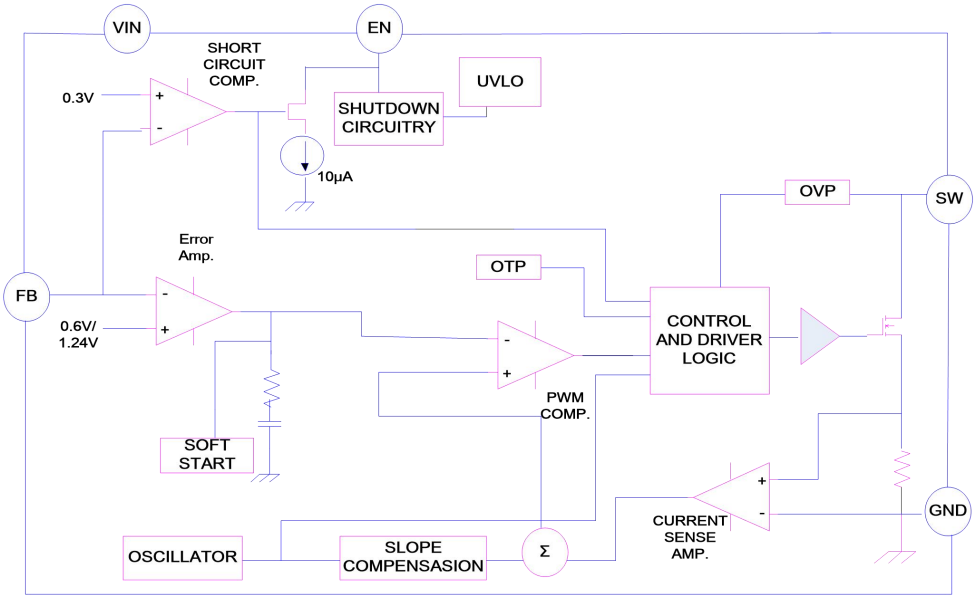
Device	Marking	Package	Shipping
LP6216B6F	LPS 5EYWX	SOT23-6	3K/REEL
Marking indication: Y:Production year W:Production period X:Production batch			

Functional Pin Description

Package Type	Pin Configurations
SOT23-6	

Pin	Name	Description
1	SW	switching pin.
2	GND	Ground.
3	FB	Regulation Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage.
4	EN	Regulator ON/OFF Control Input. A logic high input(V_{EN}>1.4V) turns on the regulator. A logic low input(V_{EN}<0.4V) puts the LP6216 into low current shutdown mode.
5	VIN	Power Supply pin.
6	NC	No connecter.

Function Block Diagram



Absolute Maximum Ratings Note 1

- ✧ VIN to GND ---------- -0.3V to 26V
- ✧ SW to GND ---------- -0.3V to 30V
- ✧ EN to GND ---------- -0.3V to 26V
- ✧ Other Pin Voltage to GND ---------- -0.3V to 6V
- ✧ Maximum Junction Temperature ---------- 150°C
- ✧ Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (P_D,T_A=25°C) ---------- 0.45W
- ✧ Thermal Resistance (J_A) ---------- 250°C/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

Recommended Operating Conditions

- ✧ Ambient Temperature Range ---------- -20°C to 85°C

Electrical Characteristics

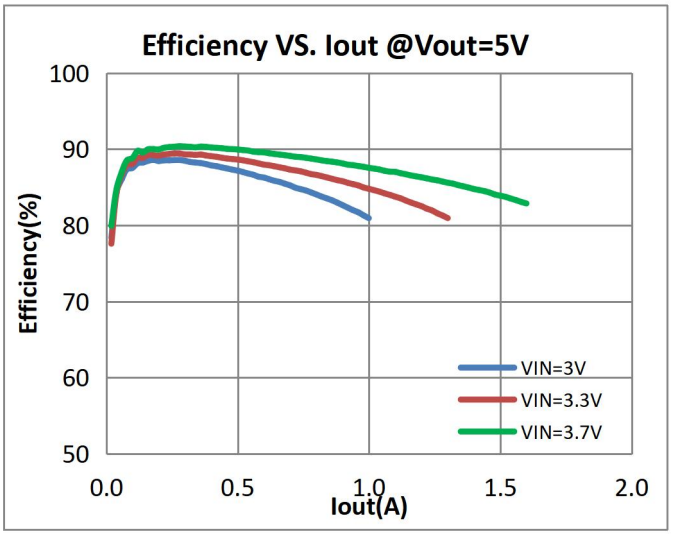
(V_{IN}=3.3V, V_{OUT}=5V, C_{IN}=22uF, C_{OUT}=22uF, L=4.7uH, R_1=110K, R_2=15K)

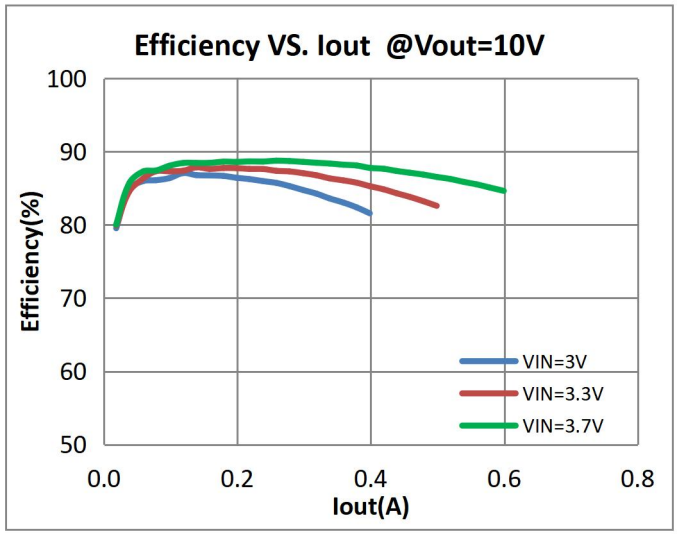
Parameter		Condition	Min	Typ	Max	Units
Supply Voltage	V_{IN}		2.5		24	V
Output Voltage Range	V_{OUT}		2.5		24	V
Supply Current(Shutdown)	I_{SD}	V_{EN}=0V		1	3	μA
Supply Current	I_Q	V_{FB}=1.3V		0.35	0.6	mA
Feedback Voltage	V_{FB}	LP6216B6F	0.588	0.6	0.612	V
		LP6216AB6F	1.215	1.24	1.265	V
Feedback Input Current(2)	I_{FB}	V_{FB}=1.2V		50		nA
Switching Frequency	f_{OSC}			1		MHz
Maximum Duty Cycle			85	92	98	%
EN Input Low Voltage	V_{EN-L}				0.4	V
EN Input High Voltage	V_{EN-H}		1.4			V
EN input current	I_{EN}	VEN=5		1		uA
Switch MOSFET Current Limit(2)	I_{SW}			3		A
High-side On Resistance(2)	$R_{DS(ON)}$	V_{OUT}=5V		150		mΩ

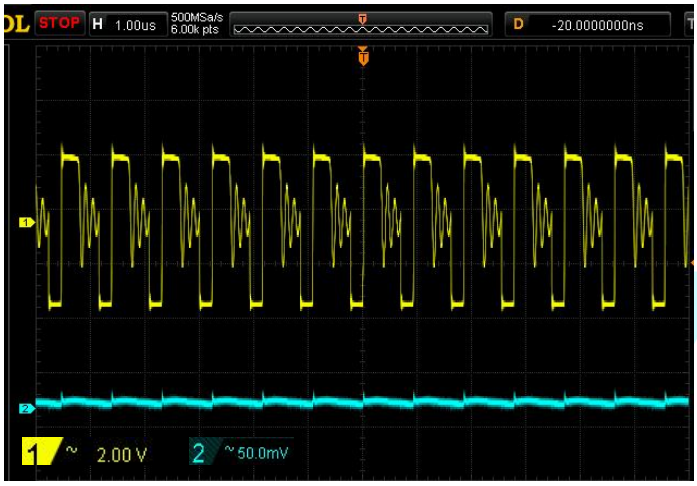
Note 2. The parameter is guaranteed by design and characterization.

Typical Operating Characteristics

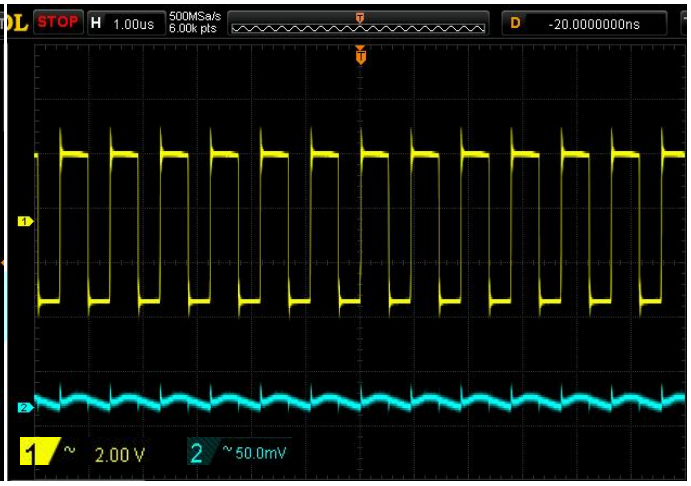
(C_{IN}=22uF,C_{OUT}=22uF,L=4.7uH,T_A=25℃,unless otherwise noted)





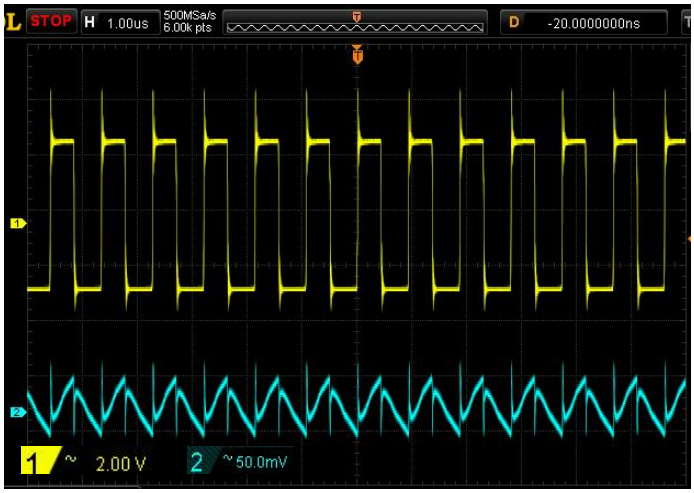


V_{IN}=3V,V_{OUT}=5V,I_{OUT}=50mA,CH_1=V_{SW},CH_2=△V_{OUT}



V_{IN}=3V,V_{OUT}=5V, I_{OUT}=200mA,CH_1= V_{SW},CH_2=△V_{OUT}

V_{IN}=3V,V_{OUT}=5V,I_{OUT}=500mA,CH_1= V_{SW},CH_2=△V_{OUT}



V_{IN}=3V,V_{OUT}=5V, I_{OUT}=1A,CH_1= V_{SW},CH_2=△V_{OUT}

Operation Information

The LP6216 uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals The output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 0.6V bandgap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. TheLP6216 has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.6V feedback voltage. Use a 100K resistor for R_2 of the voltage divider. Determine the high-side resistor R_1 by the equation:

$$V_{OUT} = (R_1 / R_2 + 1) \times V_{FB}$$

Current Limitation

The internal power-MOS switch current is monitored cycle-by-cycle and is limited to the value not exceed 3A(Typ.). When the switch current reaches the limited value, the internal power-MOS is turned off immediately until the next cycle. Keep traces at this pin as short as possible. Do not put capacitance at this pin.

Inductor Selection

For a better efficiency in high switching frequency converter, the inductor selection has to use a proper core material such as ferrite core to reduce the core loss and choose low ESR wire to reduce copper loss. The most important point is to prevent the core saturated when handling the maximum peak current. Using a shielded inductor can minimize radiated noise in sensitive applications. The maximum peak inductor current is the maximum input current plus the half of inductor ripple current. The calculated peak current has to be smaller than the current limitation in the electrical characteristics. A typical setting of the inductor ripple current is 20% to 40% of the maximum input current. If the selection is 40%, the maximum peak inductor current is

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} I_{RIPPLE} = 1.2 \times I_{IN(MAX)}$$
$$= 1.2 \times \left[\frac{I_{OUT(MAX)} \times V_{OUT}}{\eta \times V_{IN(MIN)}} \right]$$

The minimum inductance value is derived from the following equation:

$$L = \frac{\eta \times V_{IN(MIN)}^2 \times [V_{OUT} - V_{IN(MIN)}]}{0.4 \times I_{OUT(MAX)} \times V_{OUT}^2 \times f_{OSC}}$$

Depending on the application, the recommended inductor value is between 2.2μH to 10μH.

Diode Selection

To achieve high efficiency, Schottky diode is good choice for low forward drop voltage and fast switching time. The output diode rating should be able to handle the maximum output voltage, average power dissipation and the pulsating diode peak current.

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 22μF input capacitor is sufficient for most applications. For a lower output power requirement application, this value can be decreased.

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitors are recommended. The tantalum capacitors can be used as well, but the ESR is bigger than ceramic capacitor. The output voltage ripple consists of two components: one is the pulsating output ripple current flows through the ESR, and the other is the capacitive ripple caused by charging and discharging.

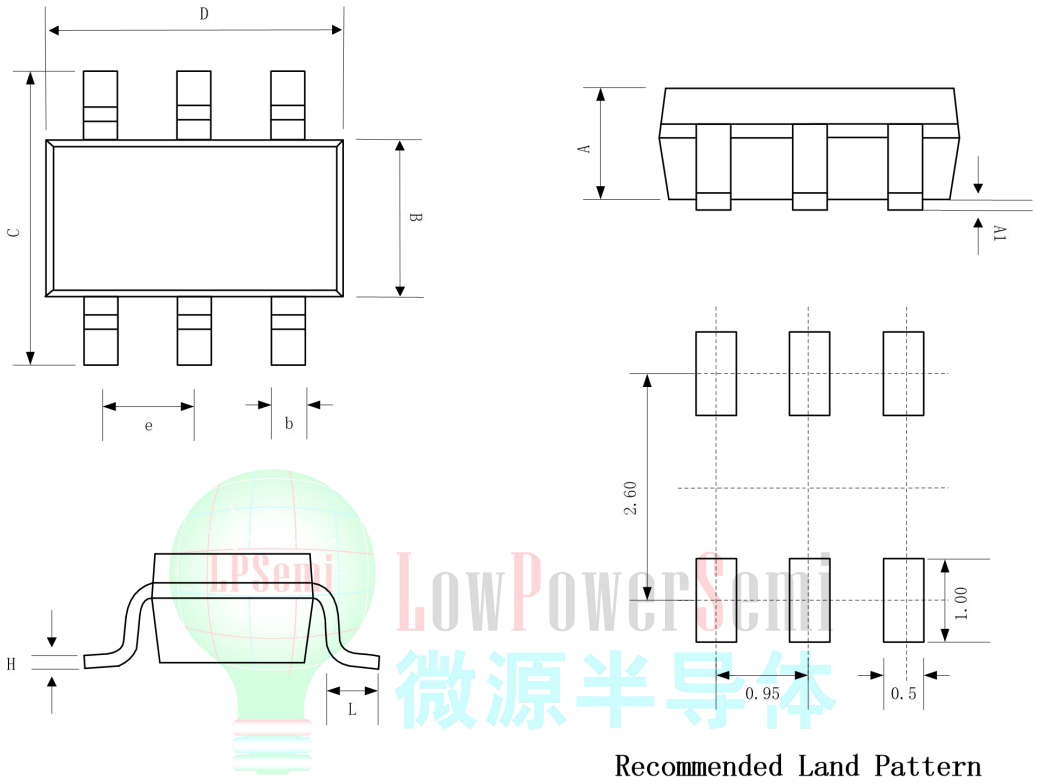
$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C}$$
$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \times f_{OSC}} \right)$$

Layout Guideline

For high frequency switching power supplies, the PCB layout is important step in system application design. In order to let IC achieve good regulation, high efficiency and stability, it is strongly recommended the power components should be placed as close as possible. The set races should be wide and short. The feedback pin and then works of feedback and compensation should keep away from the power loops, and be shielded with a ground trace or plane to prevent noise coupling.Input and Output capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.

Packaging Information

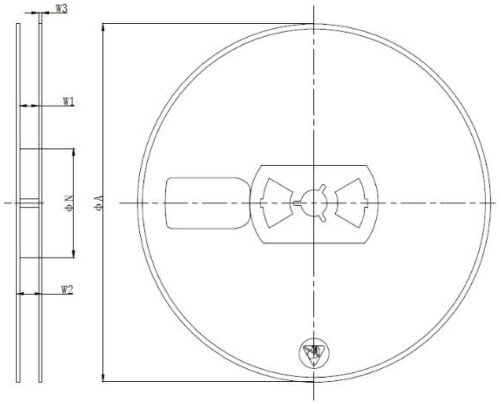
SOT23-6



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

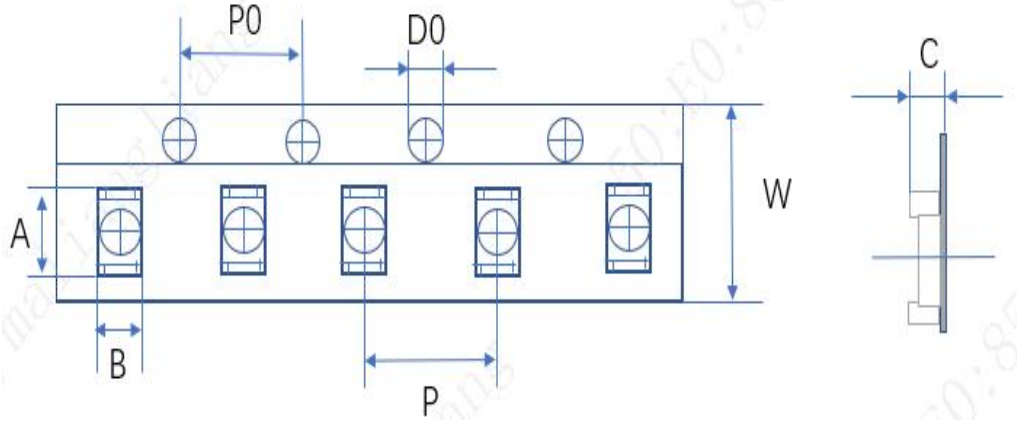
Tape and Reel Information

REEL DIMENSIONS（Unit:mm）



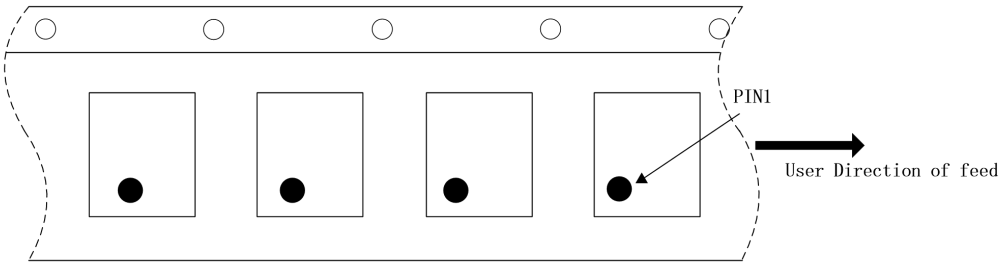
ΦA	W2
180±4	12±0.6

TAPE DIMENSIONS（Unit:mm）



口袋宽度A		口袋长度B		编带孔中心间距P0		IC中心间距P		孔径D0		编带宽度W		编带厚度C	
尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差	尺寸(mm)	公差
3.2	±0.2	3.26	±0.2	4	±0.1	4	±0.1	1.5	±0.15	8	±0.3	1.4	±0.2

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed theClassification temp in Table 1. For suppliers T_P must equal or exceedthe Classification temp in Table 1.	For users T_P must not exceed theClassification temp in Table 2. For suppliers T_P must equal or exceedthe Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

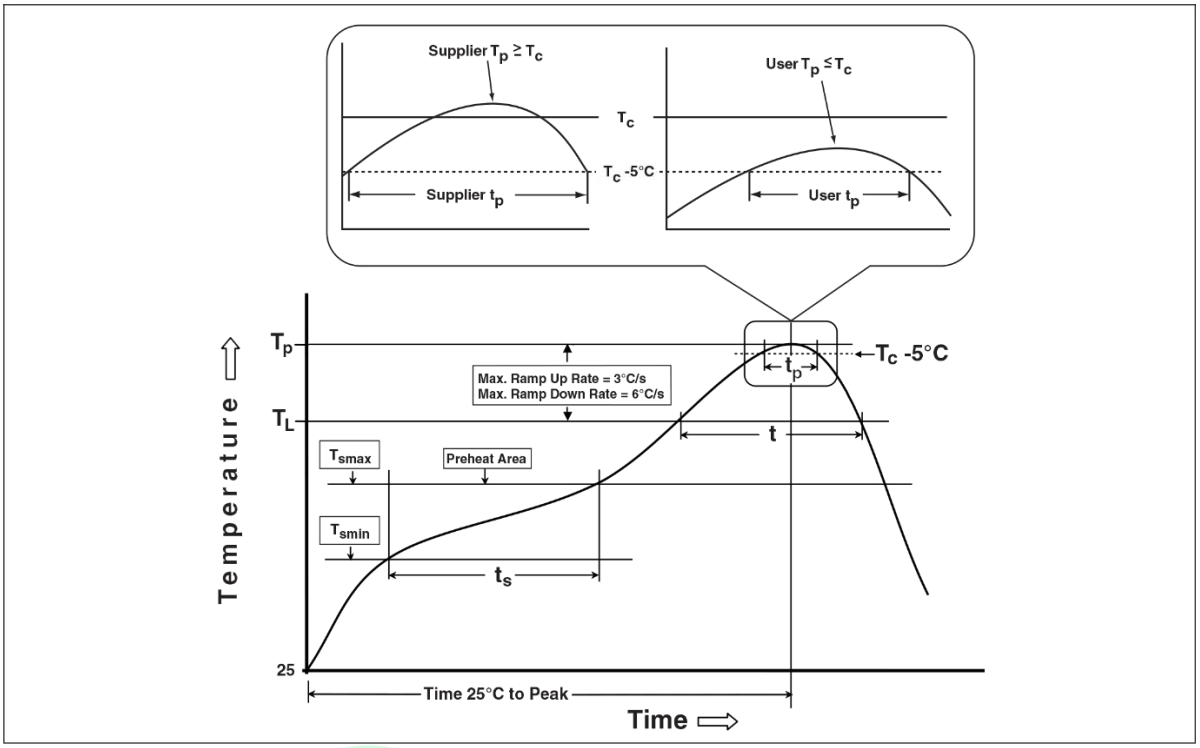


Figure1Classification Profile (Not to scale)

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;