



### Features

- Input voltage range: 2.7V~ 5.5V
- Output voltage range: 0.6V ~VIN
- High efficiency operation
  - Integrated a 120mΩ LS-MOSFET and a 200mΩ HS-MOSFET
  - Integrated a 130mΩ LS-MOSFET and a 215mΩ HS-MOSFET
  - More than 90% efficiency at 1A load from 5V to 3.3V conversion
- Automatic PFM mode at light load
- $\pm 1.5\%$   $V_{REF}$  accuracy at 25°C
- Low quiescent current: 40μA
- Shutdown current <1μA
- Pseudo fixed 1.5MHz switching frequency
- Adaptive COT control scheme with fast load transient response
- PG output
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- 0.4ms typical soft-start time
- Auto-discharge
- SOT23-5, SOT23-6 and SOT563 package
- RoHS Compliant and 100% Lead (Pb) Free

### Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV
- Set-top Box
- WIFI
- Battery powered devices

### General Description

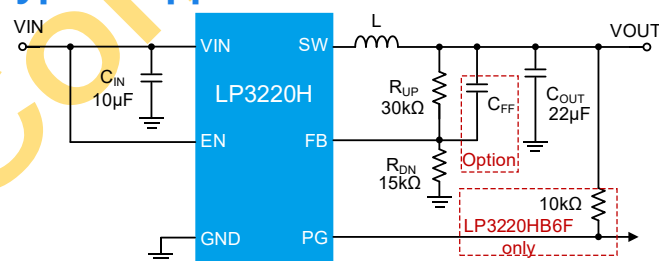
The LP3220H is a synchronous buck converter supporting up to 1.2A output current. The LP3220H employs an adaptive constant-off-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP3220H supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP3220H integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP3220H also integrates multiple protection functions, i.e., over current protection (OCP), over temperature protection (OTP), under voltage lockout (UVLO) and short circuit protection (SCP).

The LP3220H is available in a small SOT23-5/-6 or SOT563 package.

### Typical Application Circuit



### Order Information

LP3220H

F: Pb Free  
 Package Type  
 B5: SOT23-5  
 B6: SOT23-6  
 G6: SOT563



## Device Information

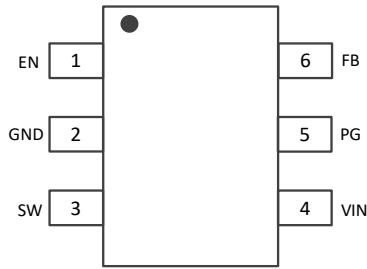
Part Number	Top Marking	Operation Mode	Moisture Sensitivity Level	Package	Shipping
LP3220HB5F	LPS A1YWX	PFM/PWM	LEVEL 3	SOT23-5	3K/REEL
LP3220HG6F	LPS A1YWX	PFM/PWM	LEVEL 3	SOT563	3K/REEL

Marking indication:  
Y: Year code. W: Week code. X: Batch numbers.

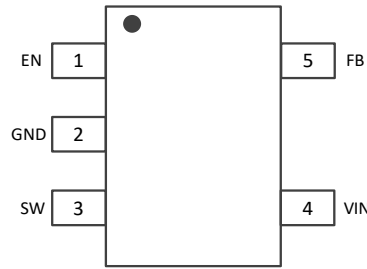
Preliminary Datasheet  
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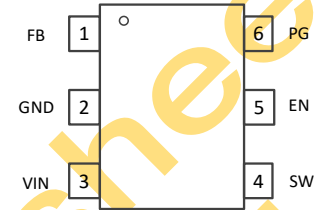
## Pin Diagram



SOT23-6 (top view)



SOT23-5 (top view)



SOT563 (top view)

## Pin Description

Pin			Name	Description
SOT23-6	SOT23-5	SOT563		
1	1	5	EN	Enable pin. Active high. Logic low disables the device. Do not leave the pin floating.
2	2	2	GND	Ground pin.
3	3	4	SW	Switching node of the converter. Connect the inductor to this pin.
4	4	3	VIN	Power supply voltage pin. Must be closely decoupled to GND with a capacitor. Place the capacitor as close as to the pin as possible.
5	-	6	PG	Power Good. Open drain output, if not used, leave the pin floating.
6	5	1	FB	Feedback pin. Use a resistor divider to set the output voltage.



## Absolute Maximum Ratings (Note 1)

VIN, SW, EN Pin to GND	-----	-0.3~6.5V
SW Pin to GND (5ns transient)	-----	-2~8V
Maximum Junction Temperature (T <sub>J</sub> )	-----	150°C
Maximum Soldering Temperature (at leads, 10 sec)	-----	260°C
Storage Temperature Range	-----	-65°C to 125°C

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Susceptibility

HBM (Human Body Model)	-----	2kV
CDM (Charged Device Model)	-----	500V

## Thermal Information (Note 2)

θ <sub>JA</sub> (Junction-to-Ambient Thermal Resistance, SOT23-5/-6)	-----	160°C/W
θ <sub>JA</sub> (Junction-to-Ambient Thermal Resistance, SOT563)	-----	140°C/W

**Note 2.** Measured using 2S2P JEDEC standard PCB.

## Recommended Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>IN</sub>	Input voltage	2.7		5.5	V
V <sub>OUT</sub>	Output voltage	0.6		V <sub>IN</sub>	V
L	Inductor	0.7		3.3	μH
T <sub>A</sub>	Ambient temperature range	-40		85	°C
C <sub>IN</sub>	Input decoupling capacitor, effective capacitance	4.7		100	μF
C <sub>OUT</sub>	Output capacitor, effective capacitance	10		100	μF



## Electrical Characteristics

(The specifications are measured under conditions  $V_{IN} = 5V$ ,  $L=2.2\mu H$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 22\mu F$ ,  $T_J = 25^\circ C$ , unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SECTION</b>						
$V_{ULVO\_R}$	Input under voltage lockout threshold	$V_{IN}$ rising threshold	2.3	2.4	2.5	V
$V_{ULVO\_H}$	UVLO hysteresis	$V_{IN}$ falling threshold		0.1		V
$t_{UVLO}$	UVLO deglitch time			32		$\mu s$
$I_{Q\_VIN}$	Input quiescent current	No switching, $EN=3V$ , $FB=1.0V$		40	80	$\mu A$
$I_{SD\_VIN}$	Input shutdown current	No switching, $EN=0V$		0.1	1	$\mu A$
<b>BUCK CONVERTER</b>						
$I_{LIM\_PEAK}$	High-side peak current limit			2.0		A
$I_{LIM\_VALLEY}$	Low-side valley current limit			1.2		A
$I_{ZCD}$	Zero current detection	PFM	0.05	0.1	0.15	A
$V_{REF}$	Reference voltage	$T_J=25^\circ C$	0.591	0.6	0.609	V
$R_{DSON\_HS}$	High-side FET on resistance	SOT23-5/-6 package		200		$m\Omega$
		SOT563 package		215		$m\Omega$
$R_{DSON\_LS}$	Low-side FET on resistance	SOT23-5/-6 package		120		$m\Omega$
		SOT563 package		130		$m\Omega$
$F_{sw}$	Switching frequency			1500		kHz
$t_{EN\_DLY}$	EN delay time	EN turn high to first switching cycle		100	200	$\mu s$
$t_{ss}$	Soft start time	From 1 <sup>st</sup> switching cycle to 95% $V_{ref}$		400		$\mu s$
$t_{SCP}$	SCP deglitch time <sup>[1]</sup>	SCP deglitch time		32		cycle
<b>Thermal Shutdown</b>						
$T_{SD\_R}$	Shutdown threshold temperature	Rising threshold		155		$^\circ C$
$T_{SD\_F}$	Recovery threshold temperature	Falling threshold		135		$^\circ C$



EN and PG						
V <sub>EN_H</sub>	EN high threshold	Rising threshold	1.2			V
V <sub>EN_L</sub>	EN low threshold				0.4	V
R <sub>EN_PD</sub>	EN pin pull-down resistance			1000		kΩ
R <sub>DIS</sub>	SW Discharge FET on-resistance	EN=0		1		kΩ
V <sub>FB_PG_R</sub>	FB High threshold to trigger PG output	FB rising, reference to VREF		95		%
V <sub>FB_PG_F</sub>	FB low threshold to trigger PG output	FB falling reference to VREF		90		%
t <sub>FB_PG</sub>	PG deglitch	FB rising/falling	5	10	15	μs
R <sub>ON_PG</sub>	PG FET discharge on-resistance				10	Ω

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## Typical Characteristics

( $T_J = 25^\circ\text{C}$ ,  $V_{IN}=3.3\text{V}$ ,  $R_{UP}=30\text{k}\Omega$ ,  $R_{DOWN}=15\text{k}\Omega$ ,  $V_{OUT}=1.8\text{V}$ ,  $C_{IN}=10\mu\text{F}$ ,  $C_{OUT}=22\mu\text{F}$ ,  $L=2.2\mu\text{H}$ , unless otherwise noted.)

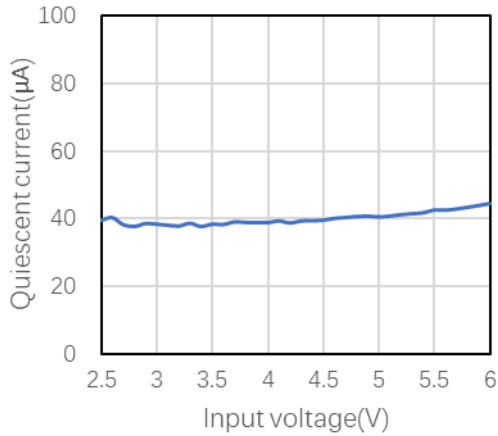


Figure 1 Quiescent vs Input Voltage

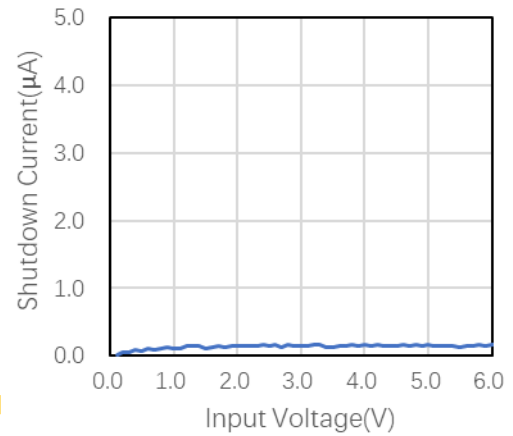


Figure 2. Shutdown Current vs Input Voltage

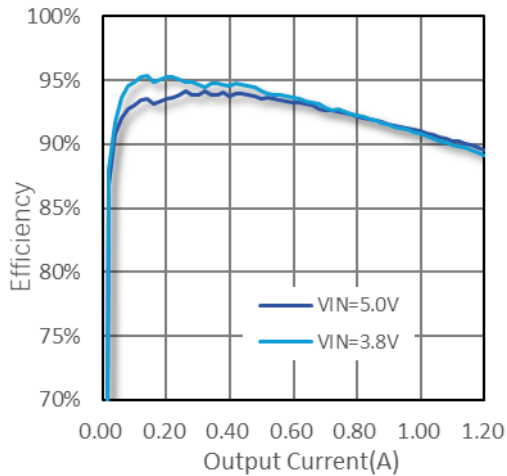


Figure 3 Efficiency vs Output Current  
 $R_{UP}=54\text{k}\Omega$ ,  $R_{DOWN}=12\text{k}\Omega$ ,  $V_{OUT}=3.3\text{V}$ , SOT23-5

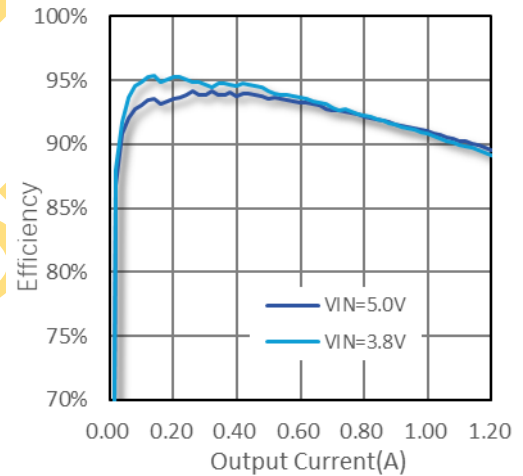


Figure 4 Efficiency vs Output Current  
 $R_{UP}=30\text{k}\Omega$ ,  $R_{DOWN}=15\text{k}\Omega$ ,  $V_{OUT}=1.8\text{V}$ , SOT23-5



Start up and Turn off Waveform:

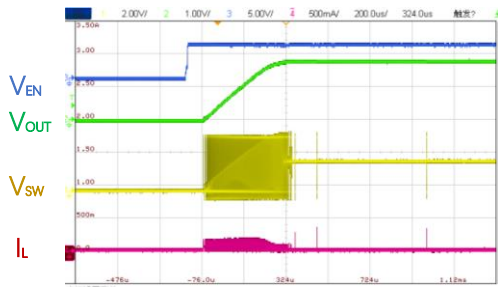


Figure 5 Start up with EN on, no load

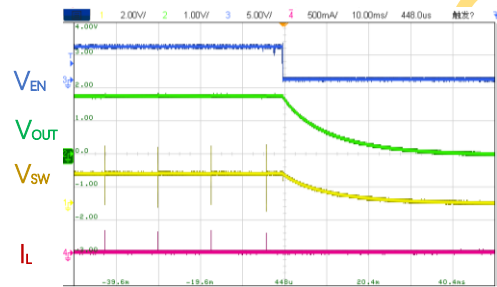


Figure 6 Turn off with EN off, no load

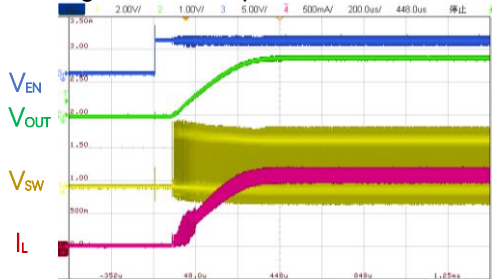


Figure 7 Start up with EN on, Rload=1.8Ω

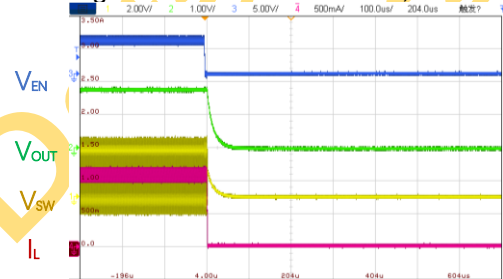


Figure 8 Turn off with EN off, Rload=1.8Ω

PWM operation Waveform:

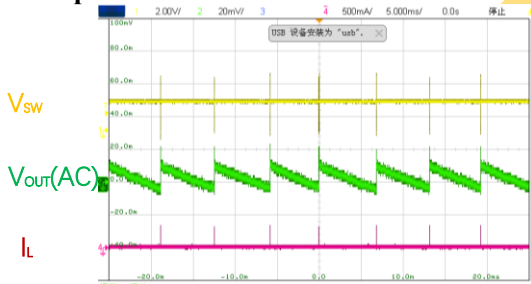


Figure 9. PWM operation with 1mA load,



Figure 10. PWM operation with 100mA load

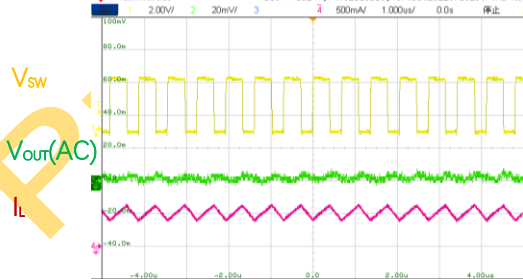


Figure 11. PWM operation with 500mA load,

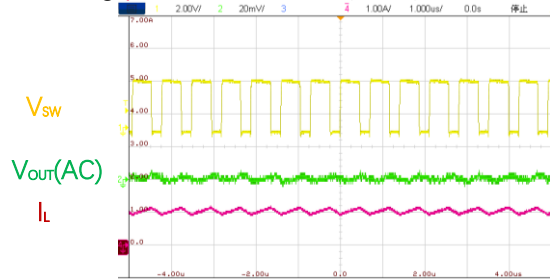


Figure 12. PWM operation with 1A load,



## Typical Characteristics(continued)

( $T_J = 25^\circ\text{C}$ ,  $V_{IN}=3.3\text{V}$ ,  $R_{UP}=30\text{k}$ ,  $R_{DOWN}=15\text{k}$ ,  $V_{OUT}=1.8\text{V}$ ,  $C_{IN}=10\mu\text{F}$ ,  $C_{OUT}=22\mu\text{F}$ ,  $L=2.2\mu\text{H}$ , unless otherwise noted.)

### Load Transient:

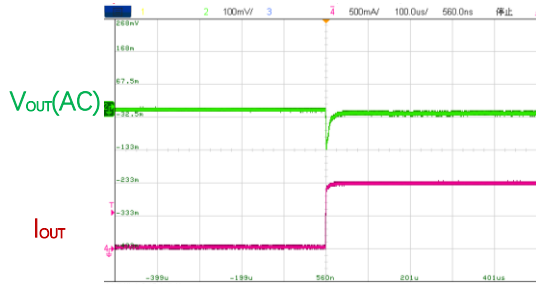


Figure 13. Load Transient no load->1A, CFF=0,

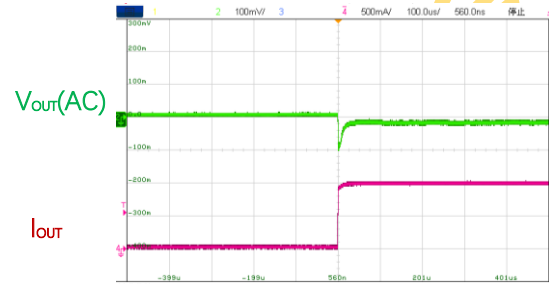


Figure 14. Load Transient no load->1A, CFF=20pF,



Figure 15. Load Transient 300mA->1A, CFF=0,

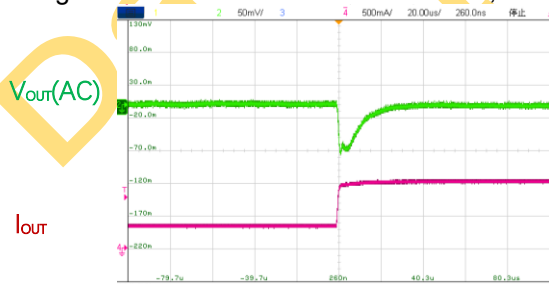
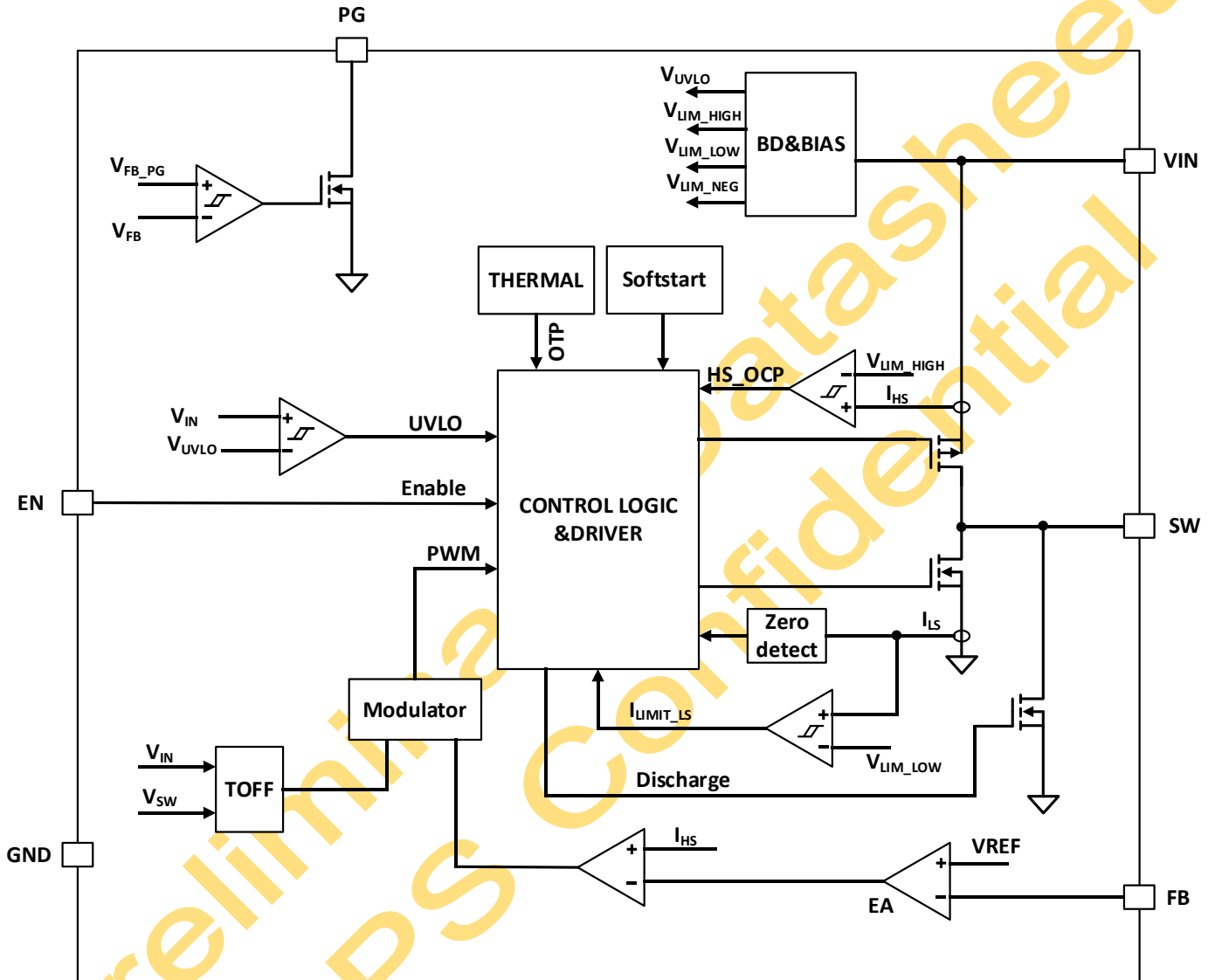


Figure 16. Load Transient 300mA->1A, CFF=20pF,



## Functional Block Diagram





## Detailed Description

### Overview

The LP3220H is a 1.2A synchronous buck converter, supporting 2.7-5.5V input voltage range. The adaptive COT(constant-off-time) control scheme enables fast transient response and minimizes the output capacitance. The LP3220H supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP3220H automatically transfers between PFM and PWM according to the output current.

### Under Voltage Lockout (UVLO)

When the input voltage  $V_{IN}$  is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP3220H can be enabled by the EN pin.

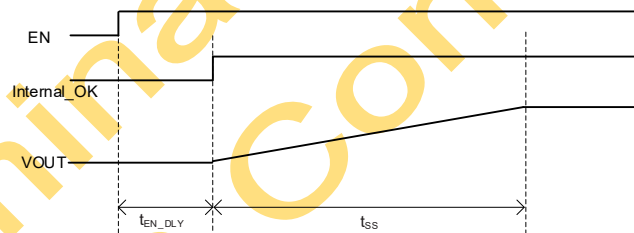
### EN Control

The EN pin can be used to control the system power-up sequence. When the  $V_{IN}$  is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold, the LP3220H enables all the internal circuits, delays for 100us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1000k $\Omega$  pull-down resistor to ground.

### Soft-start

The LP3220H integrates soft-start function with a typical time of 0.4ms ( $t_{SS}$ ). After passing the UVLO threshold and enabled by the EN pin with the 100us delay( $t_{EN\_DLY}$ ), the internal reference voltage ramps from zero to the  $V_{REF}$  in 0.4ms and the output voltage ramps up accordingly.



Soft Start Sequence

### Constant OFF Time (COT) Control Scheme

The LP3220H integrates the peak current and COT control scheme for pseudo-fixed-frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal off-time (TOFF) generator block monitors the  $V_{IN}$  and  $V_{SW}$  voltage and turns on the high-side MOSFET to start a switching cycle, when the TOFF timer time expires.

Then, the high-side current ( $I_{HS}$ ) is monitored and the LP3220H turns off the high-side MOSFET when  $I_{HS}$  reaches the error amplifier output voltage.

### PFM Operation

The LP3220H is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

### Over Current Protection and Short Circuit Protection

The LP3220H protects an over current situation by limiting the both the inductor peak and valley current. The current of low-side MOSFET is monitored when low-side FET is turned ON and the current of high-side is monitored when the high-side FET is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side



valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit plus a half of the inductor ripple current. The high-side is turned off immediately when the peak current reaches the threshold.

The SCP is realized by monitoring the high-side or low-side current limit. Once the output load draws more current than the current limit, the output voltage drops. When the current limit continues for 32 cycles, the LP3220H shutdowns. The LP3220H restarts after a typical 80us delay. If the SCP condition still holds after soft-start, the LP3220H shutdown again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

### Power Good (LP3220HB6F/G6F only)

The LP3220HB6F/G6F integrates power good indicator. When the FB voltage is lower than 90%  $V_{REF}$ , PG is pulled to GND by internal circuit. The PG recovers when the FB rises above 95% $V_{REF}$ . A 10k $\Omega$ ~100k $\Omega$  resistor is recommended to connect between  $V_{OUT}$  and PG pin. The PG-FET on-resistance is 10 $\Omega$ .

### Active output discharge

The output capacitor is discharged by EN is low,  $V_{OUT}$  is not ready or under fault conditions. The resistance between SW and GND is 1000 $\Omega$  typically.

Output Discharge Logic Table

EN State	Thermal Shutdown	Output Discharge
EN=Low	No thermal shutdown	YES
EN=High		NO
EN=Low	Thermal shutdown	YES
EN=High		YES

### Thermal Shutdown

The LP3220H has a thermal protection function. The device will shut down when the internal temperature is higher than 155°C and will restart after the temperature drops below 135°C.



## Application Information

### Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider  $R_{UP}$  and  $R_{DOWN}$  according to the equation below:

$$V_{OUT} = \left( \frac{R_{UP}}{R_{DOWN}} + 1 \right) \times V_{REF}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V.

For better accuracy, the  $R_{DOWN}$  is recommended to be lower than 100k $\Omega$  to ensure the current flowing through  $R_{DOWN}$  is at least 100 times larger than the FB pin leakage current.

For a 1.8V-output application, a 15k $\Omega$   $R_{DOWN}$  is selected and the  $R_{UP}$  is 30k $\Omega$ .

### Inductor and Output Capacitor Setting

The inductor ripple of CCM is calculated by the equation below:

$$I_{PP} = \left( \frac{V_{OUT}}{L * F_{SW}} * \frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.

For a typical 5V input voltage and 3.3V output voltage, a low DCR value, 2.2 $\mu$ H inductor is recommended.

The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor  $C_{FF}$  can be selected to improve the transient behavior. The typical capacitance can be 20~100pF.

$V_{OUT}$	Inductor-L	$C_{OUT}$	$R_{UP}$	$R_{DOWN}$	$C_{FF}$
1.2V	2.2 $\mu$ H	22 $\mu$ F	15 k $\Omega$	15 k $\Omega$	0-100pF
1.8V	2.2 $\mu$ H	22 $\mu$ F	30 k $\Omega$	15 k $\Omega$	0-100pF
3.3V	2.2 $\mu$ H	22 $\mu$ F	54 k $\Omega$	12 k $\Omega$	0-100pF

### Input capacitor

A typical higher than 10 $\mu$ F ceramic capacitor is needed to serve as the bulk capacitor at the  $V_{IN}$  pin of the LP3220H. An additional 0.1 $\mu$ F is strongly recommended to provide additional high frequency filtering and should be placed to the  $V_{IN}$  pin and GND as close as possible.

### PCB Layout Guidelines

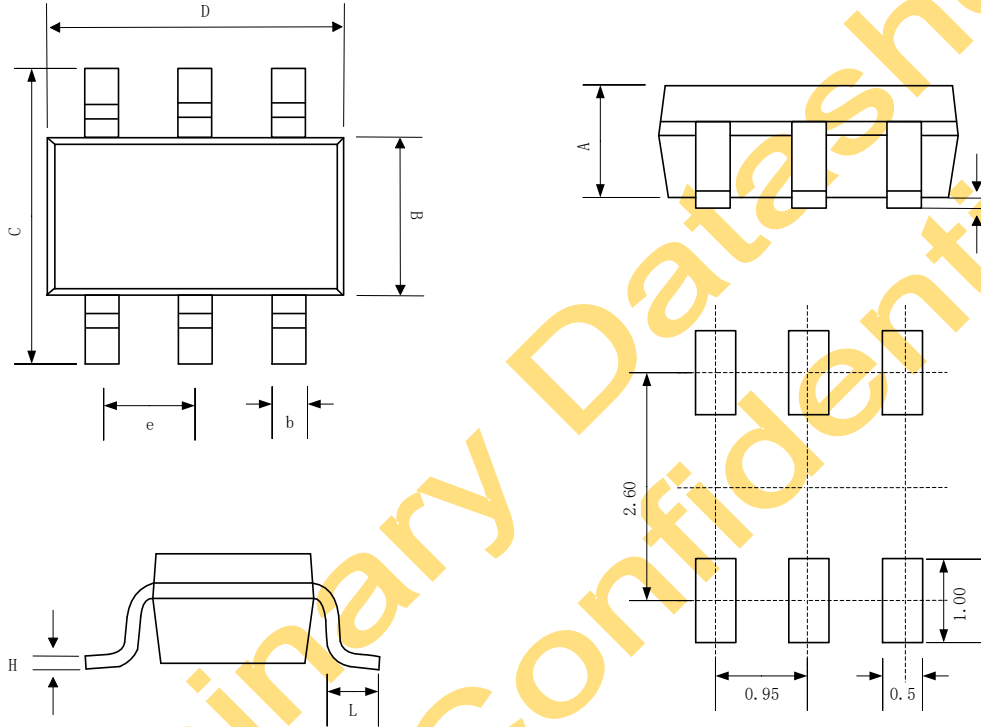
The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor as close as possible to  $V_{IN}$  pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.



Packaging Information

SOT23-6

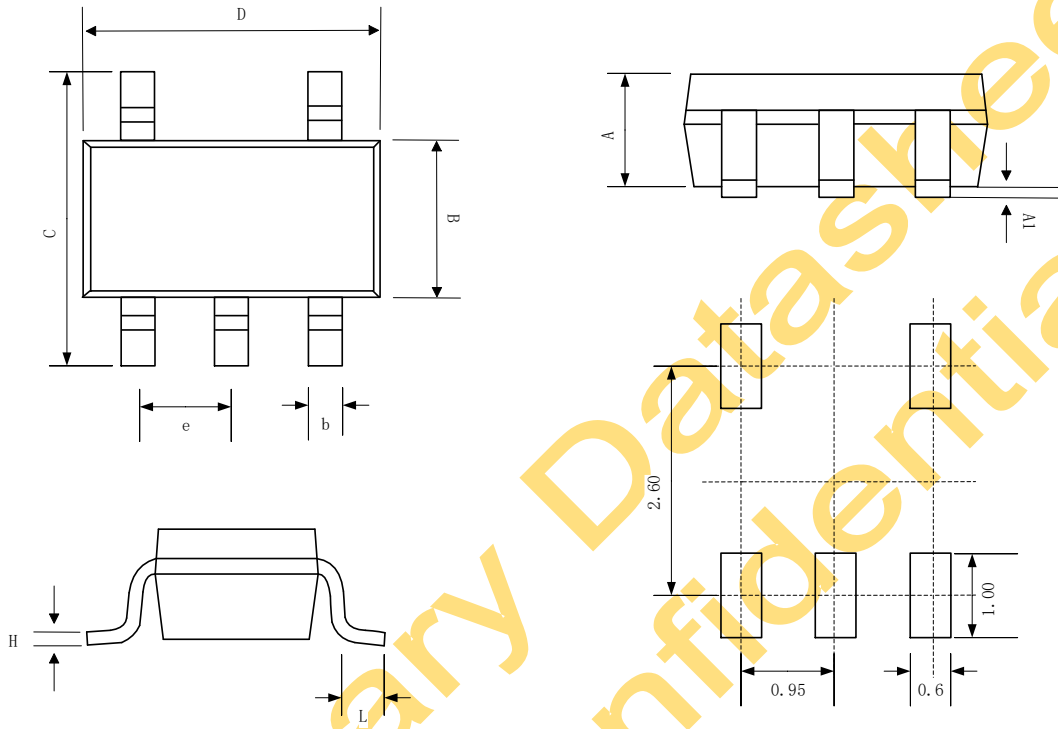


Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610



SOT23-5

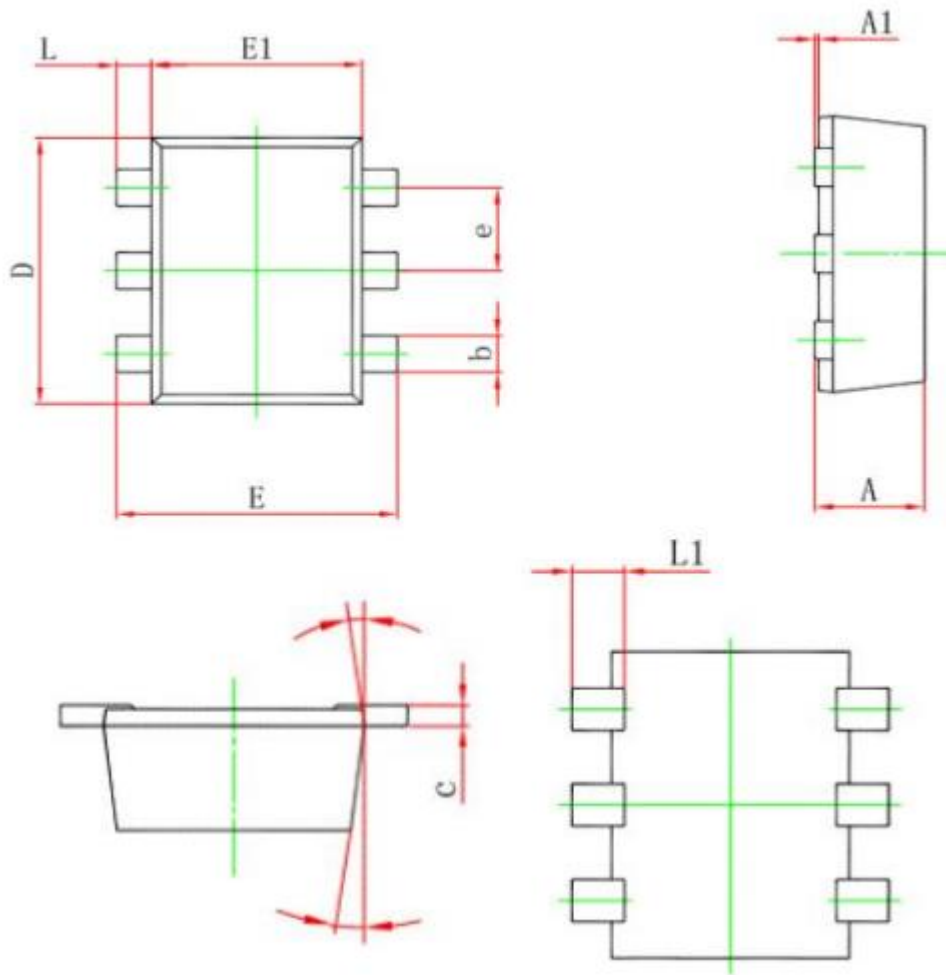


Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610



SOT563



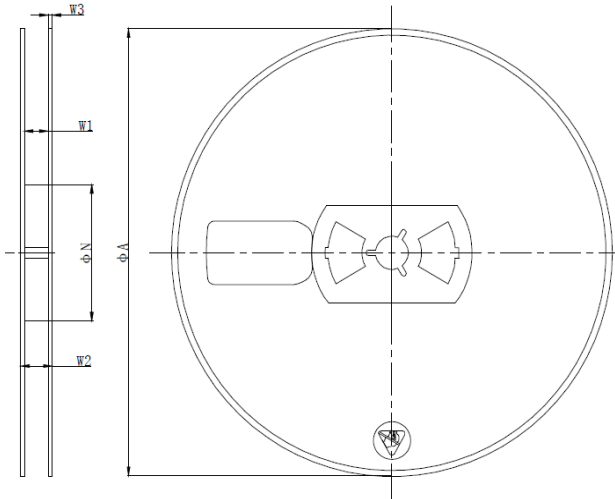
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	0.025	0.050
e	0.450	0.500	0.550
c	0.100	0.150	0.200
D	1.500	1.600	1.700
b	0.150	0.250	0.350
E1	1.100	1.200	1.300
E	1.500	1.600	1.700
L	0.100	0.200	0.300
L1	0.200	0.300	0.400
θ	7° REF		



## Tape and Reel Information

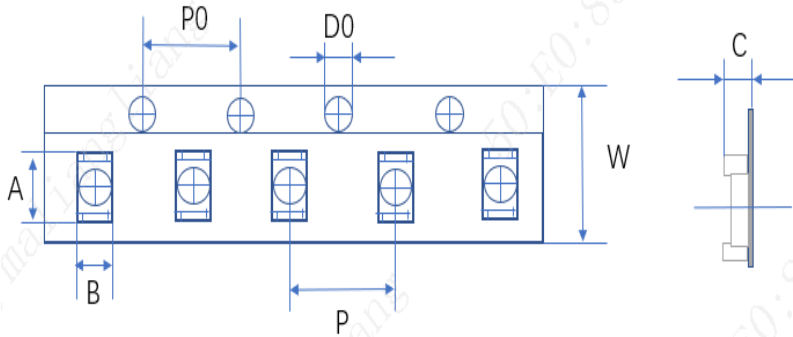
SOT23-5&SOT23-6

### REEL DIMENSIONS



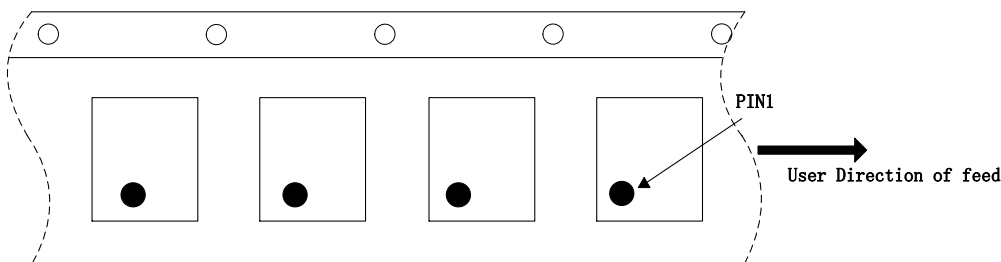
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
$\phi A$	176.00	180.00	184.00
W2	10.00	12.00	14.00

### TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	3.06	3.26	3.46
P0	3.90	4.00	4.10
P	3.90	4.00	4.10
D0	1.35	1.50	1.65
W	7.70	8.00	8.30
C	1.20	1.40	1.60

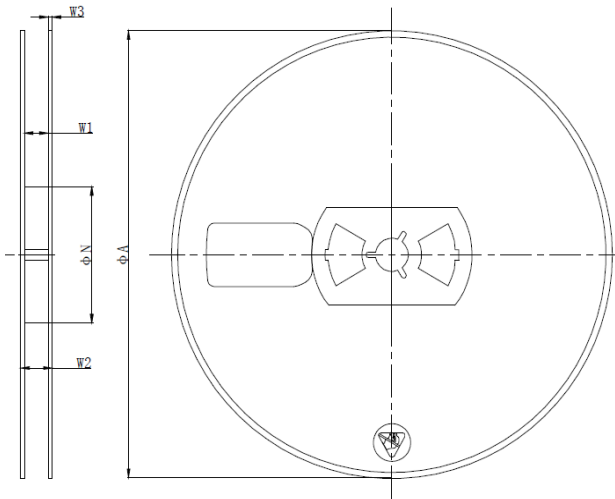
### PIN1 AND TAPE FEEDING DIRECTION





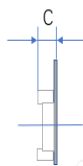
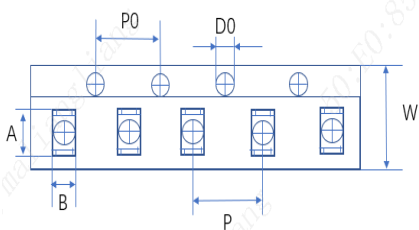
SOT563

REEL DIMENSIONS



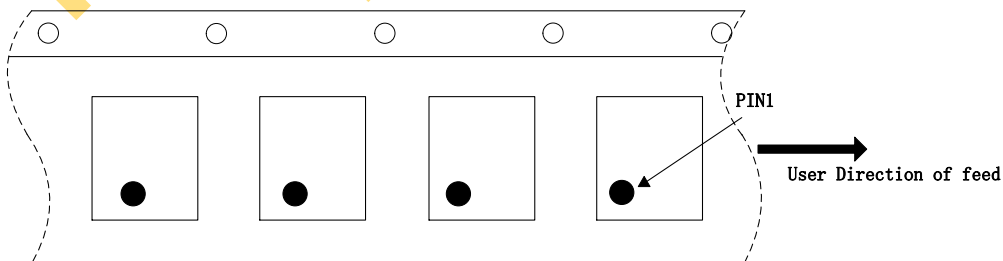
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
$\phi A$	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.63	1.83	2.03
B	1.60	1.80	2.00
P0	3.80	4.00	4.20
P	3.80	4.00	4.20
D0	1.30	1.50	1.70
W	7.70	8.00	8.30
C	0.55	0.75	0.95

PIN1 AND TAPE FEEDING DIRECTION





## Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat/Soak</b>		
Temperature Min( $T_{SMIN}$ )	100°C	150°C
Temperature Max( $T_{SMAX}$ )	150°C	200°C
Time( $T_s$ ) from ( $T_{SMIN}$ to $T_{SMAX}$ )	60~120 seconds	60~120 seconds
Ramp-up rate ( $T_L$ to $T_P$ )	3°C/second max	3°C/second max
Liquidous temperature( $T_L$ )	183°C	217°C
Time( $t_L$ ) maintained above $T_L$	60~150 seconds	60~150 seconds
Peak package body temperature ( $T_P$ )	For users $T_P$ must not exceed the Classification temp in Table 1. For suppliers $T_P$ must equal or exceed the Classification temp in Table 1.	For users $T_P$ must not exceed the Classification temp in Table 2. For suppliers $T_P$ must equal or exceed the Classification temp in Table 2.
Time( $t_P$ )* within 5°C of the specified classification temperature( $T_C$ ), see Figure1	20* seconds	30* seconds
Ramp-down rate ( $T_P$ to $T_L$ )	6°C/second max	6°C/second max
Time 25°C to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature ( $T_P$ ) is defined as a supplier minimum and a user maximum.		

**Table 1 Sn-Pb Eutectic Process - Classification Temperatures ( $T_C$ )**

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5mm	235°C	220°C
≥2.5mm	220°C	220°C

**Table 2 Pb-Free Process - Classification Temperatures ( $T_C$ )**

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350~2000	Volume mm <sup>3</sup> ≥350
<1.6mm	260°C	260°C	260°C
1.6mm~2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

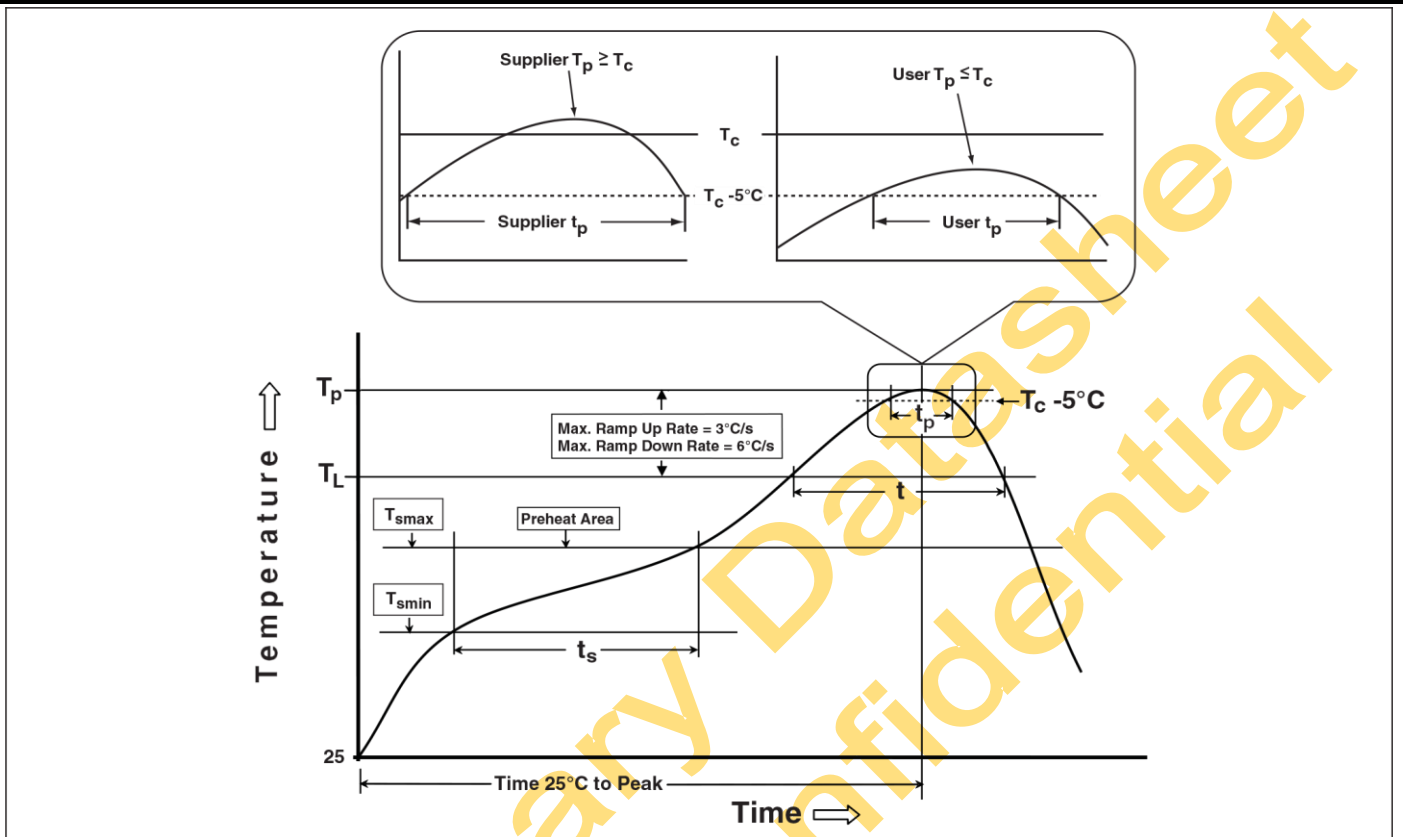


Figure1 Classification Profile (Not to scale)

Products conform to “JEDEC J-STD-020C” standards;

Products shipped conform to “Rohs” standards;

Moisture Sensitivity Level: MSL3 (CONDITION:  $\leq 30\text{ }^{\circ}\text{C}/60\%\text{RH}$ 、Time control:168 hours) ;



## Revision History

Revision	Date	Change Description
Rev0.1	5/24/2025	First version
Rev0.2	7/24/2025	Add SOT563 package information

Preliminary Datasheet  
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