LP6434SPF

30V, 4A Synchronous BUCK Switching Converter

Features

- Wide input voltage range: 4.2V – 30V, 32V absolute maximum voltage rating
- Output voltage range: V_{ref} – 13.2V
- High efficiency operation
  - Integrated a 40-mΩ LS-MOSFET and a 70-mΩ HS-MOSFET
  - 95% peak efficiency from 12V to 5V conversion
- Constant-on time (COT) control with fast transient response
- ±1% 0.6V Vref accuracy
- Typical 500-kHz switching frequency
- 95% maximum duty cycle
- Programmable soft-start time
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- ESOP-8 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV and TV box
- 12V Industrial bus applications

General Description

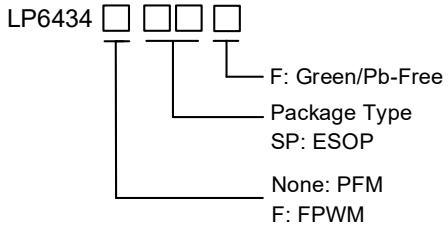
The LP6434SPF is a high efficiency synchronous buck converter supporting up to 4A output current and low heat. The LP6434SPF employs an adaptive constant-on-time (COT) control scheme to achieve fast load transient response and without external compensation. The external components are minimized, requiring only one inductor, several resistors and capacitors.

The LP6434SPF supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

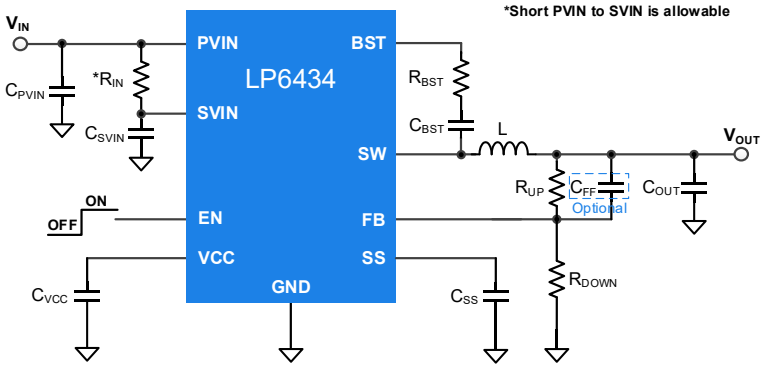
The LP6434SPF integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP6434SPF also integrates multiple protection functions, i.e., over-voltage protection (OVP), over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), and short circuit protection (SCP).

The LP6434SPF is available in an 8-pin ESOP-8 package.

Order Information



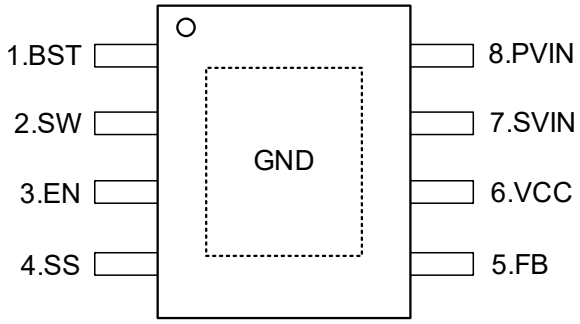
Typical Application Circuit



Device Information

Part Number	Top Marking	Output Current	Operation Mode	V_{ref}	Package	Shipping	MSL
LP6434SPF	LPS LP6434 YWX	4A	PFM/PWM	0.6V	ESOP-8	4K/REEL	LEVEL 3
LP6434FSPF	LPS LP6434 FYWX	4A	FPWM	0.6V	ESOP-8	4K/REEL	LEVEL 3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. **MSL: Moisture Sensitivity Level according to JEDEC Standard.**							

Pin Diagram



LP6434SPF Pinout

Pin Description

Pin #	Name	Description
1	BST	Bootstrap pin. Power supply for high-side MOSFET gate driver. A 0.1-μF capacitor series with a 47-Ω resistor is recommended to be connected between this pin and SW pin.
2	SW	The switching node of the converter.
3	EN	Enable input. This pin can be used to control the system power sequence as well.
4	SS	Soft start bias current output pin. A capacitor must be connected between this pin and GND pin to program the soft start time.
5	FB	Feedback pin. Use a resistor divider to set the desired output voltage.
6	VCC	Internal LDO output pin. A 1-μF or higher capacitor must be connected between this pin and GND pin.
7	SVIN	IC control power input. Connect a 1-μF bypass capacitor from this pin to the ground. A typical 100-Ω resistor can be connected between SVIN and PVIN, but short SVIN to PVIN pin directly is also supported, which is determined by specific application.
8	PVIN	IC power FET supply input. Decouple this pin with at least a 10-μF ceramic capacitor to the ground. If there is no strong request of decoupling the control input and power input, this pin can be directly connected to SVIN pin.
Thermal PAD	GND	Power ground of the IC.

Absolute Maximum Ratings (Note)

PVIN, SVIN, SW, and EN to GND ---------- -0.3V to 32V

VCC, FB, SS to GND ---------- -0.3V to 6.5V

BST to SW ---------- -0.3V to 6.5V

SW to GND (20ns transient) ---------- -3.5V to 32V

Junction Temperature Range (T_J) ---------- -40°C to 150°C

Maximum Soldering Temperature (at leads, 10 sec) ---------- 260°C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV

CDM (Charged-device Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance, ESOP-8) ---------- 35°C/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	4.2		30	V
V_{OUT}	Output voltage range	V_{ref}		13.2	V
T_A	Ambient temperature range	-40		85	°C
L	Inductor	3.3		10	μH
C_{PVIN}	Power input decoupling capacitor	4.7	10	100	μF
C_{SVIN}	Control input bypass capacitor	1		10	μF
C_{OUT}	Output capacitor	47		150	μF
C_{VCC}	VCC capacitor	1		2.2	μF
C_{BST}	BST-SW capacitor		0.1		μF

Electrical Characteristics

(The specifications are measured under conditions V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_R}	Input under voltage lockout threshold	V_{IN} rising threshold	3.8	4.0	4.2	V
V_{ULVO_H}	UVLO hysteresis	V_{IN} falling threshold		0.3		V
I_{Q_VIN}	Input quiescent current	No switching, V_{EN}=3V, V_{FB}=1.0V		250		μA
I_{SD_VIN}	Input shutdown current	V_{EN}=0, V_{IN}=12V		1.5	5	μA
BUCK CONVERTER						
I_{LIM}	Low-side valley current limit	T_A=25°C, 4A version	3.95	4.2	4.5	A
I_{NLIM}	Low-side negative current limit (ZCD)	PFM/PWM version		0.15		A
		FPWM version		-3		A
V_{ref}	Reference voltage	T_A=25°C, 0.6V version	0.594	0.6	0.606	V
		T_J=-40°C~125°C	0.585		0.615	V
		T_A=25°C, 0.8V version	0.792	0.8	0.808	V
R_{DS_H}	High-side FET on resistance	V_{IN}=12V		70		mΩ
R_{DS_L}	Low-side FET on resistance	V_{IN}=12V		40		mΩ
R_{DIS}	SW discharge FET on resistance	V_{IN}=12V		50		Ω
F_{SW}	Switching frequency	500kHz	375	500	625	kHz
t_{ON_MIN}	Minimum on-time[1]			100	200	ns
D_{MAX}	Maximum duty cycle	V_{FB}=0.8*Vref, V_{IN}=5V		95		%
t_d	EN delay time[1]	From EN high to first switching		150		μs
t_{SS}	Soft-start time[1]	SS pin float, from first switching to 0.95*Vref		1		ms

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SS}	Soft-start bias current			10		μA
V_{UVP_F}	UVP threshold	FB falling edge, reference to Vref	40	50	60	%
V_{UVP_R}	UVP recovery threshold	FB rising edge, reference to Vref		60		%
V_{OVP_R}	OVP threshold	FB rising edge, reference to Vref	108	113	118	%
V_{OVP_F}	OVP recovery threshold	FB falling edge, reference to Vref		108		%
I_{LEAK_FB}	FB pin leakage current			0.01		μA
THERMAL SHUTDOWN						
T_{JSD}	Thermal shutdown threshold	Rising threshold	140	155	170	°C
	Thermal shutdown recovery threshold	Falling threshold		135		°C
EN LOGIC						
V_{EN_H}	EN pin logic high threshold	EN rising threshold	1.1	1.2	1.3	V
V_{EN_HYS}	EN pin threshold hysteresis			0.2		V
R_{EN_DOWN}	EN pin internal pull-down resistance			1500		kΩ

[1]: Not production tested. Guaranteed by design.

Typical Characteristics

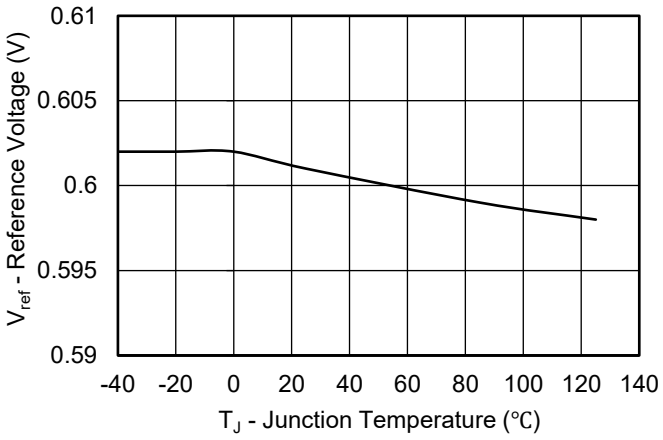


Figure 1. Reference Voltage vs. Temperature (V_{IN}=12V, I_{OUT}=0A)

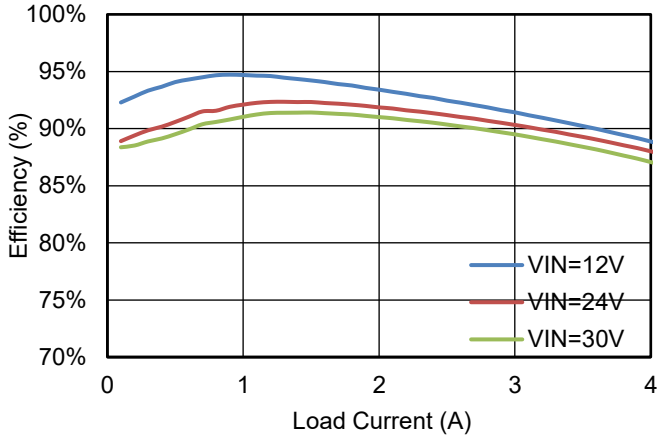


Figure 2. Efficiency vs. Load Current (V_{OUT}=5.0V, L=4.7μH with 12mΩ DCR, R_{BST}=47Ω)

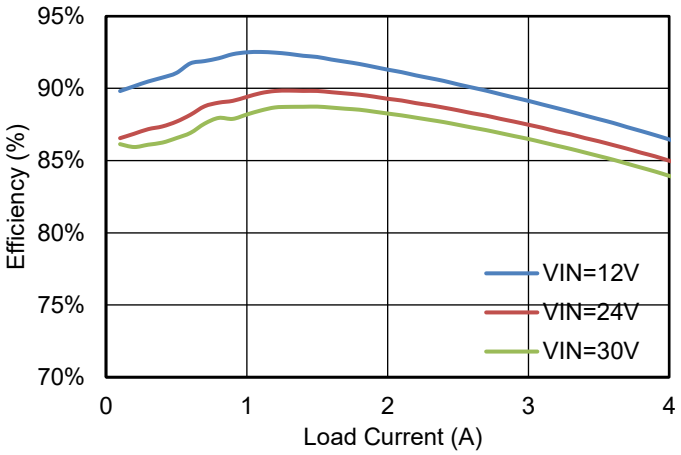


Figure 3. Efficiency vs. Load Current (V_{OUT}=3.3V, L=3.3μH with 11mΩ DCR, R_{BST}=47Ω)

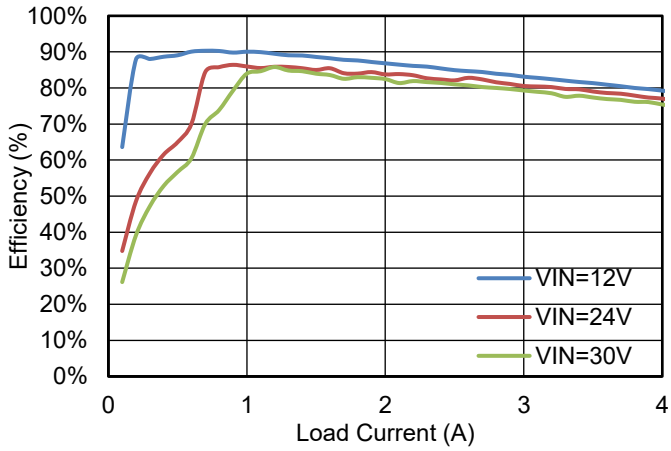


Figure 4. Efficiency vs. Load Current (V_{OUT}=1.8V, L=3.3μH with 11mΩ DCR, R_{BST}=47Ω)

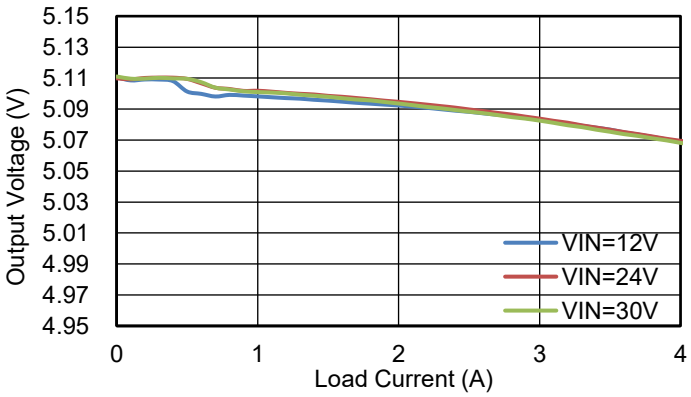


Figure 5. Output Voltage vs. Load Current (VOUT=5.0V, L=4.7μH with 12mΩ DCR, R_{BST}=47Ω)

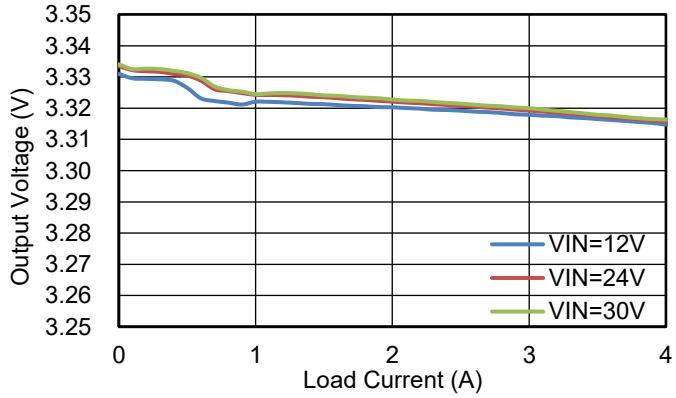


Figure 6. Output Voltage vs. Load Current (VOUT=3.3V, L=3.3μH with 11mΩ DCR, R_{BST}=47Ω)

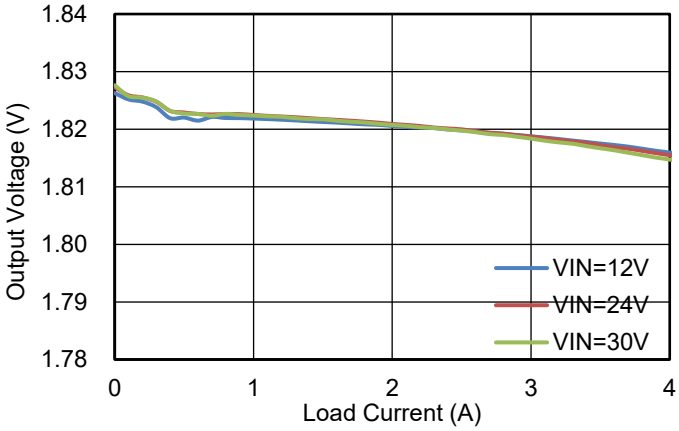
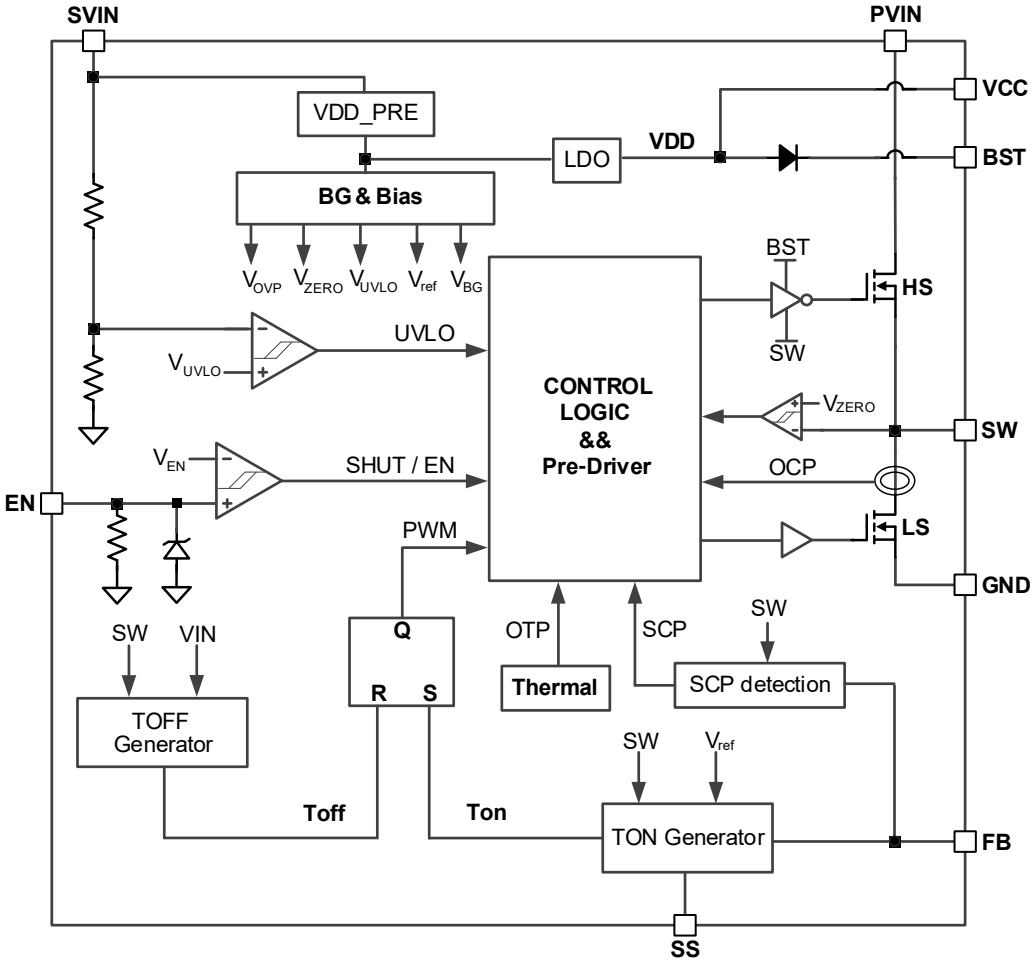


Figure 7. Output Voltage vs. Load Current
(VOUT=1.8V, L=3.3μH with 11mΩ DCR, R_{BST}=47Ω)

Functional Block Diagram



Detailed Description

Overview

The LP6434SPF is a 4A integrated MOSFET synchronous buck converter, supporting 4.2-30V input voltage range. This device adopts adaptive COT control scheme which enables fast transient respond and minimizes the output capacitance. The LP6434SPF supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP6434SPF automatically transfers between PFM at light load and PWM at heavy load according to the output current.

Under Voltage Lockout (UVLO)

When the input voltage VIN is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP6434SPF can be enabled by the EN pin. This function is non-latching.

EN Control and Soft-Start

The EN pin can be used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP6434SPF enables all the internal circuits and begins the soft-start. The EN pin has an internal 1500-kΩ pull-down resistor to ground to prevent the noise from falsely enabling the converter at shutdown mode.

The LP6434SPF integrates soft-start function with a typical startup time of 1-ms (t_{SS}) if SS pin floating. After passing the UVLO threshold and enabled by the EN pin with the 150-μs delay (t_d), the internal reference voltage ramps from zero to the Vref in 1-ms and the output voltage ramps up accordingly. Soft-start time also supports programming by charging the external soft-start capacitor at SS pin with an internal bias current.

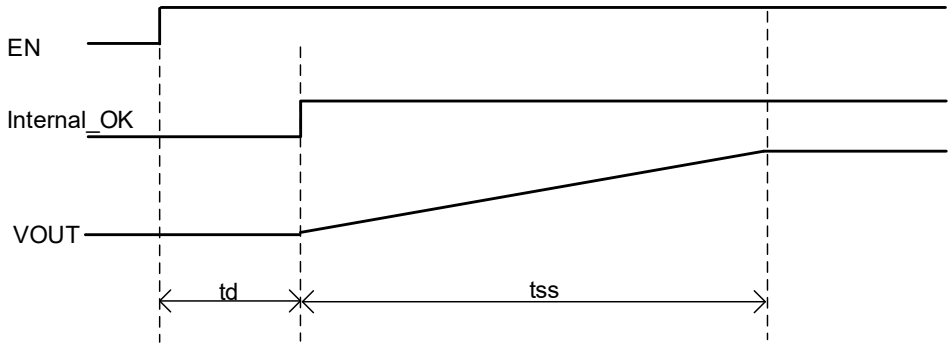


Figure 8. Soft Start Sequence

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes higher than the feedback voltage.

Constant-ON Time (COT) Control Scheme

The LP6434SPF integrates the COT control scheme for pseudo-fixed-frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal on-time generator block monitors the FB-pin voltage and turns on the high-side MOSFET to start a switching cycle, when the FB-pin voltage drops to an internal reference voltage Vref. Then the internal circuits start to calculate the on-time of the high-side MOSFET, which is proportional to the input voltage and inversely proportional to the output voltage. Once the on-time is finished, the TOFF generator turns off the high-side MOSFET and turns on the low-side MOSFET.

PFM Operation (LP6434SPF)

The LP6434SPF is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

FPWM Operation (LP6434FSPF)

The LP6434FSPF is designed to work at FPWM to maintain the good regulation and transient performance. When the output decreases, the inductor current is allowed to flow from the output to the ground plane. In this way, the switching frequency is kept the same even without load.

The negative current limit is -3A typically.

The FPWM operation mode can reduce the output ripple under light load at the cost of lower light load efficiency.

Output Active discharge function

The LP6434SPF sinks current from the SW pin when the device is shut down by EN, input UVLO or output OVP. An internal 50-Ω on-resistance FET is turned on and the energy from the output capacitor is discharged to the ground under these states. The input power supply should remain present for the output discharge function to be active.

Table 1. Output Discharge Logic Table

State	Description	Output Discharge
EN=Low	VIN>=VTH	YES
EN=High	VIN>=UVLO	NO
UVLO	VTH=<VIN<UVLO	YES
UVLO	VIN<VTH	LOSE CONTROL
OVP	FB>=113%*Vref	YES
OVP recover	FB<108%*Vref	NO
Thermal shutdown	VIN>=VTH	YES
Soft start	VIN>=UVLO, EN=High	NO

Bootstrap Capacitor

The LP6434SPF integrates two N-MOSFETs to achieve high efficiency. The high-side MOSFET is powered by the typical 100-nF bootstrap capacitor $C_{BST.}$ A 47-Ω resistor R_{BST} must be connected in series with C_{BST} between the BST pin and SW pin to achieve enough current capability and good stability.

Over Current Protection (OCP) and Short Circuit Protection (SCP)

The LP6434SPF protects an over current situation by limiting the inductor valley current. The current of low-side MOSFET is monitored all the time to sense the inductor valley current when the LP6434SPF is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side valley current limit. The inductor current is limited to the valley current limit pluses a half of the inductor ripple current in this way.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to 50% of the Vref for 1.5-ms, the LP6434SPF shuts down. The LP6434SPF will restart automatically after at least 32-ms waiting time. If the SCP condition still holds after soft-start, the LP6434SPF shuts down again, repeating the operation described above.

When the over current condition is removed, the LP6434SPF returns to normal operation.

Over Voltage Protection (OVP)

The LP6434SPF protects an over voltage situation by turning off the power stage. The FB voltages monitored all the time to sense the output voltage when the LP6434SPF is enabled. The high-side MOSFET is turned off immediately if the FB voltage is higher than the V_{OVP_R} threshold. The high-side MOSFET is allowed to be turned on if the output voltage falls below V_{OVP_F} threshold. The output voltage is discharged by SW pin if the OVP signal lasts for 26-μs.

Thermal Protection (OTP)

The LP6434SPF has a thermal protection function. The device will shut down when the internal temperature is higher than 155°C and will restart after the temperature drops below 135°C.

Application Information

Design Requirements

The table 2 shows the design parameters for a typical 5V output application.

Table 2. Design Parameters

Parameter	Target
Input voltage range	9V~30V
Output voltage	5V
Transient ripple	±200mV
Operating frequency	500kHz

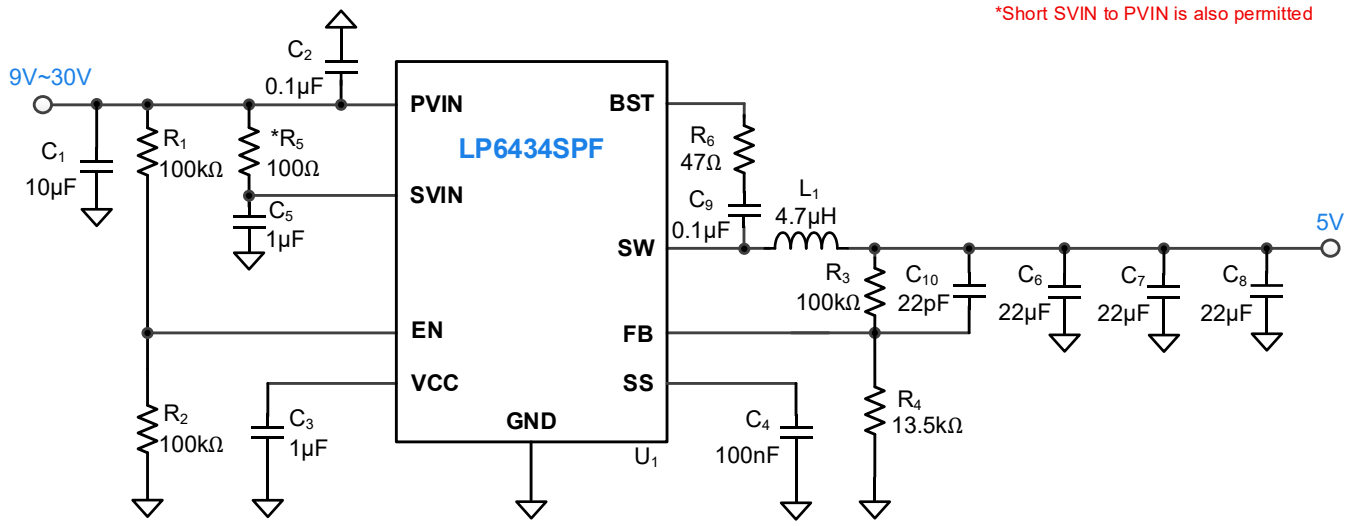


Figure 9. Typical Schematic of 5V Output

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1\right) * V_{ref}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V for LP6434SPF.
For better accuracy, the R_{DOWN} is recommended to be lower than 100-kΩ to ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current. A resistor with higher than 1-kΩ but lower than 100-kΩ is recommended to be placed between the resistor divider and FB pin if a C_{FF} capacitor is soldered.

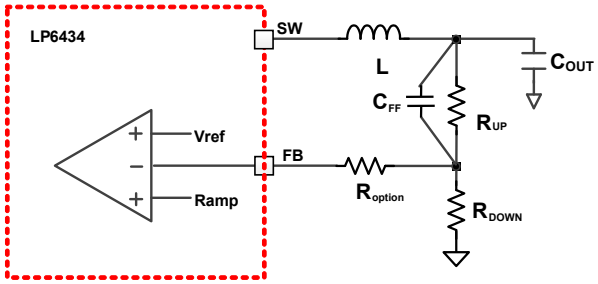


Figure 10. FB Connection of LP6434

EN Design

The LP6434SPF allows the user to design a precise VIN voltage to enable the converter during power on. The V_{EN} is the EN rising threshold voltage at which the converter is enabled, which is 1.2V typically. A 47pF-1nF capacitor is recommend to be soldered in parallel with the R_{EN_DOWN} to avoid the high-frequency noise influence from the switching node.

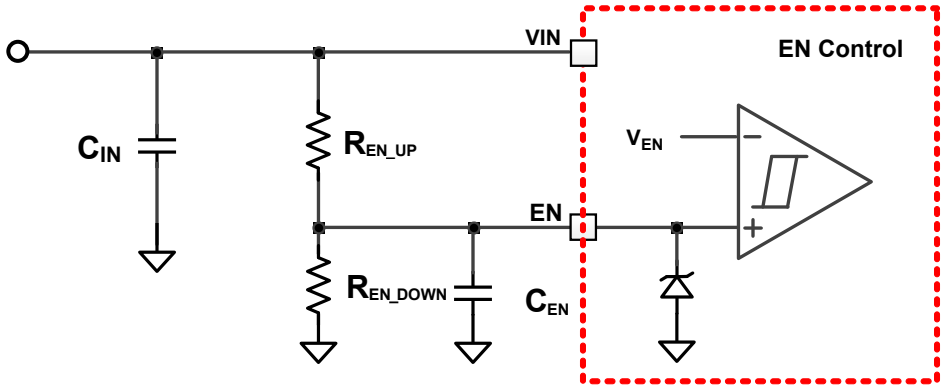


Figure 11. EN Connection of LP6434

Soft-Start Time Setting

The soft-start capacitor value can be calculated going with the following equation. Attention should be taken here that the programmed soft-start time should be at least 1-ms.

$$t_{SS} = \frac{C_{SS} * V_{ref}}{I_{SS}}$$

For this design, a 100-nF ceramic capacitor is used at SS pin to obtain 6-ms soft-start time. If SS pin float, the soft-start time will be set to 1-ms internally.

Inductor and Output Capacitor

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * F_{SW}} * \frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs. For a typical 12V input voltage and 5V output voltage, a low DCR value, 4.7-μH inductor is recommended. To be noticed, the RMS current of inductor must cover maximum continuous load current and its saturation current must be higher than 6.5A.
The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor C_{FF} can be selected to improve the transient behavior. The typical capacitance of C_{FF} can be 22~47pF. For this design, three 10V, X5R, 22μF capacitors (GRM21BR61A226ME44) are soldered at the VOUT to GND. For 12V output design, output and feedforward capacitors should satisfy 25V voltage rating.

Table 3. Recommend R/L/C values (500kHz)

V_{OUT}	Inductor-L	C_{OUT}	R_{UP}	R_{DOWN}	R_{BST}	C_{FF}
1.8V	3.3μH	22μF*3	100 kΩ	50 kΩ	47 Ω	NA
3.3V	3.3μH~4.7μH	22μF*3~22μF*4	100 kΩ	22 kΩ	47 Ω	22pF~47pF
5.0V	4.7μH~6.8μH	22μF*3~22μF*5	100 kΩ	13.6 kΩ	47 Ω	22pF~47pF
12V	6.8μH~15μH	22μF*4~22μF*6	100 kΩ	5.1 kΩ	47 Ω	22pF~47pF

Bootstrap Capacitor

A 0.1-μF ceramic capacitor is needed to supply power for the high-side N-MOSFET driver. The voltage rating of the capacitor should be at least 10V. A 47-Ω resistor must be connected in series with the bootstrap capacitor.

Input Capacitor

A typical 10-μF ceramic capacitor is needed to serve as the decoupling capacitor at the PVIN pin of the LP6434SPF. An

additional 0.1-μF ceramic capacitor is strongly recommended to provide additional high frequency filtering and should be placed to the PVIN pin and GND as close as possible.

Application Waveforms (VIN=12V, L=4.7μH, COUT=22μF*3)

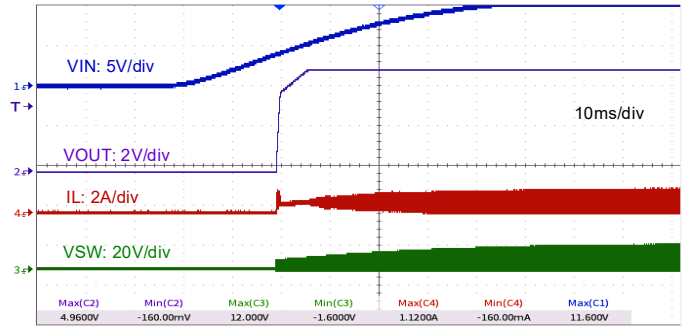


Figure 12. Startup by VIN, 10Ω load

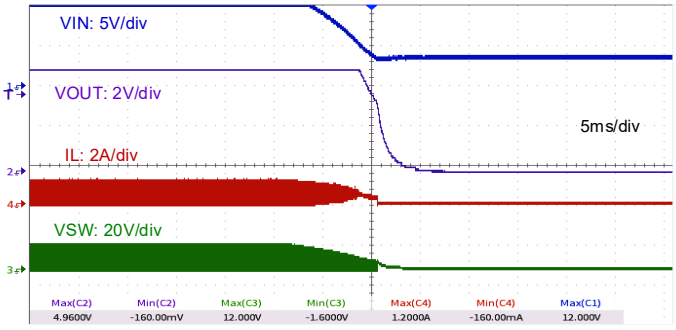


Figure 13. Shutdown by VIN, 10Ω load

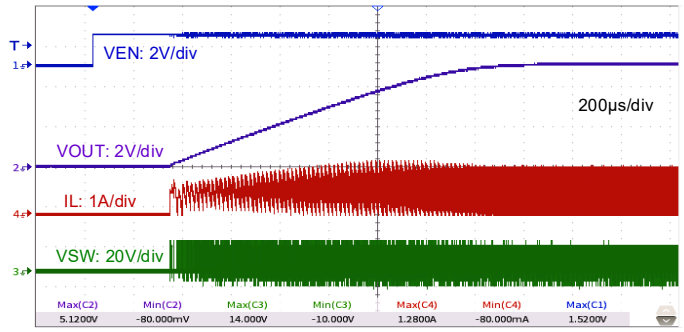


Figure 14. Startup by EN, 10Ω load

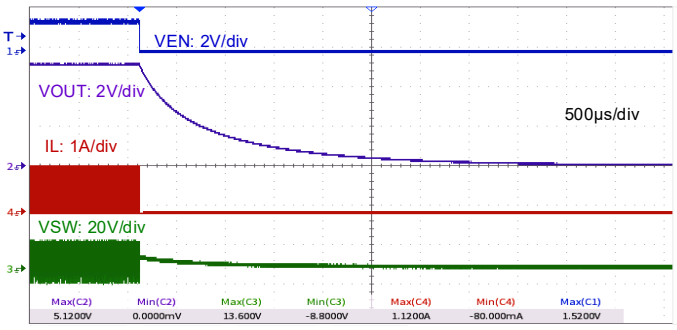


Figure 15. Shutdown by EN, 10Ω load

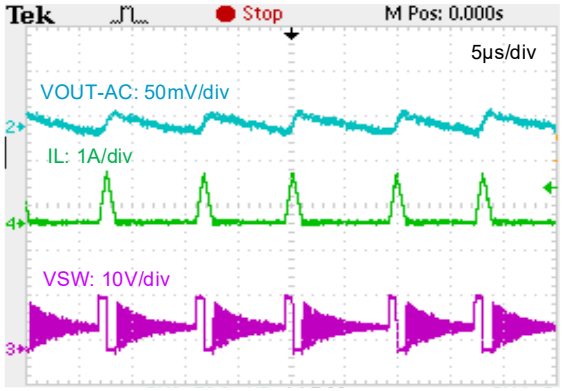


Figure 16. Switching Waveform, VOUT=5V, 0.1A load

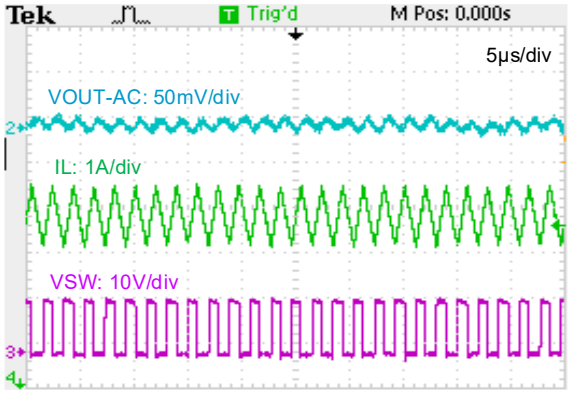


Figure 17. Switching Waveform, VOUT=5V, 4A load

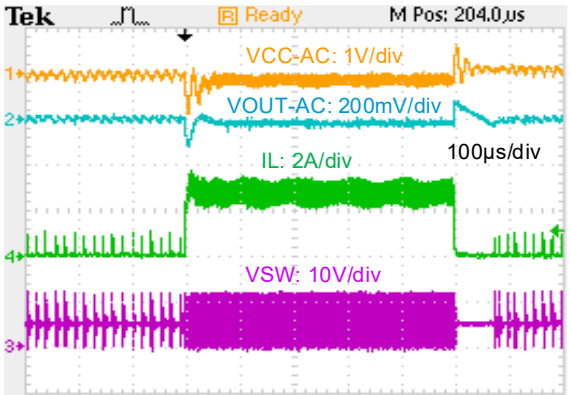


Figure 18. Load Transient, VOUT=5V, 0.1A-3A-0.1A

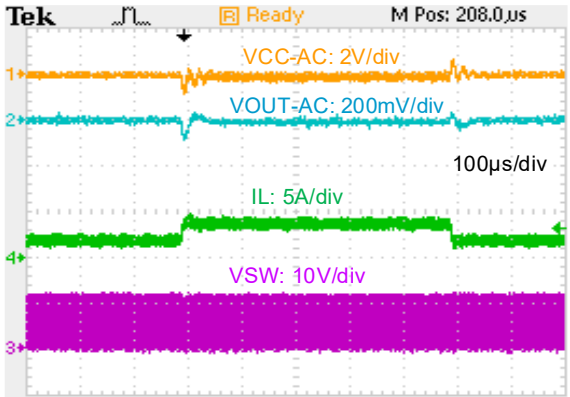


Figure 19. Load Transient, VOUT=5V, 2A-4A-2A

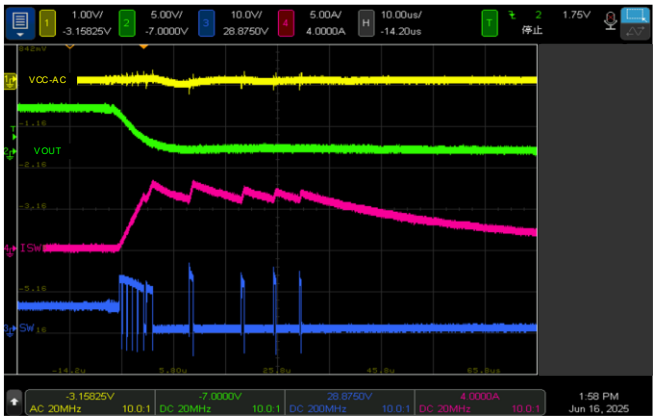


Figure 20. Output Null Load to Short, VOUT=5V

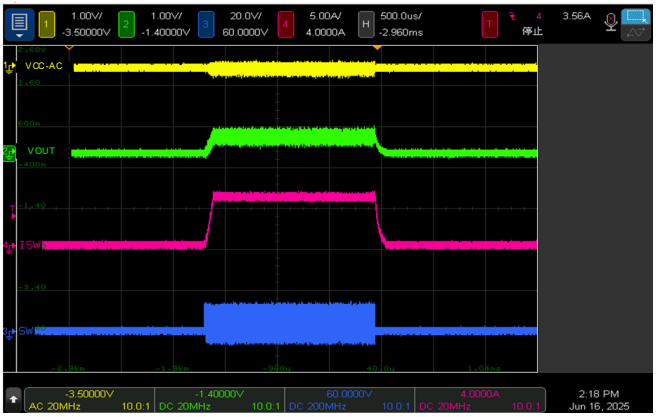


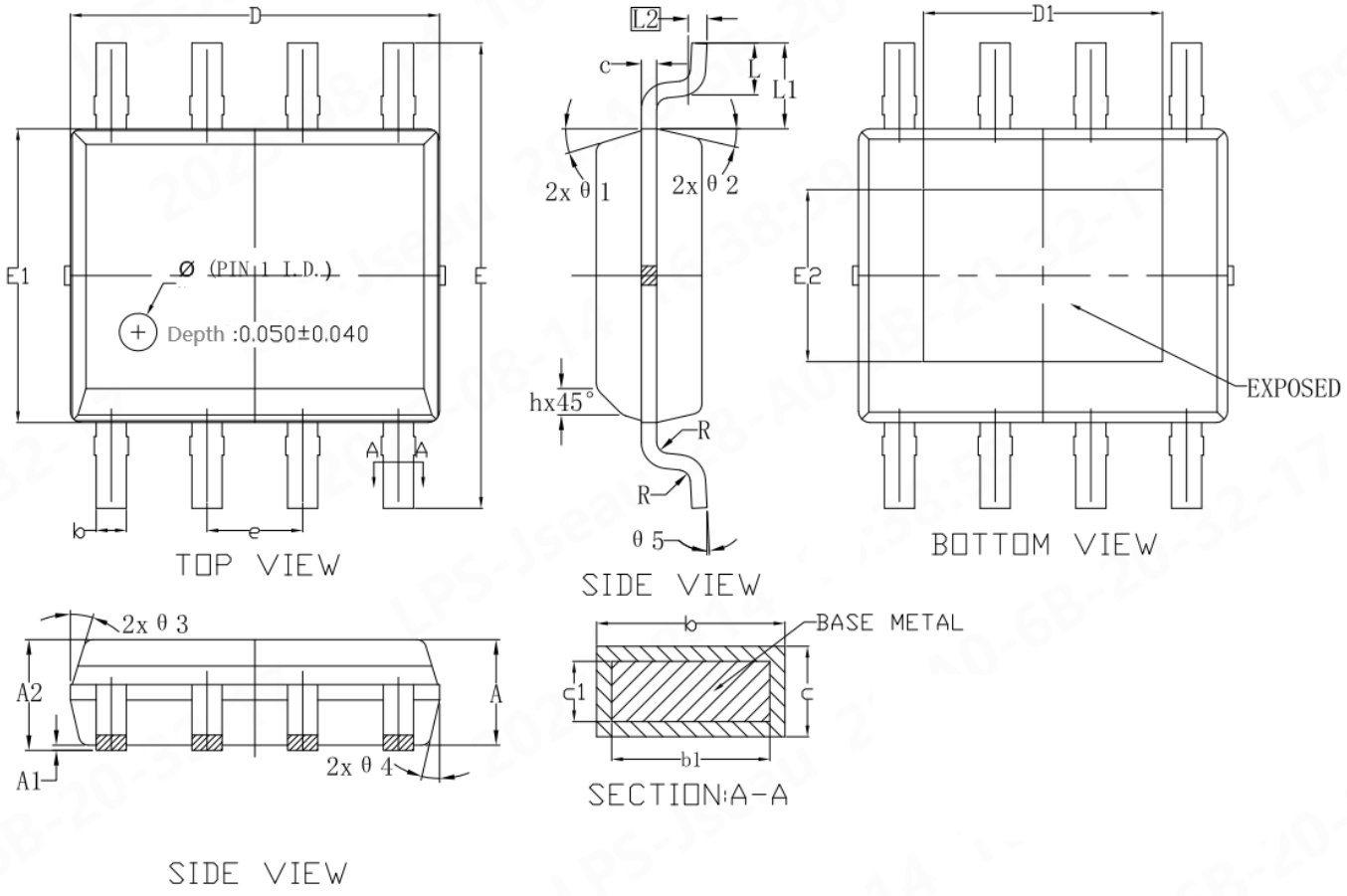
Figure 21. Output Short Hiccup Protection

PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor (C1 and C2) as close as possible to PVIN pin and GND pin and use shortest copper trace connection or GND plane. Place bypass capacitor (C5) as close as possible to SVIN pin and GND pin.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short and wide copper trace or GND plane.
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Minimize parasitic capacitance from this area to any other trace or plane.
- Place LDO output capacitor (C3) as close as possible to VCC pin. Place the feedback sensing resistor R3 and R4 as close as possible to the IC.
- Make sure the trace connecting to the FB pin not be adjacent to the SW copper area. If possible, keep the distance from the SW copper area to the feedback trace larger than 3-mm.

Packaging Information (ESOP-8)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.30	1.40	1.50
A1	0.00	/	0.12
A2	1.30	/	1.60
b	0.37	/	0.47
b1	0.35	/	0.45
c	0.17	/	0.27
c1	0.15	/	0.25
D	4.80	4.90	5.00
D1	3.02	/	/
E	6.00	/	6.30
E1	3.80	3.90	4.00
E2	2.13	/	/
e		1.27 BSC	
L	0.60	/	0.90
L1		1.14 REF	
L2		0.25 BSC	
R	0.07	/	/
h	0.25	0.35	0.45
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°
θ 5	-1.5°	/	5°
ø	0.40	0.50	0.60

Revision History

Revision	Date	Change Description
Rev 1p0	10/17/2025	Initial release